# ECE452/552
# Project #2
# Classical control design of digital controllers

**Purpose:** Gain familiarity designing digital compensators using classical control design approaches. Also, to gain experience in simulating the compensated closed loop digital system using Matlab/Simulink.

**Overview:**
Design two different compensators, one each for each of the classical design approaches discussed in class:

1) Discrete-time equivalents
2) w-plane approach

**Tasks:**
Design compensators for the following system:

$$G(s) = 10\frac{1-\frac{s}{33}}{\left(1+\frac{s}{10}\right)\left(1+\frac{s}{100}\right)}$$

Your final designs should satisfy the following specifications:

1. Phase margin > 55° while maximizing the unity gain bandwidth.
2. Zero steady state error to step input.

Use the same sampling frequency for the two designs.

Apart from the above, you are given wide latitude in how you approach your designs. However, in choosing your sampling frequency, do not make it "too high" as your designs will then be non-trivially different from the continuous-time system. Some experimentation will be needed here to try and reduce your sampling frequency.

**Report:**
Write a report documenting your designs. Your documentation should include (and not be limited to) the following:

1) Loop gain plot using the Matlab 'margin' command of your analog loop gain design.
2) Loop gain plot using the Matlab 'margin' command of your discretized loop gain design.
3) Simulink block diagram of your final designs.
4) Use your Simulink model to obtain the response to a unit step input.
5) Use the Matlab "stepinfo" command to quantify your step response performance.
6) A discussion concerning your choice of the sampling frequency (and your efforts to reduce it).

Email your completed report to tymerski@ee.pdx.edu by 5:00pm on Wednesday, March 14, 2018.