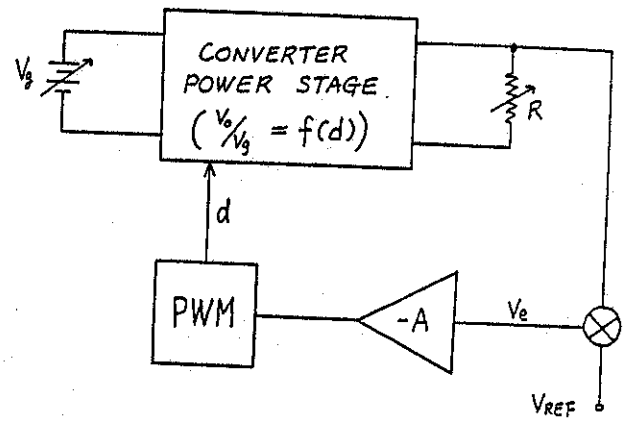
SINGLE-LOOP CONTROL FOR PWM CONVERTERS

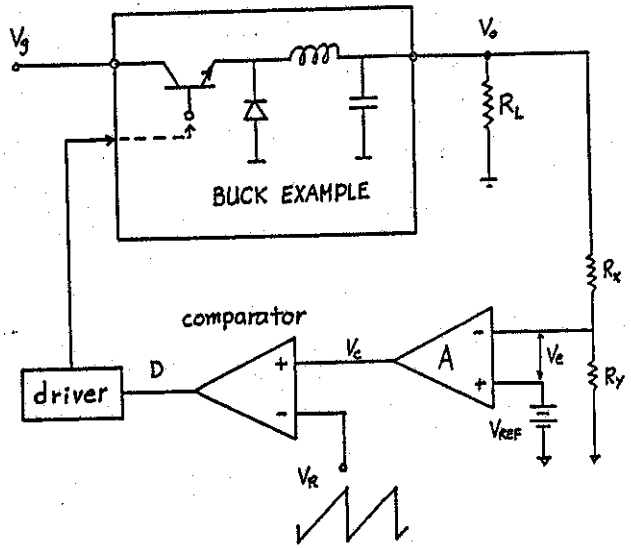
Single-Loop Controlled Switching Regulator

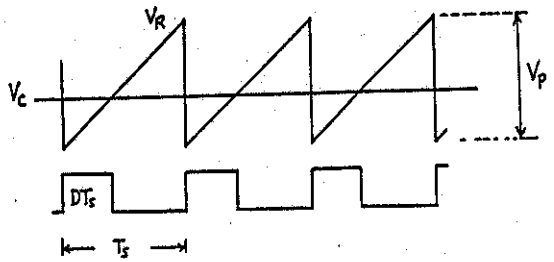


Feedback Control to Achieve :

- **Accuracy**
- **Speed**
- **Stability**

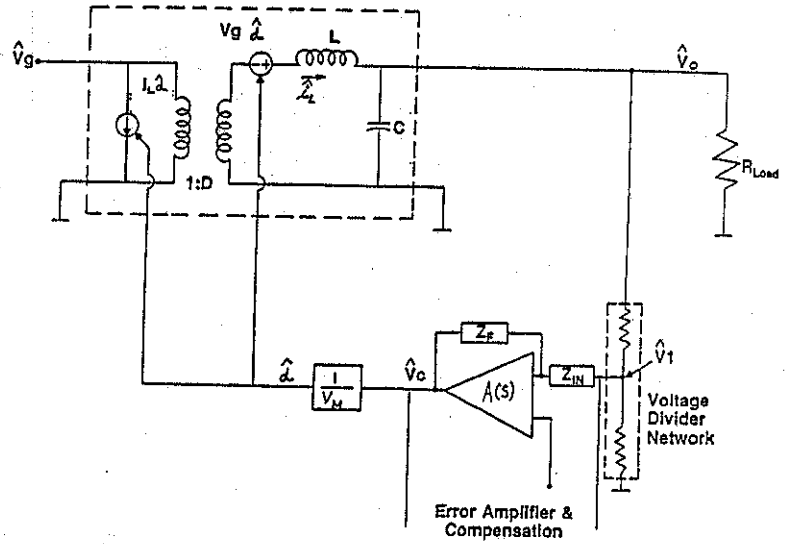
DC Analysis of Switching Regulators



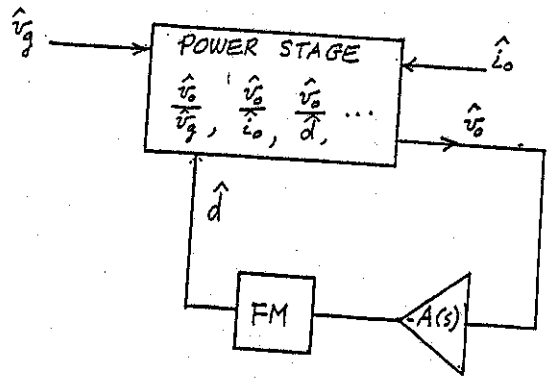


- DC PWM Gain : $\frac{D}{V_c} = \frac{1}{V_p}$

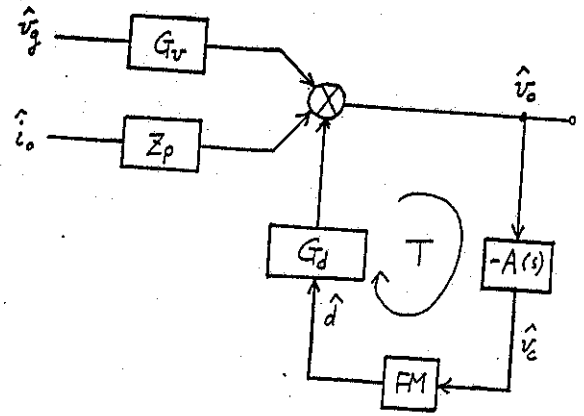
Small-Signal Analysis of Switching Regulators



Small-Signal Analysis of Switching Regulators



Small-signal Block diagram



5

where :

$G_v = \left.\frac{\hat{v}_o}{\hat{v}_g}\right|_{\hat{d}=0}$; open-loop audio susceptibility

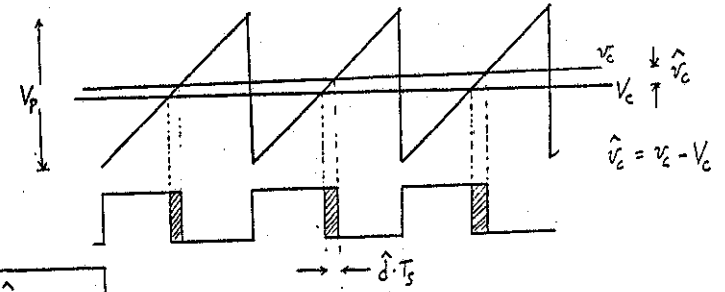
$Z_p = \left.\frac{\hat{v}_o}{\hat{i}_o}\right|_{\hat{d}=0}$; Open-loop output impedance

$G_d = \left.\frac{\hat{v}_o}{\hat{d}}\right|_{\hat{v}_g=\hat{i}_o=0}$; control to output transfer fn.

$A(s) = \frac{\hat{v}_c}{\hat{v}_o}$: Compensator gain

$FM = \frac{\hat{d}}{\hat{v}_c}$: PWM gain

• Small-signal PWM gain, FM



$FM = \frac{\hat{d}}{\hat{v}_c} = \frac{1}{V_p}$ note $\angle FM = 0°$

6

Closed-Loop Transfer Functions

- Closed-loop audio-susceptibility, $\left.\frac{\hat{v}_o}{\hat{v}_g}\right|_{i_o=0}$

$$\hat{v}_o = G_v \cdot \hat{v}_g + G_d \cdot \hat{d} \quad \text{— ①}$$

$$\hat{d} = -A \cdot FM \cdot \hat{v}_o \quad \text{— ②}$$

Eliminate $\hat{d}$ from ①&②

$$\Rightarrow \frac{\hat{v}_o}{\hat{v}_g} = \frac{G_v}{1 + G_d \cdot FM \cdot A} \triangleq \boxed{\frac{G_v}{1 + T}}$$

where $T \triangleq G_d \cdot FM \cdot A$; Loop gain

- Closed-loop output impedance, $\frac{\hat{v}_o}{\hat{i}_o}$

$$\hat{v}_o = Z_p \cdot \hat{i}_o + G_d \cdot \hat{d} \quad \text{— ③}$$

From ③ & ②

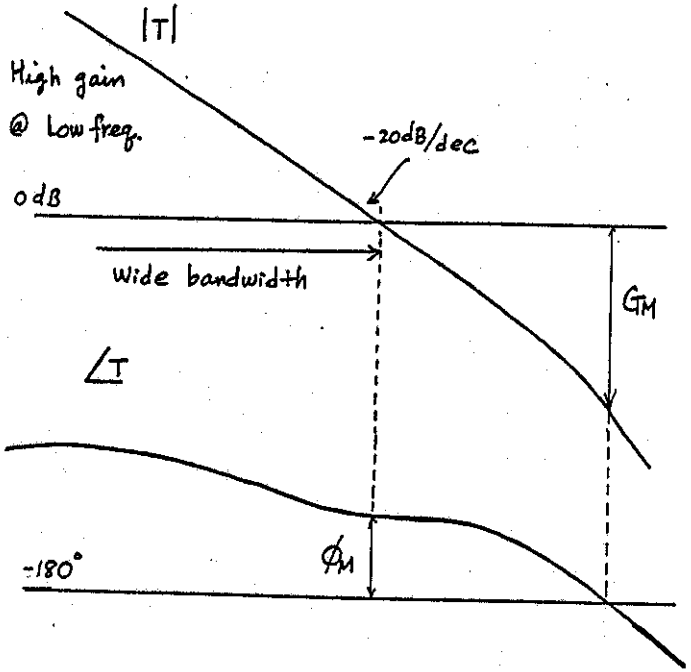
$$\boxed{\frac{\hat{v}_o}{\hat{i}_o} = \frac{Z_p}{1 + T}}$$

Loop Gain Analysis

Provides :

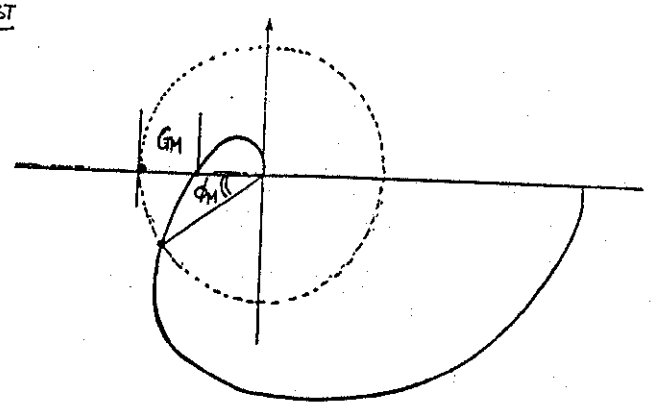
- System performance analysis
- Stability analysis
  - absolute stability
  - degree of stability
- Design insight
- Measurement verification

Desired Loop Gain Characteristics

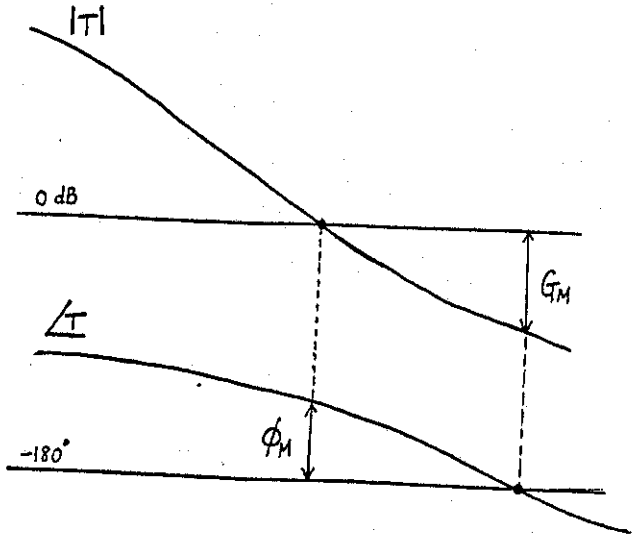


Stability Margins

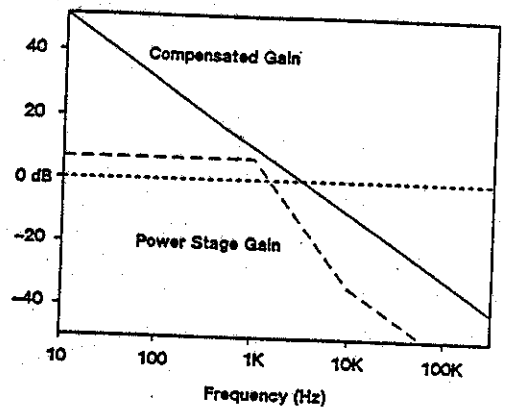
NYQUIST



BODE



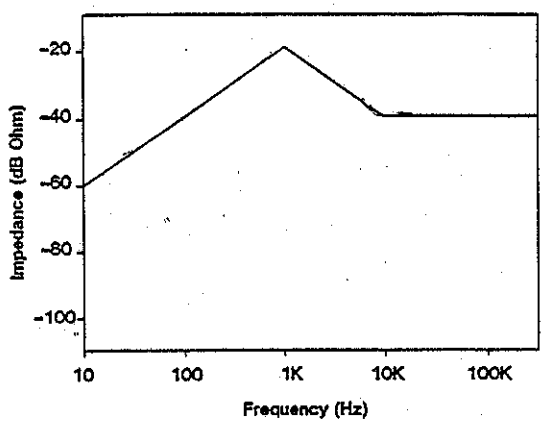
LOOP GAIN ASYMPTOTES



Compensation:

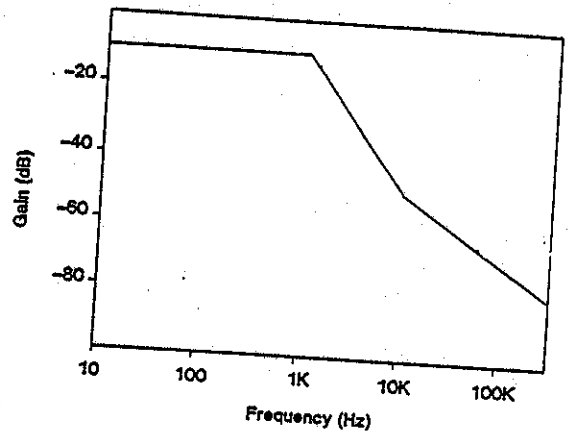
- Pole at Origin.
- Double Zero at f_0.
- Pole at ESR Zero

OPEN-LOOP OUTPUT IMPEDANCE ASYMPTOTES



- Zero at Origin ($R_l = 0$).
- Double Pole at f_0.
- Zero due to Capacitor ESR.

AUDIO SUSCEPTIBILITY ASYMPTOTES

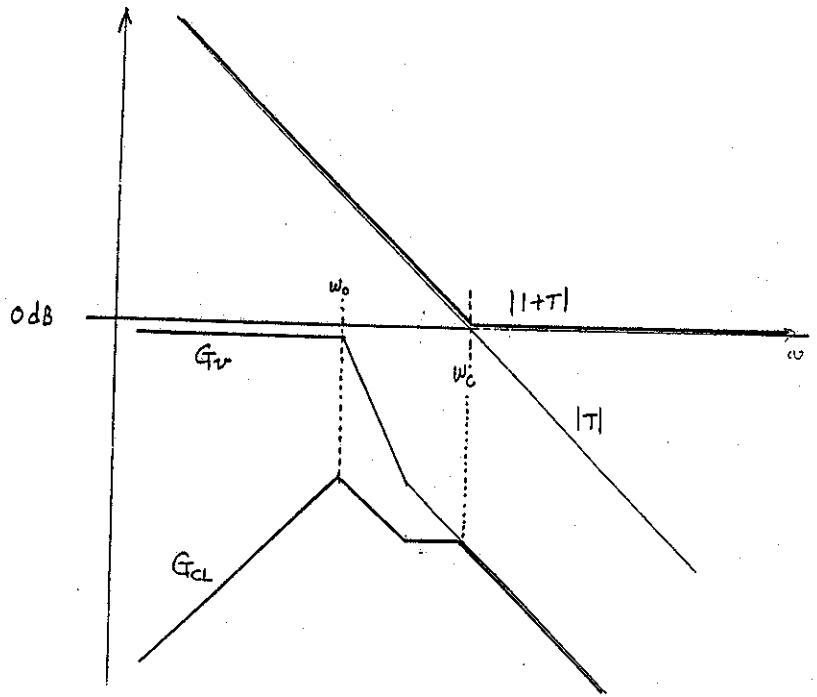


- DC Gain Determined by Steady-State Duty Cycle.
- Double Pole at f_0.
- Zero due to Capacitor ESR.

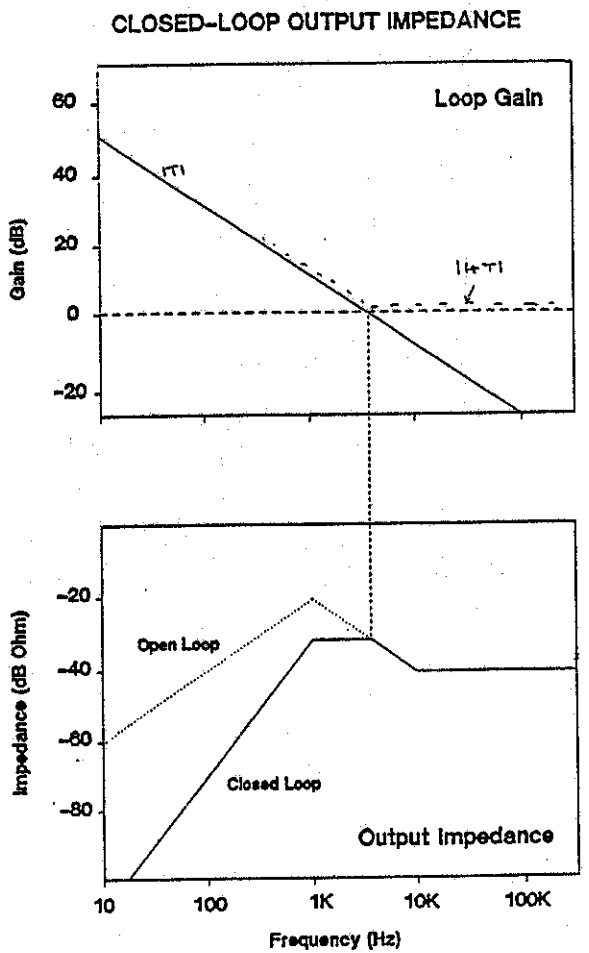
Function of the Loop Gain, T

Example : Closed-loop audio-susceptibility

$$\left.\frac{\hat{v}_o}{\hat{v}_g}\right|_{CL} = \frac{G_v}{1+T} \triangleq G_{CL}$$



Function of the Loop Gain, T



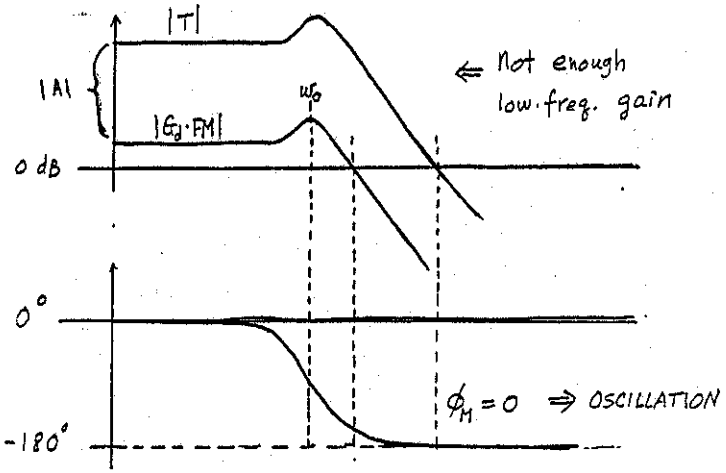
Compensator, A(s) Design Considerations

- to Shape the Loop Gain, T = G_d FM A(s)

Consider an ideal buck converter

$$G_d = \frac{G_m}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \qquad G_m = \frac{V_o}{D}, \quad \omega_o = \frac{1}{\sqrt{LC}}, \quad Q = R\sqrt{\frac{C}{L}}$$

• Suppose $A(s) = K$; constant gain



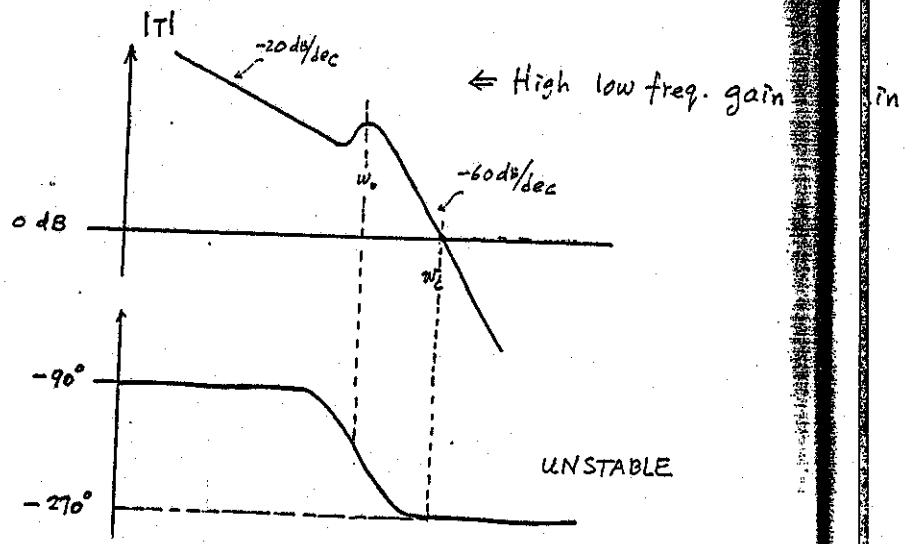
⇒ Need an integrator for a high gain at low freq.

Compensator, A(s) Design Considerations

- to Shape the Loop Gain, T = G_d FM A(s)

- Suppose $A(s) = \frac{\omega_I}{s}$; integrator

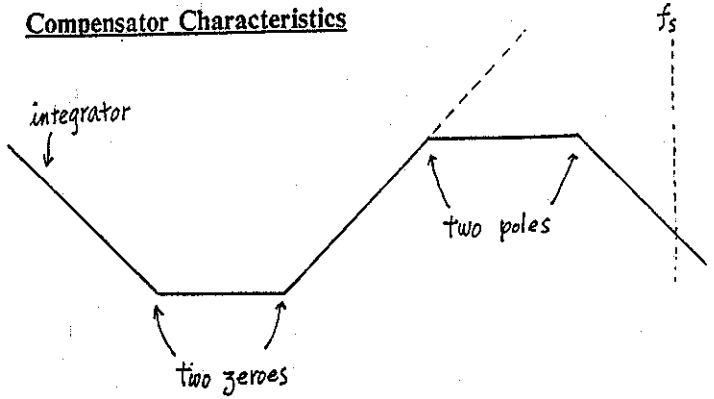
$$T = \frac{\omega_m}{s} \cdot \frac{1}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \qquad \omega_m = \omega_I \cdot G_{id} \cdot FM$$



⇐ High low freq. gain

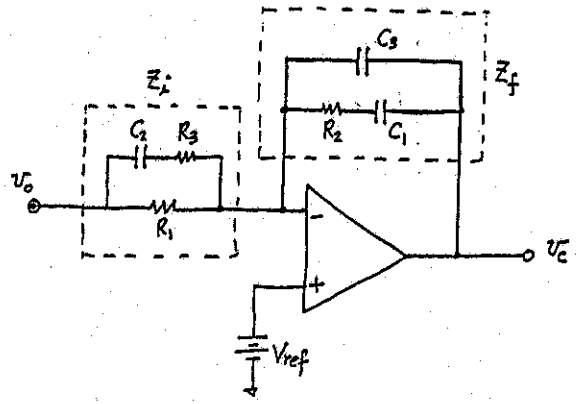
⇒ Exessive phase lag at the loop gain crossover, ω_c due to the integrator (-90°) and complex pole pair (-180°) need to be compensated by introducing two zeroes before ω_c

Compensator Characteristics



- An integrator for high dc gain
- Two zeroes below the loop gain crossover frequency, f_c to compensate the excessive phase lag due to the integrator and the power stage complex pole pair.
- Two high frequency poles
  - to attenuate high frequency noise
  - to ensure the magnitude of the loop gain keeps decreasing after the 0 dB crossover
  - * phase lag due to the two poles at the loop gain crossover should be minimum

Compensator Circuit



$$\frac{\hat{v}_c}{\hat{v}_o} = -\frac{Z_f}{Z_i}, \qquad Z_i = R_1 \,//\, \left(\frac{1}{sC_2} + R_3\right)$$

$$Z_f = \frac{1}{sC_3} \,//\, \left(\frac{1}{sC_1} + R_2\right)$$

$$= -\frac{\omega_I}{s} \frac{(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}$$

where

$$\omega_I = \frac{1}{R_1 (C_1 + C_3)},$$

$$\omega_{z1} = \frac{1}{R_2 C_1}, \qquad \omega_{z2} = \frac{1}{C_2 (R_1 + R_3)}$$

$$\omega_{p1} = \frac{1}{R_3 C_2}, \qquad \omega_{p2} = \frac{1}{R_2 \cdot \frac{C_1 C_3}{C_1 + C_3}}$$

Compensator Circuit

For $C_1 \gg C_3$, $R_1 \gg R_3$

$$\omega_I = \frac{1}{R_1 C_1}$$

$$\omega_{z1} = \frac{1}{R_2 C_1}, \qquad \omega_{z2} = \frac{1}{R_1 C_2}$$

$$\omega_{p1} = \frac{1}{R_3 C_2}, \qquad \omega_{p2} = \frac{1}{R_2 C_3}$$

Buck Regulator Design

Loop gain, $T = G_d \cdot FM \cdot A(s)$

$$G_d \triangleq \frac{\hat{v}_o}{\hat{d}} = V_g \cdot \frac{1 + s/\omega_z}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}$$

$$\omega_z = \frac{1}{R_c C}$$

$$\omega_o \approx \frac{1}{\sqrt{LC}} \qquad Q \approx R \cdot \sqrt{\frac{C}{L}}$$

$$G_v \triangleq \frac{\hat{v}_o}{\hat{v}_g} = D \cdot \frac{1 + s/\omega_z}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}$$

$$Z_p \triangleq \frac{\hat{v}_o}{\hat{i}_o} = R_l \| R \cdot \frac{(1 + s/\omega_z)(1 + s/\omega_{z1})}{1 + s/Q\omega_o + s^2/\omega_o^2}$$

$$\omega_{z1} = \frac{R_l}{L}$$

Loop Gain Design Procedure

$$T = \frac{\omega_M}{s} \cdot \frac{(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \cdot \frac{(1 + s/\omega_z)}{(1 + s/Q\omega_o + s^2/\omega_o^2)}$$

where $\omega_M = V_g \cdot FM \cdot \omega_I$

The objective is to design a compensator, ω_I, ω_{z1}, ω_{z2}, ω_{p1} and ω_{p2} to shape the loop gain, T for stability and optimum performance for given power stage parameters, ω_z, ω_o, Q and V_g, and the PWM gain, FM.

Design Steps

1. Set the loop gain crossover frequency, f_c for given switching frequency, f_s.
   i.e., $f_c = f_s / 6$:

2. Cancel the ESR zero, f_z, by a compensator pole, f_{p1}. ($f_{p1} = f_z$)

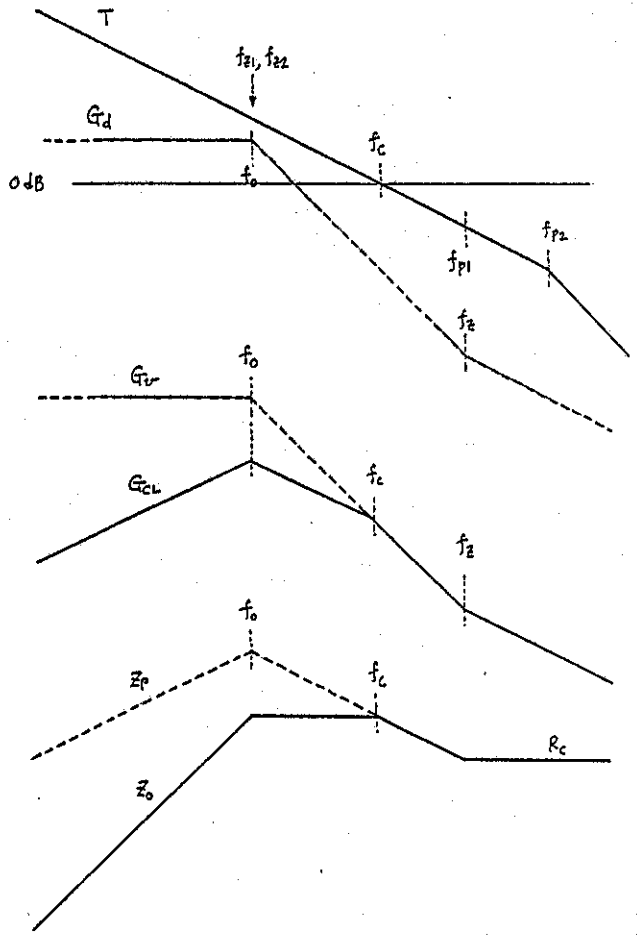
3. Place a high frequency compensator pole, f_{p2} to get the maximum attenuation of the switching ripple and high frequency noise with the minimum phase lag at f_c.

4. Place the two compensator zeroes, f_{z1} and f_{z2} below f_c.
   Place f_{z1} below the power stage resonant frequency, f_o to avoid a conditional stability.
   Design f_{z1} and f_{z2} considering the trade-off between the regulator performance and the stability margin.

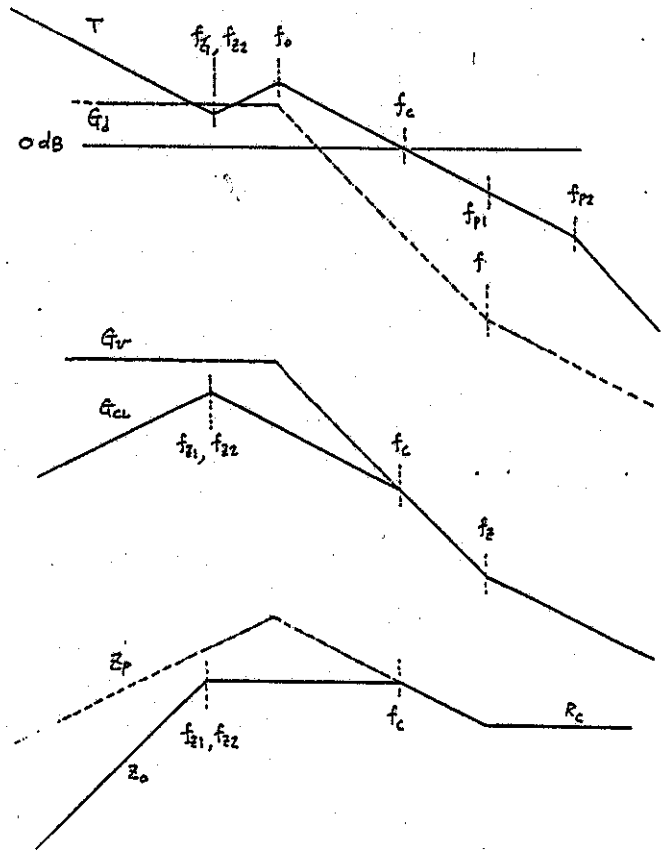
5. The integrator gain, f_i is determined after the the step 4

6. Select the compensator parameters. (R's and C's)

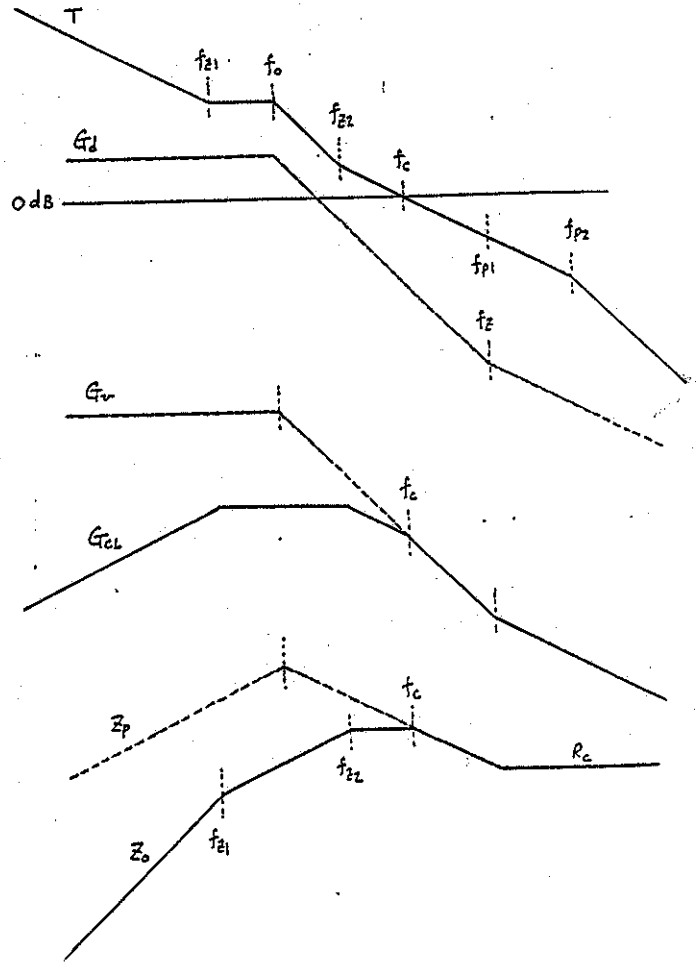
Design of f_{z1} and f_{z2} - Case 1



Design of f_{z1} and f_{z2} - Case 2



Design of f_{z1} and f_{z2} - Case 3



Settling Time for the Step Input / Load Transient

Closed-loop transfer function

$$G_{CL} = \frac{G_o}{1+T}$$

$$\approx \frac{G_o}{T} \quad \text{at low frequency} \quad (|T| \gg 1)$$

$$G_o = \frac{F_1(s)}{G(s)}$$

$$T = \frac{(1+s/\omega_z)}{G(s)} \cdot \frac{\omega_m}{s} \cdot \frac{(1+s/\omega_{z1})(1+s/\omega_{z2})}{(1+s/\omega_{p1})(1+s/\omega_{p2})}$$

$$\therefore G_{CL} = \frac{s/\omega_m \cdot F_1(s) \cdot (1+s/\omega_{p1})(1+s/\omega_{p2})}{(1+s/\omega_{z1})(1+s/\omega_{z2})(1+s/\omega_z)}$$

↑ ESR zero

The lower frequency compensator zero, f_{z1} determines the settling time.

Design Trade-Off for f_{z1} and f_{z2}

	freq.	closed-loop peak	Settling time	Stability margin
f_{z1}	↑	↓	faster	↓
	↓	↑	slower	↑
f_{z2}	↑	↓		↓
	↓	↑		↑

Flyback Regulator Design

$$G_d \triangleq \frac{\hat{v}_o}{\hat{d}} = \frac{N_s}{N_p} \cdot \frac{V_g}{D'^2} \cdot \frac{(1 - s/\omega_a)(1 + s/\omega_b)}{\left\| 1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2} \right\|}$$

$$\omega_o \cong \frac{D'}{\sqrt{LC}}, \quad Q \cong D'R \cdot \sqrt{\frac{C}{L}}$$

$$\omega_a \cong \frac{D'^2 R}{DL}, \quad \omega_b = \frac{1}{R_c C}$$

$$G_v \triangleq \frac{\hat{v}_o}{\hat{v}_g} = \frac{D}{D'} \frac{N_s}{N_p} \cdot \frac{1 + s/\omega_b}{\| \quad \|}$$

$$Z_p \triangleq \frac{\hat{v}_o}{\hat{i}_o} = \left(\frac{R_L}{D'^2}\right) \| R \cdot \frac{(1 + s/\omega_b)(1 + s/\omega_c)}{\| \quad \|}$$

$$\omega_c = \frac{R_L}{L}$$

Loop Gain Design

- Due to the RHP zero, f_z the loop gain crossover frequency, f_c must be designed well below the RHP zero.

  i.e., $f_c = f_z / 10$

- The two poles in the compensator should cancel both ESR zero, f_b and RHP zero, f_z

- Design of the two zeroes are the same as in the buck regulator case.