

Part II

Impedance Interactions in DC

Distributed Power Systems

by

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Chapter 5

Impedance Interactions: An Overview

5.1 Introduction

In this chapter, interconnections among DC power distribution subsystems are analyzed, and an investigation is launched into how the performance of the global interconnection differs from that predicted by the analysis of each independent subsystem. Typical examples of these interconnections are a power converter with a dynamic load, a power converter with an input line filter, power converters connected in parallel or cascade, and combinations of the above.

Most of the literature on the subject is focused on the problem of a power con-

verter in the presence of an input filter, but more recently the same ideas are being applied in the context of DC Distributed Power Systems (DPS). Every interface in any interconnection of power converters, filters and/or loads is subject to impedance interactions. This is the case of DPS, in particular the Intermediate Bus Architecture (IBA) in which an off-line converter provides a mildly regulated DC line that is distributed among subsystems, with Point-Of-Load (POL) converters providing voltage regulation in close proximity to the loads. Typical applications for this architecture are communications systems, data centers, motherboards, and even on-chip power distribution networks.

A typical diagram for a DPS is shown in Fig. 5.1. One or more AC/DC converters with Power Factor Correction provide an intermediate DC voltage from the same or potentially different AC sources. A battery can be present for power backup. Many POL converters with their respective EMI filters feed independent or shared loads. Some loads could even be connected to the intermediate bus directly. In this diagram, it can be appreciated that interfaces marked as A, B, and C are prone to impedance interactions and potential performance degradation.

The state of the art is such that it is very simple to check the overall performance and stability of an already engineered system by simulation or experimentation. This is usually a system integrator's job. If a problem is encountered, there is little possibility of modifying the internal dynamics of the converters. As a consequence, the most

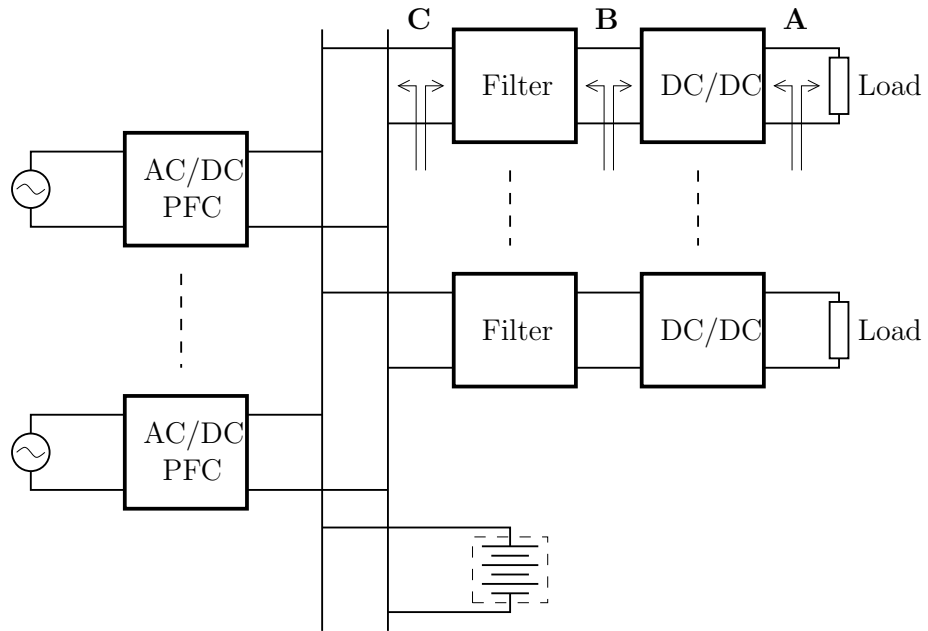


Figure 5.1: Typical DPS diagram.

likely outcome of this process is that the filters become oversized, by the addition of capacitors, inductors, damping, or some combination of these.

A literature review as well as an exposition of the most important aspects of this subject are presented first in this chapter. In the following chapter, a contribution to the understanding of this problem using fundamentals of control systems theory is developed and the feasibility of reducing impedance interactions by control methods instead of physical design is explored.

5.2 Literature review

It was observed early in the development of the discipline of Power Electronics that certain power converters showed unstable behavior in the presence of an input filter [30]. This problem was analyzed using newly derived averaged models in the mid-seventies [31]. A theoretical understanding of the phenomenon was consolidated and design guidelines were derived in order to guarantee the eradication of the problem in voltage programmed regulators [32]. This contribution is usually referred to as the “Middlebrook criterion”. Results were extended for current programmed regulators in [33].

The solution proposed was based on adding damping to the input filter. Optimization procedures were derived in order to minimize the size of the filter, the power dissipation, or some other quantity of interest while still achieving the desired damping [34, 35].

In the eighties an input voltage feedforward scheme was proposed in order to mitigate the effects of the input filter [36, 37]. This method is based on a zero-pole cancellation that is difficult to achieve in practice, even using adaptive methods [38]. This was, however, the first attempt to solve the problem using control methods instead of modifying the physical design of the filter.

A practical overview of the problem of impedance interactions in the context of input filter interactions, with a timeline of key papers can be found in [39].

As scaling in IC technology increased density and speed, DPS were proposed to meet the new power demands [10]. This created new topologies of interconnected power converters and line filters in which impedance interactions at every interface could potentially degrade the performance of the system. Analysis methods were extended and new design guidelines developed for this type of system [40–44].

Recent efforts have been made to measure the impedances online for the sake of analyzing stability and performance degradation due to the interconnection of power modules [45, 46]. These methods allow users to analyze the systems and subsystems without knowledge of internal components.

It has been observed that a power converter is immune to impedance interactions at its input and output ports if it has both an output impedance and a forward-voltage transfer function equal to zero [47]. These conditions are not possible to achieve in practice. A system-level approach has to be undertaken to guarantee an overall stability and performance objective.

5.3 Problem description

Traditionally, a power converter is designed under the assumption that there exists an ideal voltage source at the input, as shown in Fig. 5.2. In this case, it is clear that variations in the input current I_{in} (due to, for example, load variations) will not affect the input voltage V_{in} . It can be said that the input and the output of the converter

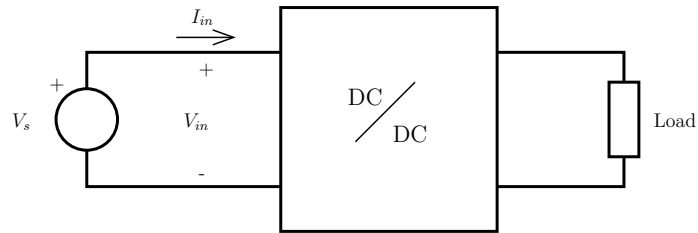


Figure 5.2: DC/DC converter without an input filter.

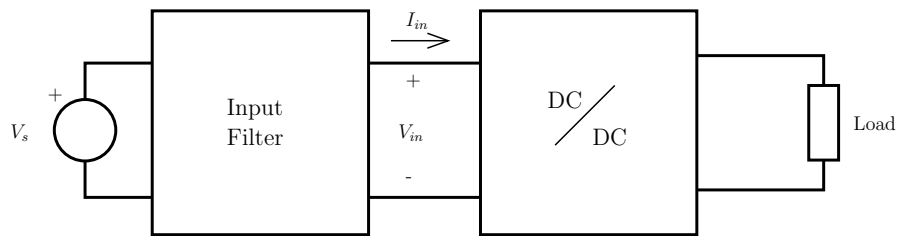


Figure 5.3: DC/DC converter with an input filter.

are “decoupled”.

Now consider the system in Fig. 5.3, in which an input filter is added. This input filter can be an EMI filter or the output impedance of another power converter. When I_{in} changes, a perturbation in the input voltage V_{in} will occur due to the output impedance of the input filter. This creates a new feedback loop that can affect significantly the dynamics of the converter, in some cases degrading its performance or even resulting in instability.

The interaction between the impedances can be analyzed by using as an illustrative example the model shown in Fig. 5.4, where Z_o is the output impedance of the input filter, and Z_i is the input impedance of the power converter. The effect of a

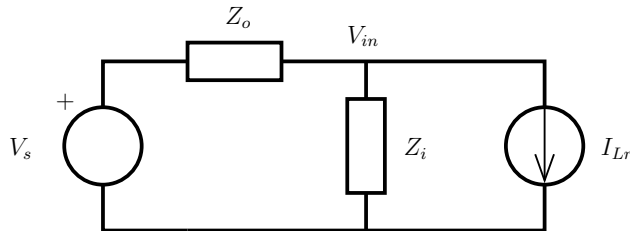


Figure 5.4: Equivalent circuit of a power converter connected to an input filter.

perturbation in the input voltage V_{in} as a function of a change in the load current (reflected to the input of the converter) I_{Lr} is

$$\frac{V_{in}}{I_{Lr}} = -(Z_o \parallel Z_i) \quad (5.1)$$

$$= -\frac{Z_o}{1 + Z_o Y_i}, \quad (5.2)$$

where $Y_i = \frac{1}{Z_i}$ is the input admittance. This means that a new feedback loop, sometimes called the “small loop”, is established. The stability of this loop can be analyzed by applying the Nyquist criterion to $Z_o Y_i$.

In general, the feedback loop created by the connection of two n -ports systems can be analyzed as a MIMO dynamic feedback system. This interpretation is presented in [48] in the context of the small gain theorem, which gives a sufficient condition for the stability of the feedback system. Necessary and sufficient stability conditions for dynamic feedback systems are given in [49]. In the special case of the interconnection of two one-ports which are stable, the feedback system is stable if and only if the zeros of $1 + Z_1 Y_2$ have negative (or zero) real part, where Z_1 and Y_2 are the impedance and

admittance of the two one-ports respectively.

In conclusion, the Nyquist criterion applied to $Z_o Y_i$ as in (5.2) is a necessary and sufficient condition for stability of the interconnection of stable one-ports. This is a very useful result because in practice most of the circuits interconnected in a DPS are stable.

Stability of the interconnection is critical, but from an engineering perspective performance should also be analyzed. Even if the loop is stable, it can still affect significantly the dynamics of the power converter and degrade its performance. The analytical tools for analyzing the performance will be given in the next section.

Example: Buck converter with LC input filter

The ideas exposed above are illustrated here with a simple but important example. Assume a buck converter is controlled such that the output power is constant. This could be the case, for example, if the load is resistive and the converter regulates the output voltage. The closed-loop input impedance over the controller bandwidth is then computed as follows. First, the input power is expressed as a function of the output power and the efficiency:

$$V_{in} I_{in} = \frac{V_o I_o}{\eta}. \quad (5.3)$$

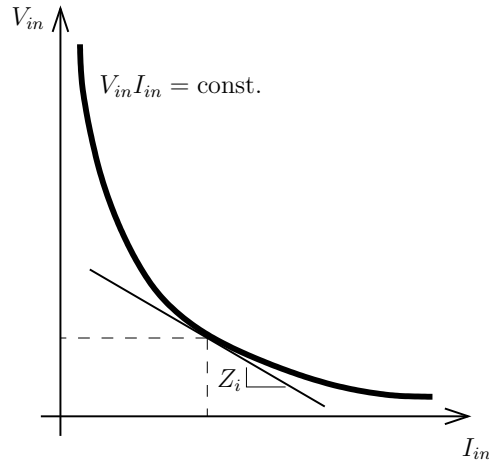


Figure 5.5: Negative input impedance of a constant-power converter.

Then, the small-signal input impedance is computed as the partial derivative of the input voltage with respect to the input current:

$$V_{in} = \frac{V_o I_o}{\eta I_{in}} \quad (5.4)$$

$$\Rightarrow \frac{\partial V_{in}}{\partial I_{in}} = -\frac{V_o I_o}{\eta I_{in}^2}. \quad (5.5)$$

Finally, by substituting $I_{in} = D I_o$ (buck converter) and $\frac{V_o}{I_o} = R_L$ (resistive load), the following result is obtained:

$$Z_i = -\frac{R_L}{\eta D^2}. \quad (5.6)$$

This negative input impedance can be seen graphically in Fig. 5.5 as the slope of the (V_{in}, I_{in}) curve. The impedance depends on the operating point.

Now assume the converter is connected with an LC input filter like the one depicted

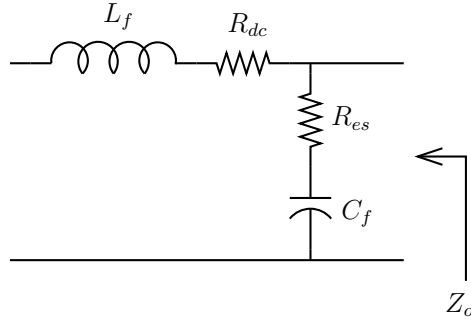


Figure 5.6: Input filter.

in Fig. 5.6. The output impedance of this filter is

$$Z_o = \frac{(L_f s + R_{dc})(R_{es} C_f + 1)}{L_f C_f s^2 + (R_{dc} + R_{es}) C_f s + 1}. \quad (5.7)$$

The stability of the system can be analyzed by computing explicitly the transfer function (5.2). For simplicity of notation, η is assumed to be equal to unity. Then

$$\frac{V_{in}}{I_{Lr}} = -\frac{Z_o}{1 + Z_o Y_i} \quad (5.8)$$

$$= \frac{-(L_f s + R_{dc})(R_{es} C_f s + 1)}{\left(1 - \frac{D^2 R_{es}}{R_L}\right) L_f C_f s^2 + \left[\left(R_{dc} + R_{es} - \frac{D^2 R_{es} R_{dc}}{R_L}\right) C_f - \frac{D^2 L_f}{R_L}\right] s + 1 - \frac{D^2 R_{dc}}{R_L}} \quad (5.9)$$

Applying the Routh-Hurwitz criterion to the denominator of this expression, a stability condition can be derived. Usually $\left(1 - D^2 \frac{R_{es}}{R_L}\right)$ and $\left(1 - D^2 \frac{R_{dc}}{R_L}\right)$ are positive.

Assuming the latter, the stability condition can be written as

$$\left(R_{dc} + R_{es} - D^2 \frac{R_{es} R_{dc}}{R_L}\right) C_f - D^2 \frac{L_f}{R_L} > 0 \quad (5.10)$$

$$\Leftrightarrow \frac{R_L}{D^2} > (R_{es} \parallel R_{dc}) + \frac{Z_C^2}{R_{es} + R_{dc}} \approx Q Z_C \quad (5.11)$$

where $Z_C^2 = \frac{L_f}{C_f}$ and $Q \approx \frac{Z_C}{R_{es} + R_{dc}}$. This is equivalent to say that the magnitude of

the input impedance of the converter has to be larger than the peak of the output impedance of the LC filter at the resonance frequency. This is consistent with the Nyquist criterion, because at that frequency the term $Z_o Y_i$ has an angle of 180° and needs to have a magnitude less than unity in order not to encircle the $(-1,0)$ point.

This example is valid as long as the controller bandwidth of the converter is high enough such that the constant-power assumption holds for the resonant frequency of the LC filter. More exact, but also more complicated results can be obtained by computing the closed-loop input impedance of the converter based on a small-signal model.

5.4 Middlebrook criterion

The Middlebrook criterion is a sufficient condition for guaranteeing the stability of two interconnected systems. Moreover, the criterion also guarantees that no performance degradation occurs due to the interconnection. Following this criterion, the designer can effectively “decouple” one module from its source or load impedance.

The derivation of the criterion can be better understood by applying the Extra Element Theorem (EET) [50]. The EET is used when a transfer function for a system is known and an additional element is connected to one port of the system, modifying the original transfer function. The setup is shown in Fig. 5.7. Suppose the transfer function $T_{u \rightarrow y}$ is known when there is no impedance Z connected to the port in system

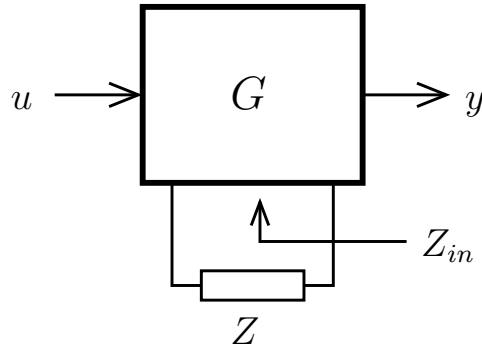


Figure 5.7: The Extra Element Theorem.

G (either $Z = \infty$ or $Z = 0$). When the impedance is connected, this will naturally affect the transfer function. The EET postulates that the new transfer function will be:

$$T_{u \rightarrow y}|_Z = T_{u \rightarrow y}|_{Z=\infty} \frac{1 + \frac{Z_n}{Z}}{1 + \frac{Z_d}{Z}} \quad (5.12)$$

$$= T_{u \rightarrow y}|_{Z=0} \frac{1 + \frac{Z}{Z_n}}{1 + \frac{Z}{Z_d}} \quad (5.13)$$

$$\text{where } Z_n = Z_{in}|_{y \rightarrow 0} \quad (5.14)$$

$$\text{and } Z_d = Z_{in}|_{u=0} \quad (5.15)$$

The two new quantities that need to be computed are the input impedance of the port under special circumstances. For computing Z_n the input variable u has to be set such that the output variable y vanishes (notice that this is not the same as shorting the output). For computing Z_d the input variable u has to be set to zero.

In the case of a converter with an input filter, the port would be the input port of

the converter and the impedance to add would be the output impedance of the input filter Z_o . Since this impedance is usually assumed to be zero, the effect of a non-zero impedance can be analyzed by using form (5.13) of the EET. The transfer functions of interest would usually be the output impedance of the converter, the duty-cycle to output voltage, or the audio susceptibility transfer functions. The duty-cycle to output voltage transfer function $T_{d \rightarrow v_o}$ will be analyzed next as an example.

To compute Z_n the duty cycle has to be set such that the (small signal) output voltage vanishes. This is usually the control objective (voltage regulation), so it can be concluded that Z_n is the ideal closed-loop input impedance of the converter Z_i^{CL} (ideal in the sense that would achieve perfect regulation over all frequencies). To compute Z_d the duty cycle has to be set to zero, which means that the converter operates in open loop. Therefore, Z_d is the open-loop input impedance of the converter Z_i^{OL} . By substituting into (5.13) the following result is obtained:

$$T_{d \rightarrow v_o}|_{Z_o} = T_{d \rightarrow v_o}|_{Z_o=0} \frac{1 + \frac{Z_o}{Z_i^{CL}}}{1 + \frac{Z_o}{Z_i^{OL}}} \quad (5.16)$$

This result is exact and predicts the effect of the input filter in the dynamics of the converter. Based on this result, Middlebrook established the simple, although conservative, design rule that is today known as the Middlebrook criterion and can be stated as follows:

“The dynamics of the converter will not be significantly affected by an input filter if $|Z_o| \ll |Z_i^{CL}|$ and $|Z_o| \ll |Z_i^{OL}|$.”

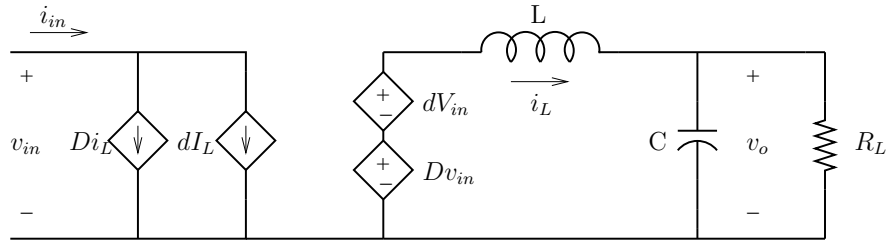


Figure 5.8: Small-signal model of a buck converter with resistive load.

This criterion can be immediately understood by looking at (5.16): the conditions imply that the multiplying term that affects the transfer function is close to unity. If the dynamics are not affected, then clearly stability and performance of the converter are preserved. It is also evident that the criterion is a sufficient condition that can potentially be very conservative.

Example: Applying the EET to a buck converter with input filter

In the case of a buck converter, whose small-signal model is shown in Fig. 5.8, the duty-cycle to output voltage transfer function is:

$$T_{d \rightarrow v_o} = \left. \frac{v_o}{d} \right|_{v_{in}=0} = V_{in} \cdot \frac{1}{LCs^2 + \frac{L}{R_L}s + 1}. \quad (5.17)$$

In order to apply the EET, it is necessary to compute the open-loop and ideal closed-loop input impedances. The former is:

$$Z_i^{OL} = \left. \frac{v_{in}}{\dot{i}_{in}} \right|_{d=0} = \frac{R_L}{D^2} \cdot \frac{LCs^2 + \frac{L}{R_L}s + 1}{R_LCs + 1}, \quad (5.18)$$

while the latter needs to be computed by setting the duty-cycle such that it cancels the output voltage, namely $d = -\frac{D}{V_{in}}v_{in}$. Then

$$Z_i^{CL} = \left. \frac{v_{in}}{i_{in}} \right|_{d=-\frac{D}{V_{in}}v_{in}} = -\frac{R_L}{D^2}. \quad (5.19)$$

Finally, we can apply the EET as stated in (5.13) to obtain the duty-cycle to output voltage transfer function when we connect the input filter of Fig. 5.6:

$$T_{d \rightarrow v_o} = V_{in} \cdot \frac{1}{LCs^2 + \frac{L}{R_L}s + 1} \cdot \frac{1 - \frac{D^2}{R_L} \cdot \frac{(L_f s + R_{dc})(R_{es}C_f + 1)}{L_f C_f s^2 + (R_{dc} + R_{es})C_f s + 1}}{1 + \frac{D^2}{R_L} \cdot \frac{R_L C_s + 1}{LCs^2 + \frac{L}{R_L}s + 1} \cdot \frac{(L_f s + R_{dc})(R_{es}C_f + 1)}{L_f C_f s^2 + (R_{dc} + R_{es})C_f s + 1}}. \quad (5.20)$$

After some algebra the expression can be reduced to

$$T_{d \rightarrow v_o} = V_{in} \cdot \frac{N(s)}{D(s)} \quad (5.21)$$

where

$$N(s) = \left(1 - D^2 \frac{R_{es}}{R_L}\right) L_f C_f s^2 + \left[\left(R_{dc} + R_{es} - D^2 \frac{R_{es} R_{dc}}{R_L} \right) C_f - D^2 \frac{L_f}{R_L} \right] s + 1 - D^2 \frac{R_{dc}}{R_L} \quad (5.22)$$

and

$$\begin{aligned} D(s) = & L_f C_f L C s^4 + \\ & \left[L_f C_f \left(\frac{L}{R_L} + D^2 R_{es} C \right) + (R_{dc} + R_{es}) C_f L C \right] s^3 + \\ & \left[L_f C_f \left(1 + D^2 \frac{R_{es}}{R_L} \right) + L C + L C_f \frac{R_{dc} + R_{es}}{R_L} + D^2 L_f C + D^2 R_{dc} R_{es} C C_f \right] s^2 + \\ & \left[\left(R_{es} + R_{dc} + D^2 \frac{R_{dc} R_{es}}{R_L} \right) C_f + \frac{L + D^2 L_f}{R_L} + D^2 R_{dc} C \right] s + \\ & 1 + D^2 \frac{R_{dc}}{R_L}. \end{aligned} \quad (5.23)$$

Although the denominator of the expression does not add much insight into the problem, the numerator shows an interesting fact. Comparing (5.22) with the denominator in (5.9), it can be concluded that the zeros of the duty-cycle to output voltage transfer function are equal to the poles of the closed-loop transfer function computed in the previous section under the assumption of perfect regulation. This is consistent with control theory results, namely that under the condition of infinite feedback gain the poles of the closed-loop transfer function are equal to the zeros of the plant. More importantly, this example shows that instability of the closed-loop system is related to the existence of right half-plane zeros in the plant, and that those zeros are introduced by the input filter.

An illustration of the effect of an input filter in the dynamics of a buck converter is shown in Fig. 5.9. The top two graphs show the bode plots in the case of a damped input filter. Since $|Z| \ll |Z_n|, |Z_d|$ (i.e., the Middlebrook criterion is satisfied) the plant transfer function $T_{d \rightarrow v_o}$ presents its characteristic second-order shape, unaffected by the input filter. The bottom two graphs show the case of an undamped (or lightly damped) input filter. The plant transfer function shows the effect of the input filter resonance, leading potentially to a degradation of performance and even instability.

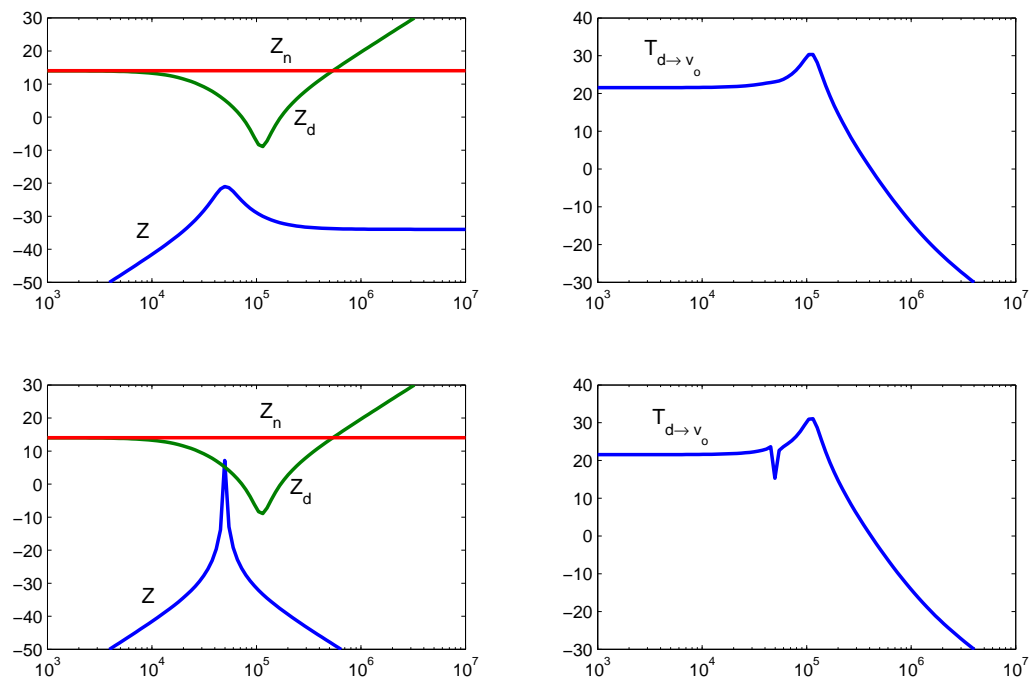


Figure 5.9: Effect of input filter in buck converter dynamics. Top: Damped input filter. Bottom: Undamped input filter.

5.5 Modeling

When designing the control system of a power converter, it is standard practice to derive a small-signal model and from there extract the transfer functions of interest, for example the duty-cycle to output voltage transfer function, duty-cycle to inductor current transfer function, output impedance, etc. If the converter is connected to a source or load impedance these transfer functions are not valid any longer, as explained in the previous sections. There are many ways to deal with this:

1. Assume the Middlebrook criterion is valid and ignore impedance interactions.
2. Derive the new transfer functions using the extra-element theorem (EET).
3. Include the impedance in the small-signal model and derive the transfer functions for the new model.

In the design process, the first option is probably the only feasible one, since the complexity of the other approaches is too high for a designer. However, if the purpose is to simulate and validate a controller design, there is no need to recompute the transfer functions. A two-port model of the converter, based on the small-signal model, can be derived and connected to the impedance for simulation.

Any type of two-port model would work, however the nature of DC/DC power converters is such that in closed loop it is more useful to see the input voltage and output current as independent variables (“inputs” to the system), while the input

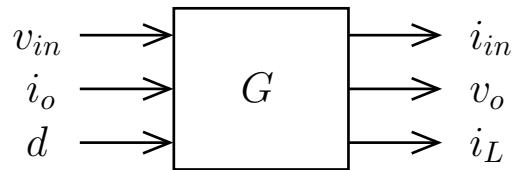


Figure 5.10: DC/DC converter model.

current and output voltage are dependent variables (“outputs” of the system). This leads naturally to a hybrid parameter model. In two-port models in which one of the ports can be naturally identified as “input” and the other as “output”, some authors make the distinction between the two possible types of hybrid models that can arise. Following this convention, the so-called inverse-hybrid parameter, or G-parameter model was proposed [51, 52]. A derivation of this type of two-port model is shown next.

Suppose the converter has a small-signal (linear), multivariable model G depicted in Fig. 5.10. The inputs are the input voltage v_{in} , the output or load current i_o , and the duty-cycle d . The outputs are the input current i_{in} , the output voltage v_o , and the inductor current i_L . (The latter is useful in the context of current-mode control, otherwise it could be obviated.)

This system can be completely described by the following set of equations:

$$\begin{cases} i_{in} = G_{iv}v_{in} + G_{ii}i_o + G_{id}d \\ v_o = G_{vv}v_{in} + G_{vi}i_o + G_{vd}d \\ i_L = G_{Lv}v_{in} + G_{Li}i_o + G_{Ld}d \end{cases} \quad (5.24)$$

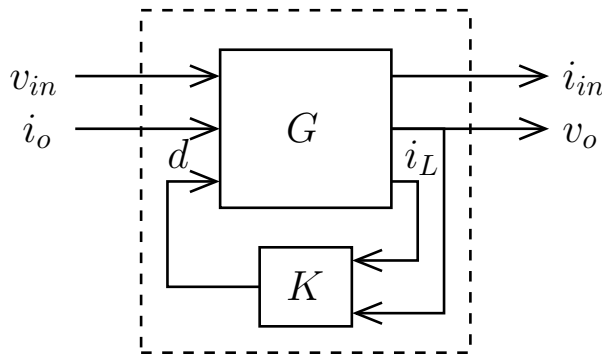


Figure 5.11: DC/DC converter model with feedback controller K .

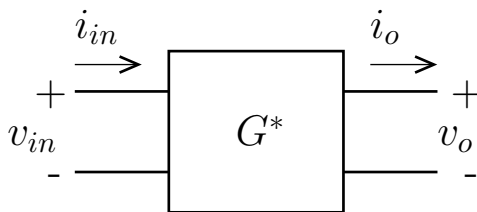


Figure 5.12: Two-port model of a closed-loop DC/DC converter.

When a feedback controller K is connected (Fig. 5.11), the closed-loop converter becomes a two-input, two-output system that can be represented as a two-port system (Fig. 5.12). Here the system G^* represents the closed-loop converter. The system can be described by the following set of equations:

$$\begin{cases} i_{in} = G_{iv}^* v_{in} + G_{ii}^* i_o \\ v_o = G_{vv}^* v_{in} + G_{vi}^* i_o \end{cases} \quad (5.25)$$

For simulation purposes, however, the transfer functions of the closed-loop description do not need to be computed. An internal description like the one inside the dashed box in Fig. 5.11 can be used. A less compact, but more realistic circuit

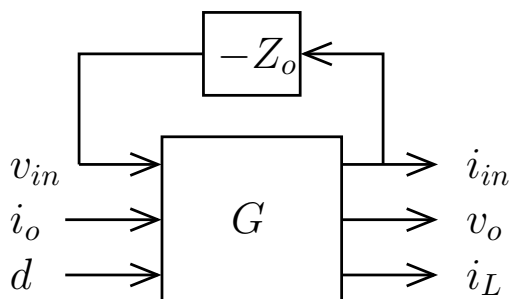


Figure 5.13: DC/DC converter with input filter. Multivariable model case.

description, like the one in Fig. 5.8 can also be used, although in some systems it could consume more computational resources.

The advantage of two-port models arises when subsystems need to be interconnected, in particular when there are many subsystems in series or parallel. For example, consider a converter with an input filter. In the multivariable model of Fig. 5.10, the filter could be accommodated by including a feedback loop with the output impedance of the filter Z_o , as depicted in Fig. 5.13. It is assumed that the only small-signal perturbation at the input of the converter is due to perturbations in the input current, interacting with the output impedance of the filter.

Now, suppose the input filter is connected to the output of another converter, for example an AC/DC converter. To include the effect of this cascaded interconnection, it would be required to compute the output impedance of the filter under the presence of the AC/DC converter, and then to substitute this value instead of Z_o in the figure. For every additional subsystem interconnected to the network, all impedances need

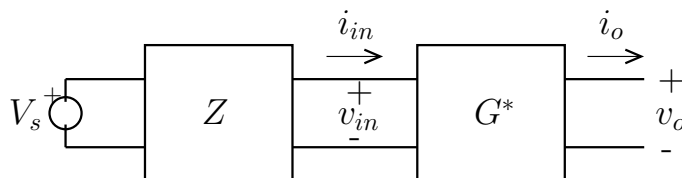


Figure 5.14: DC/DC converter with input filter. Two-port model case.

to be recomputed.

Compare this scenario with the two-port model case. The input filter can be included using its own two-port model Z as shown in Fig. 5.14, and its input port connected to a DC voltage source V_s , or equivalently a short circuit.

If a new converter is connected to the input of the filter, the voltage source can be replaced by the output port of this new converter and no modifications are needed to the filter model. No matter how complex the interconnections, the two-port model allows for a topological connection that is identical to the circuit without needing to recompute any of the models. Hence, it can be concluded that two-port models are more convenient than multivariable models for simulation and verification of interconnected systems.

It should be noted, though, that the small-signal model described so far depends on the (large-signal) operating point of the converter. Therefore, when the converter is connected to a load or a source impedance that changes the operating point, the converter model needs to be recomputed. The general form of the equations, though, does not change because only the values of some parameters are modified.

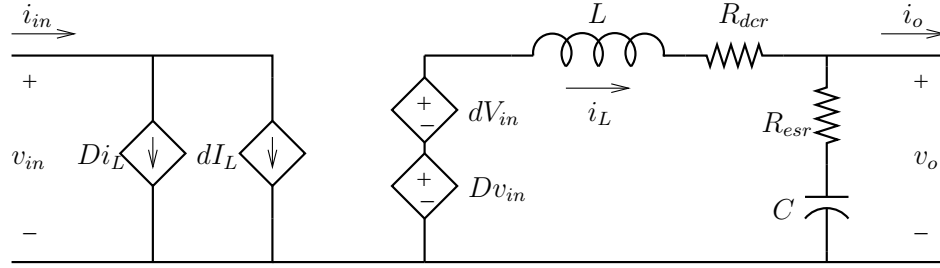


Figure 5.15: Small-signal model of buck converter with parasitic resistances.

Example: Two-port model of a buck converter

In the case of a buck converter, the traditional averaged small-signal model as shown in Fig. 5.8 (without the load resistance R_L) is simple enough to be used in simulations as a two-port model. The canonical G-parameter model is derived here for completeness. The parasitic resistances of the inductor and the switches (R_{dcr}), and the capacitor (R_{esr}) are also included in the derivation. The small-signal model of reference is shown in Fig. 5.15.

There are nine transfer functions to be derived in accordance with (5.24). These are:

$$G_{iv} = \left. \frac{i_{in}}{v_{in}} \right|_{d=i_o=0} = D^2 \cdot \frac{Cs}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.26)$$

$$G_{ii} = \left. \frac{i_{in}}{i_o} \right|_{v_{in}=d=0} = D \cdot \frac{R_{esr}Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.27)$$

$$G_{id} = \left. \frac{i_{in}}{d} \right|_{v_{in}=i_o=0} = I_o \cdot \frac{LCs^2 + (R_{dcr} + R_{esr} + \frac{V_o}{I_o})Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.28)$$

$$G_{vv} = \left. \frac{v_o}{v_{in}} \right|_{d=i_o=0} = D \cdot \frac{R_{esr}Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.29)$$

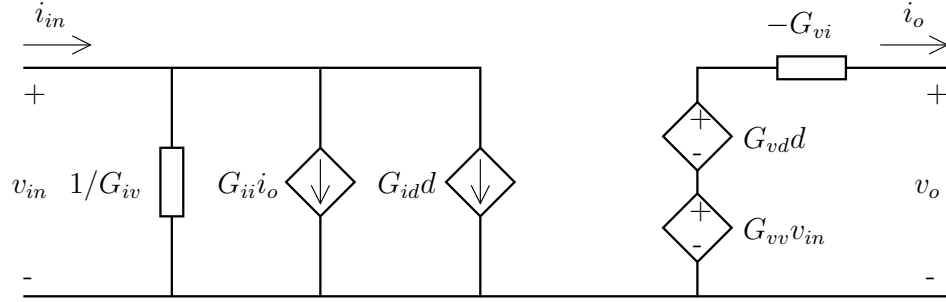


Figure 5.16: Implementation of the G-parameter two-port model. Open-loop case.

$$G_{vi} = \left. \frac{v_o}{i_o} \right|_{v_{in}=d=0} = \frac{(Ls + R_{dcr})(R_{esr}Cs + 1)}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.30)$$

$$G_{vd} = \left. \frac{v_o}{d} \right|_{v_{in}=i_o=0} = V_{in} \cdot \frac{R_{esr}Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.31)$$

$$G_{Lv} = \left. \frac{i_L}{v_{in}} \right|_{d=i_o=0} = D \cdot \frac{Cs}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.32)$$

$$G_{Li} = \left. \frac{i_L}{i_o} \right|_{v_{in}=d=0} = \frac{R_{esr}Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.33)$$

$$G_{Ld} = \left. \frac{i_L}{d} \right|_{v_{in}=i_o=0} = V_{in} \cdot \frac{Cs}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \quad (5.34)$$

The circuit representation of this model is shown in Fig. 5.16. The feedback loop can be incorporated with an additional circuit that generates the duty-cycle d . If current-mode control is used, the current i_L can be generated using (5.32–5.34).

This example shows a method to derive a canonical two-port model for a DC/DC converter. In closed-loop operation, a canonical model can also be obtained by trivial (although complicated) algebraic manipulations. In practice, the model could also be extracted from measurements. This means that a canonical model for a converter operating in closed-loop can be obtained from measurements even when the internal

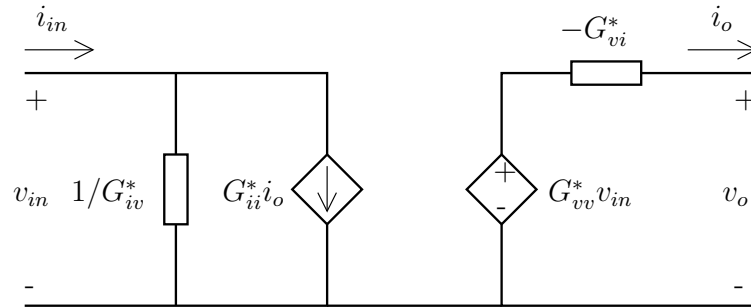


Figure 5.17: Implementation of the G-parameter two-port model. Closed-loop case.

characteristics are unknown (“black box”). The transfer functions to be obtained, according to (5.25) are only four, namely:

$$G_{iv}^* = \left. \frac{i_{in}}{v_{in}} \right|_{i_o=0} \quad (\text{input admittance}) \quad (5.35)$$

$$G_{ii}^* = \left. \frac{i_{in}}{i_o} \right|_{v_{in}=0} \quad (\text{inverse current gain}) \quad (5.36)$$

$$G_{vv}^* = \left. \frac{v_o}{v_{in}} \right|_{i_o=0} \quad (\text{voltage gain}) \quad (5.37)$$

$$G_{vi}^* = \left. \frac{v_o}{i_o} \right|_{v_{in}=0} \quad (\text{output impedance}) \quad (5.38)$$

The equivalent circuit is shown in Fig. 5.17. A system integrator could benefit from this approach when all or most of the subsystems in a DPS are modules whose internal behavior is unknown. Each one of them can be characterized by measuring these four transfer functions and the overall performance of the system can be predicted by simulation.

5.6 Conclusions

In this chapter, the problem of impedance interactions between interconnected power converters and/or passive circuits was presented. The basic results in this area were described, as well as the context in which the results were developed. A buck converter with an input filter was used as a representative example to illustrate the main ideas.

The next chapter will address this problem from a different perspective, exploring the fundamental issues that arise in this area and the feasibility of using control methods to preserve performance and stability of interconnected systems.

Chapter 6

Mitigation of Impedance

Interactions

In this chapter, the possibility of improving the performance of interconnected power converters and/or filters by using control methods instead of physical design is explored. First, some fundamental limitations are exposed. Different controller design methods are explored and compared. Finally, an example of the use of system-level design to mitigate impedance interactions is presented.

6.1 Limits of performance

It has been observed that an undamped input filter adds a pair of complex-conjugate right-half plane zeros to the duty-cycle to output transfer function of the

converter [35]. This observation is in accordance with the example shown in Section 5.4.

A RHP zero in the feedback loop is known to impose serious limits in the achievable performance of the closed-loop control system [53]. In general, the loop bandwidth should be less than half the frequency of the zero in order to preserve stability.

In many applications, the resonant frequency of the input filter is less than the resonant frequency of the output filter, which in turn is less than the desired bandwidth. As a consequence, the RHP zeros introduced by the input filter will invariably cause instability in closed-loop operation. It can be concluded that, under the presence of the RHP zeros, the performance requirements of the application (expressed, for example, as a high loop gain over the desired bandwidth) are not compatible with stable operation. It is for this reason that the most common solution to the problem is the addition of damping to the input filter, which moves the zeros from the RHP to the LHP.

When considering a power converter with an input filter, the converter's input voltage changes with its input current as described in the previous chapter. This voltage could be used as a controller input. In this case the controller would have two inputs (output voltage and input voltage) and one output (duty-cycle). In a MIMO system like this, the role of zeros is not as straightforward as in the SISO case because there is a spatial direction added to the frequency dimension. In particular, the limits

of performance imposed by RHP zeros are more difficult to analyze [54].

Therefore, the RHP zeros in traditional output voltage feedback control impose a fundamental limitation in the performance of the system, but more caution should be taken when discussing control with input voltage feedforward. In this chapter, although no definitive answer is attempted in this regard, an exploration of a large set of controllers with input voltage feedforward seems to indicate that the same limits of performance for SISO systems are valid in the MIMO case for this application.

6.2 Robust design of controllers

In this section, a robust design procedure is introduced in order to explore possible control schemes that could meet the performance and stability requirements of a representative VRM application under the presence of an input filter. It is shown that there is no stabilizing controller that can achieve high loop gain at the resonant frequency of the input filter.

The section is organized as follows. First, a model of the plant (a buck converter with an input filter) is presented in Section 6.2.1. The model includes uncertainty in the characteristics of the input filter. In Section 6.2.2, the plant is analyzed using the Middlebrook criterion (introduced in Section 5.4), revealing that for some parameter values the criterion is not satisfied and RHP zeros are introduced. A traditional PID control design is presented in Section 6.2.3 and its stability is analyzed. In

Section 6.2.4 input voltage feedforward is introduced, showing stable operation with nominal parameters but instability for some parameter values. A μ -synthesis design is presented in Section 6.2.5 that aims to find a controller that could achieve both stability and good performance under the presence of uncertain parameters in the input filter. Finally, in Section 6.2.6, conclusions are presented.

6.2.1 The plant

A diagram of the control system of a DC/DC converter using voltage mode control is shown in Fig. 6.1. The box labeled G represents the dynamics of the converter. The small-signal input voltage is generated by the presence of an input filter of output impedance Z_o . Adaptive Voltage Positioning (AVP) is achieved by subtracting the reference impedance Z_{ref} times the output current i_o from the reference voltage v_r . As an example, the generalized output impedance approach as defined in [9] is used, meaning that

$$Z_{ref} = R_{LL} \cdot \frac{R_{est}Cs + 1}{R_{LL}Cs + 1} \quad (6.1)$$

The box labeled K corresponds to the controller that generates the duty-cycle command d based on the error voltage v_e . An input voltage feedforward path is included also in order to explore a richer set of controllers.

The converter's model can be obtained based on (5.26–5.31). However, in this chapter a resistive load R_L is also included in order to explore different operating

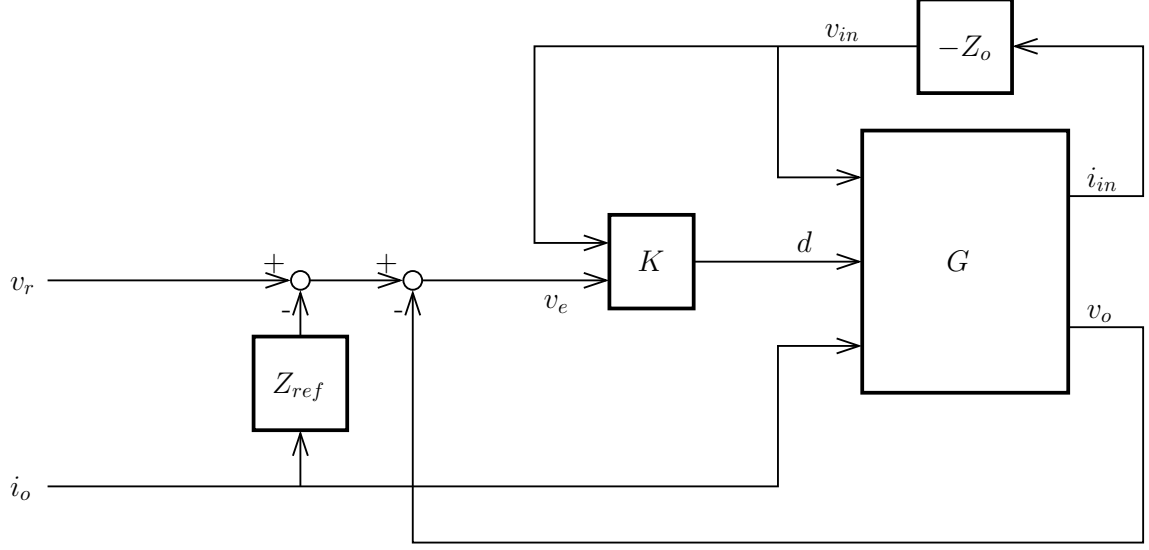


Figure 6.1: Voltage mode control of a DC/DC converter with load-line and input voltage feedforward, in the presence of an input filter.

conditions. This generates a “terminated” model, in which the following transfer functions define block G according to Fig. 6.2:

$$G_{iv} = \frac{D^2}{R_{dcr} + R_L} \cdot \frac{(R_{esr}Cs + 1)}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \quad (6.2)$$

$$G_{ii} = D \cdot \frac{R_L}{R_{dcr} + R_L} \cdot \frac{R_{esr}Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \quad (6.3)$$

$$G_{id} = \frac{DV_{in}}{R_{dcr} + R_L} \cdot \left(1 + \frac{(R_{esr} + R_L)Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \right) \quad (6.4)$$

$$G_{vv} = D \cdot \frac{R_L}{R_{dcr} + R_L} \cdot \frac{R_{esr}Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \quad (6.5)$$

$$G_{vi} = -\frac{R_L}{R_{dcr} + R_L} \frac{(Ls + R_{dcr})(R_{esr}Cs + 1)}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \quad (6.6)$$

$$G_{vd} = V_{in} \cdot \frac{R_L}{R_{dcr} + R_L} \cdot \frac{R_{esr}Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \quad (6.7)$$

For a representative VRM application, the component and parameter values are

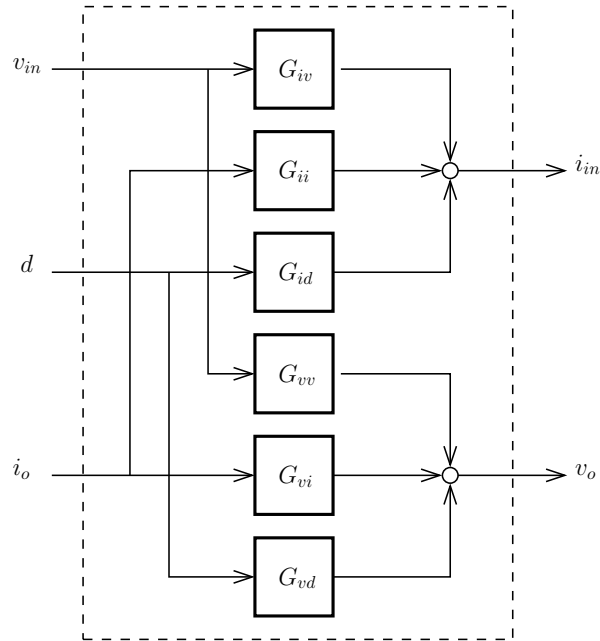


Figure 6.2: Internal structure of block G .

presented in Table 6.1. The table also includes the specification of the load-line R_{LL} and the range of output currents. The switching frequency and the desired bandwidth are also specified. The input filter corresponds to the one shown in Fig. 5.6. Table 6.2 shows the filter component values. In both tables, the range of variation for selected parameters is also indicated. The purpose of this study is to analyze the effect of the input filter on the dynamics of the converter, therefore only the filter parameters and the operating point are allowed to change, while the converter parameters are assumed constant. In order to simplify the formulation, the frequency and damping of the input LC filter are changed by variations in the capacitor's parameters only.

Table 6.1: Representative VRM application values

Component/Parameter	Nominal Value	Range of Variation
V_{in}	12V	10 – 13V
V_{ref}	1.2V	0.8 – 1.3V
L	100nH	
R_{dcr}	1m Ω	
C	800 μ F	
R_{esr}	1m Ω	
R_{LL}	1.25m Ω	
I_o	100A	1 – 120A
f_s	1MHz	
BW	80kHz	

Table 6.2: Input filter values

Component	Nominal Value	Range of Variation
L_f	800nH	
R_{dc}	0.1m Ω	
C_f	500 μ F	200 – 3,000 μ F
R_{es}	1m Ω	.2 – 20m Ω

6.2.2 Preliminary analysis

Applying the Middlebrook criterion to this system, it can be seen that the stability conditions are not met for some input filter parameters in the range specified. This is illustrated in Fig. 6.3, showing the Bode plots of the input impedance of the converter G_{iv}^{-1} at a high-load condition and the output impedance of the input filter Z_o . A set of plots for Z_o are shown corresponding to a representative set of input filter parameter variations. The input filter resonance is not damped enough in some cases and the peak becomes larger than the input impedance of the converter. It is expected, from previous analysis, that the system would be unstable if the bandwidth of the loop is above the input filter resonance for those particular sets of parameters.

This problem formulation is a good candidate to explore to what extent the use of input voltage feedforward and robust design techniques could overcome the fundamental limit of performance observed in the traditional SISO controller design.

6.2.3 PID feedback design

In this design, the controller K shown in Fig.6.1 has the feedforward path from v_{in} to d equal to zero, and the feedback path from v_e to d is designed using standard control techniques. The input filter is assumed to be absent, implying that the loop to be designed is formed by the series connection of the controller K and the duty-cycle to output voltage transfer function G_{vd} , which will be referred to as “the plant”. The

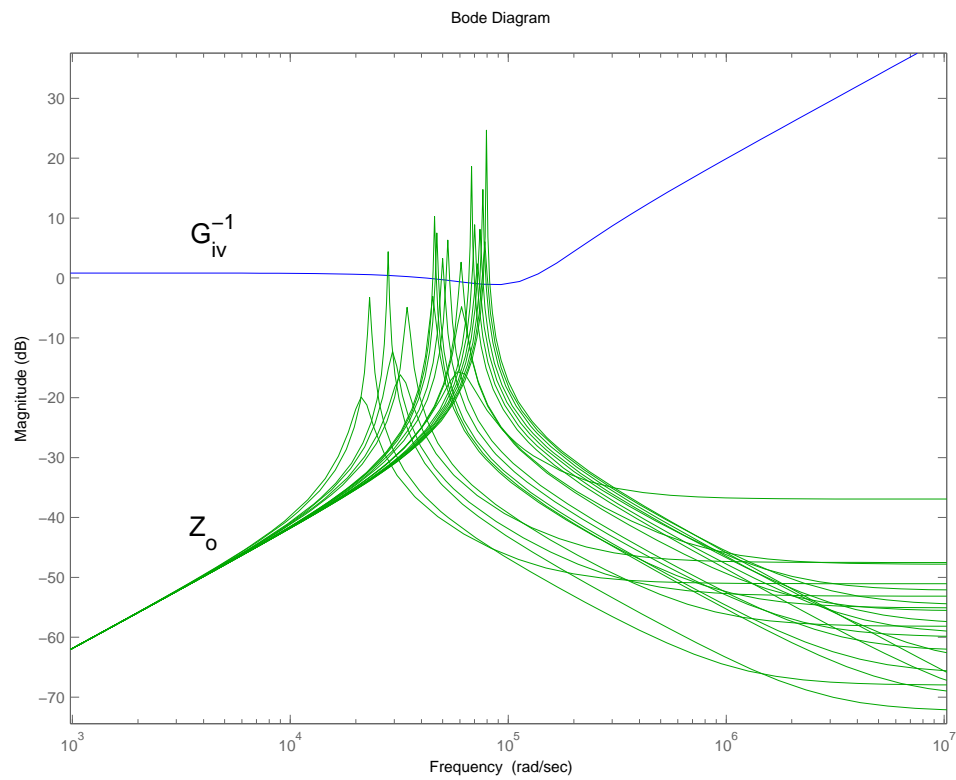


Figure 6.3: Magnitude of the input impedance of the converter G_{iv}^{-1} compared with the magnitude of the output impedance of the filter Z_o for a set of different parameter values.

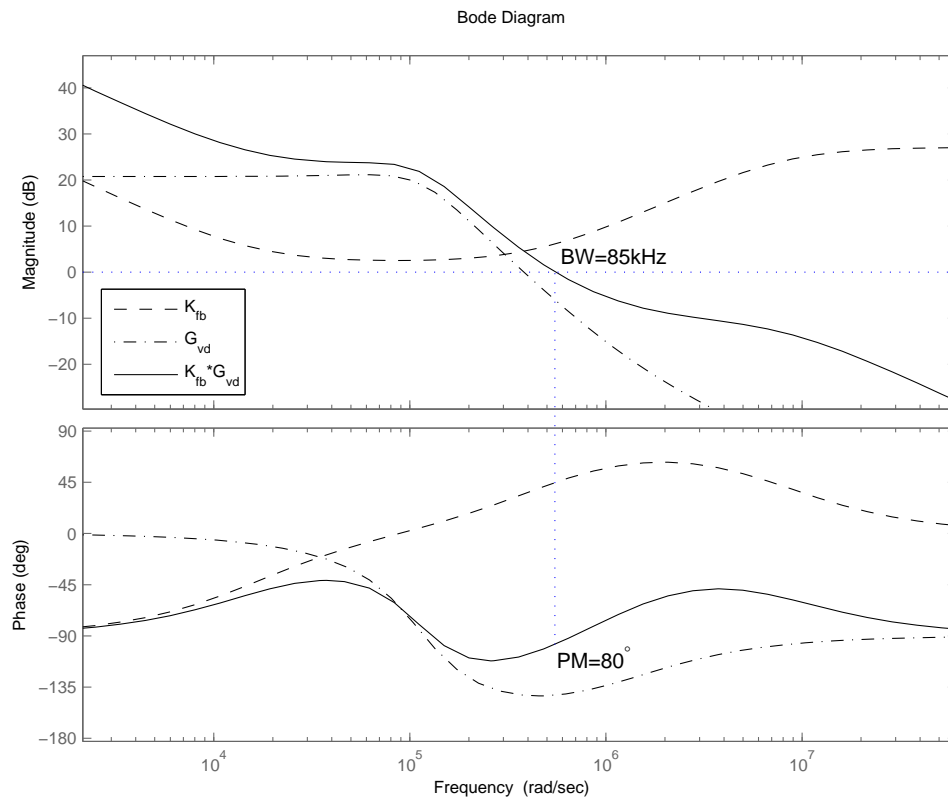


Figure 6.4: Feedback PID design. Bode plot of the controller (dashed line), the plant (dash-dotted line), and the resulting loop gain (solid line).

design is performed under the most demanding situation, which is at high load.

The PID controller has one pole at the origin, two zeros located in the proximity of the plant's double pole, and an additional pole located in proximity to the ESR zero introduced by the output capacitor. The Bode plot of the controller, the plant, and the loop are shown in Fig. 6.4. The bandwidth is around $85kHz$ and the phase margin 80° .

The design appears to be adequate, however when the input filter is connected

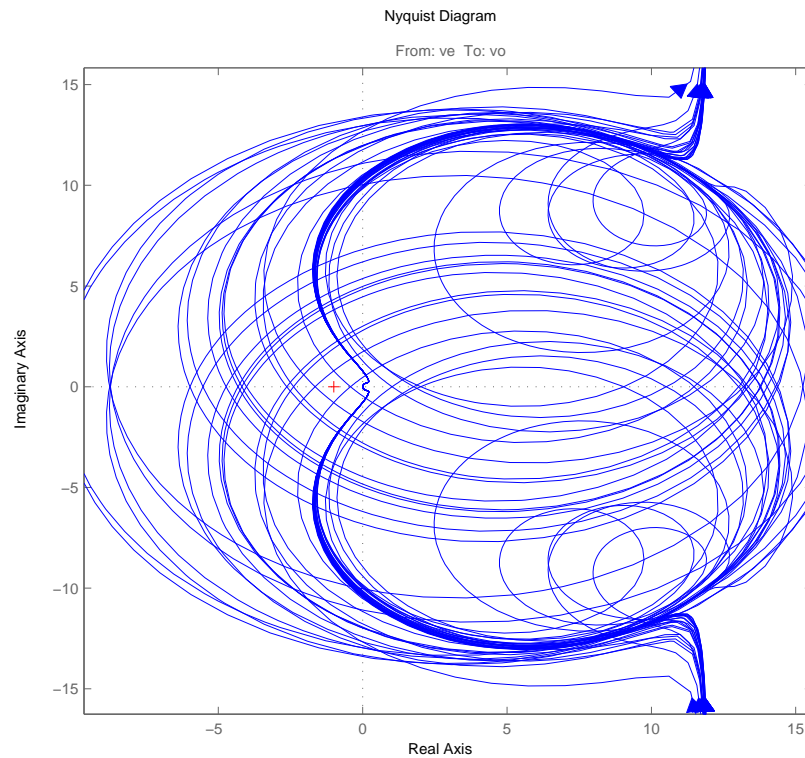


Figure 6.5: Set of Nyquist plots of the feedback PID design for different input filter parameters.

and the new loop gain computed (for example, using the extra-element theorem), instability is revealed in the set of Nyquist plots of Fig. 6.5. For each input filter parameter value set, a different Nyquist plot is shown. Some of the plots encircle the $(-1, 0)$ point, revealing instability. This is not surprising, since it was predicted in the previous section.

6.2.4 Input voltage feedforward

This design is based on that in [36]. The feedback controller is the same PID as in the previous section, but an input voltage feedforward path equal to $-\frac{D}{V_{in}}$ is added. The controller K , as shown in Fig. 6.1 has now two inputs and one output. This ideally cancels out the effect of any input filter in the loop gain. However, this is equivalent to a RHP zero-pole cancellation that hides the instability such that it is not observed at the output. A slight deviation from the ideal conditions reveals the instability in the output of the system.

The Nyquist plot of the loop under variations in the input filter is shown in Fig. 6.6. Comparing with Fig. 6.5 it can be appreciated that the feedforward term effectively cancels the effect of the input filter in the loop, which appears now to be stable. However, when the input voltage is allowed to change (in addition to the variations in the input filter), the feedforward term is not ideal anymore and the Nyquist plot of the loop becomes the set shown in Fig. 6.7. In this case it can be seen that the system is unstable for some set of parameters in the range of variation, as evidenced by the encirclement of the point $(-1, 0)$.

6.2.5 μ -synthesis design

The examples in the previous sections illustrate that the RHP zeros impose a fundamental limitation in the conventional design of controllers for DC/DC convert-

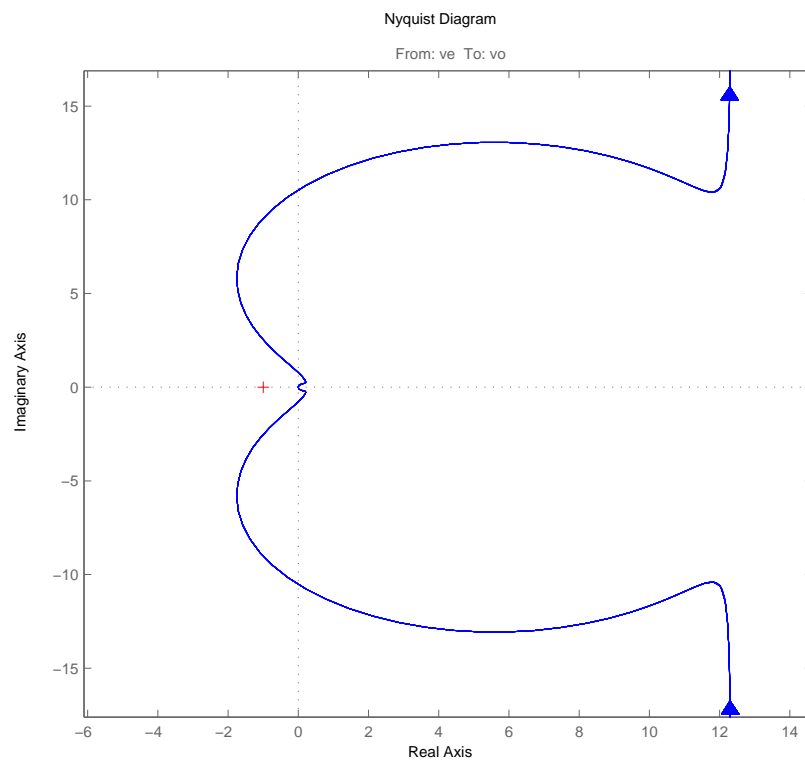


Figure 6.6: Nyquist plot of the feedforward design under ideal conditions.

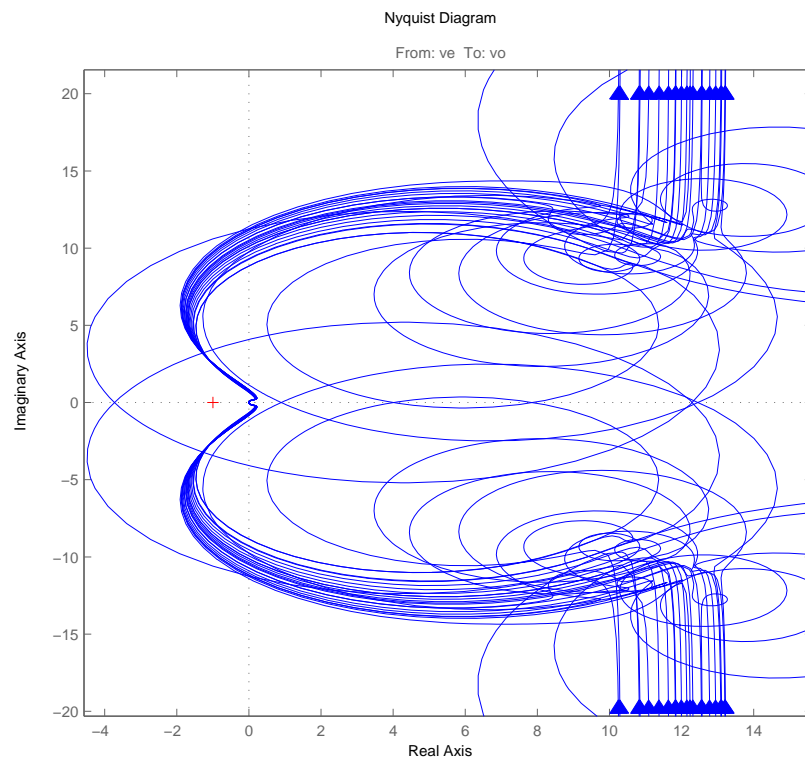


Figure 6.7: Nyquist plot of the feedforward design with variations in the input voltage.

ers with an undamped input filter. To confirm this, a larger set of controllers is explored by using the μ -synthesis algorithm available in the Matlab Robust Control Toolbox [55]. The idea is to try to find out if there exists any controller K that could achieve stability and adequate performance under the constraints of the problem. In order to proceed with the controller design, the problem has to be posed as a norm minimization problem. The following setup is based on the methodology described in [56] and [55].

The system setup is shown in Fig. 6.8. The inputs to be considered are the voltage reference v_r and the output current i_o , while the main output of interest is the error voltage v_e . In order to penalize the amplitude of perturbations in the input voltage and to comply with well-posedness conditions, the input voltage v_{in} and the duty-cycle command d are also included as outputs respectively. The model is valid up to half the switching frequency, so the uncertainty due to the switching action is included by adding an extra perturbation input v_s at the output of the plant. All these signals have to be weighted in order to constrain the problem with realistic specifications. The dashed box indicates the controller location, to be synthesized by the designer or the control design algorithm.

The system, then, has the form indicated in Fig. 6.9. The controller K has two inputs and one output, and is to be designed in order to minimize the H_∞ norm of the transfer function from the inputs (v_r, i_o, v_s) to the outputs $(\tilde{v}_e, \tilde{v}_{in}, \tilde{d})$ under all

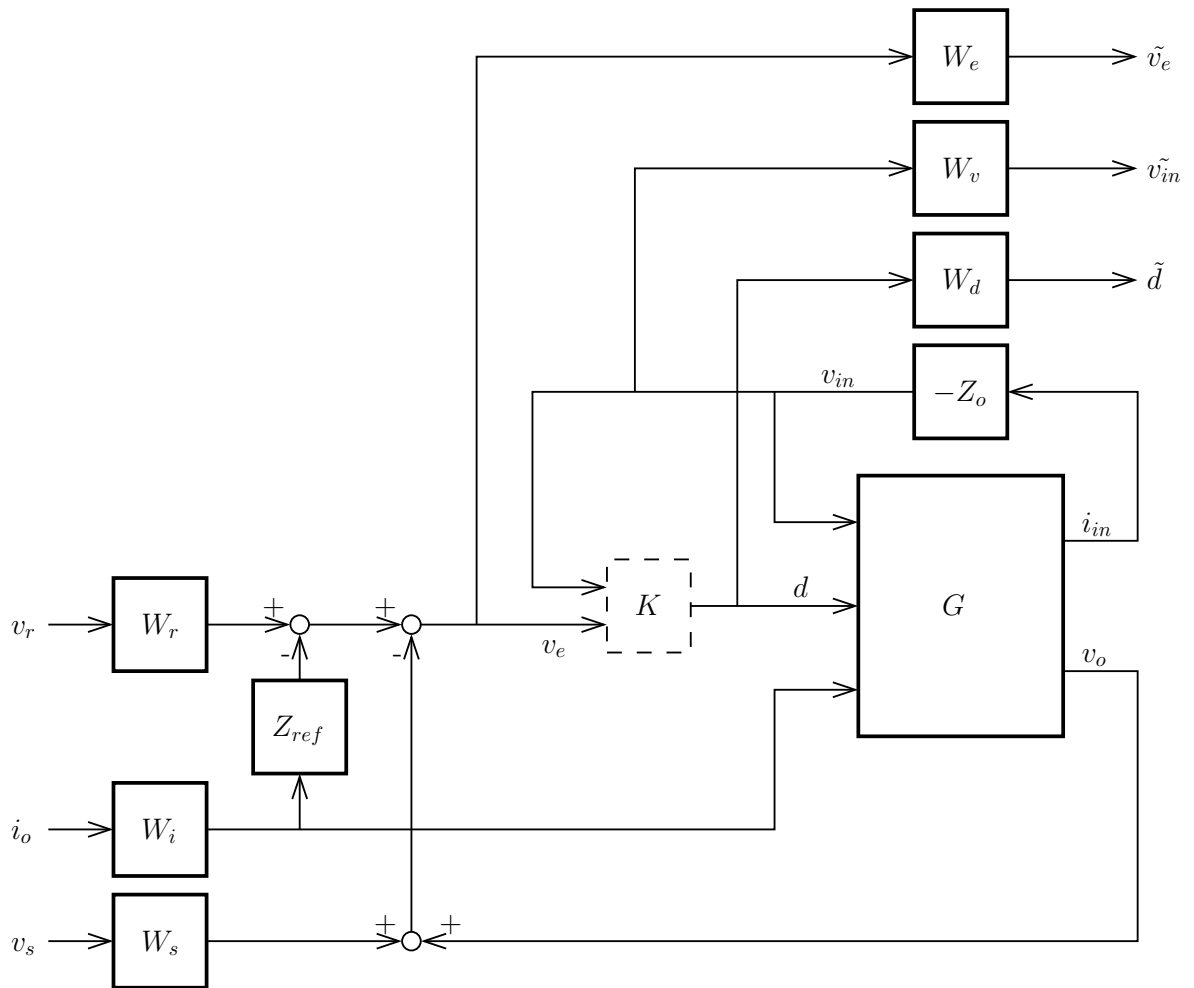


Figure 6.8: System setup for robust control design.

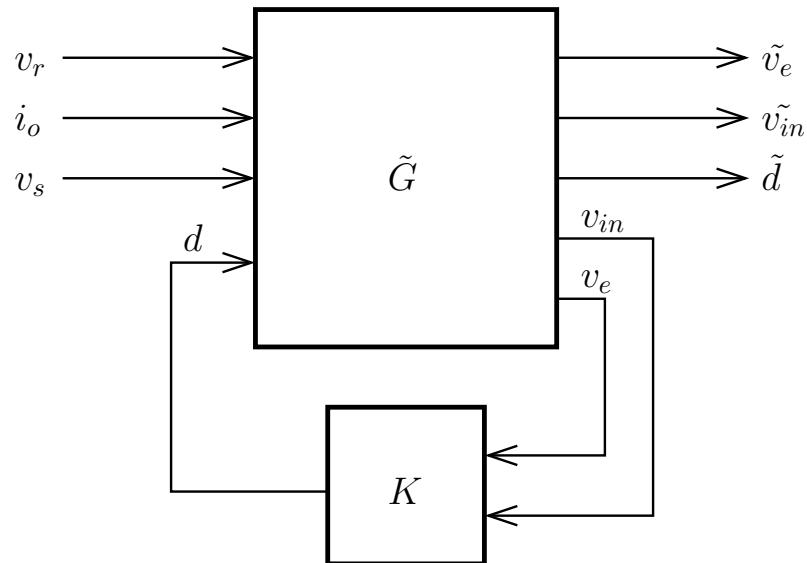


Figure 6.9: Simplified system setup for robust control design.

parameter variations, while preserving stability.

For this application, the weighting functions used to shape the system's response are shown in Figs. 6.10 and 6.11 for the inputs and outputs respectively. The weights at the reference inputs v_r and i_o represent the bandwidth of the signals to be tracked. The weight in the perturbation v_s represents the uncertainty at frequencies above half the switching frequency. On the other hand, the weights at the outputs represent the desired bandwidth of the system as well as the relative importance of the different signals.

The μ -synthesis algorithm was run on a system with uncertainties in the input filter and the input voltage. The code is presented in Appendix C. The Bode plot of the controller synthesized is shown in Fig. 6.12, compared with the controller of the

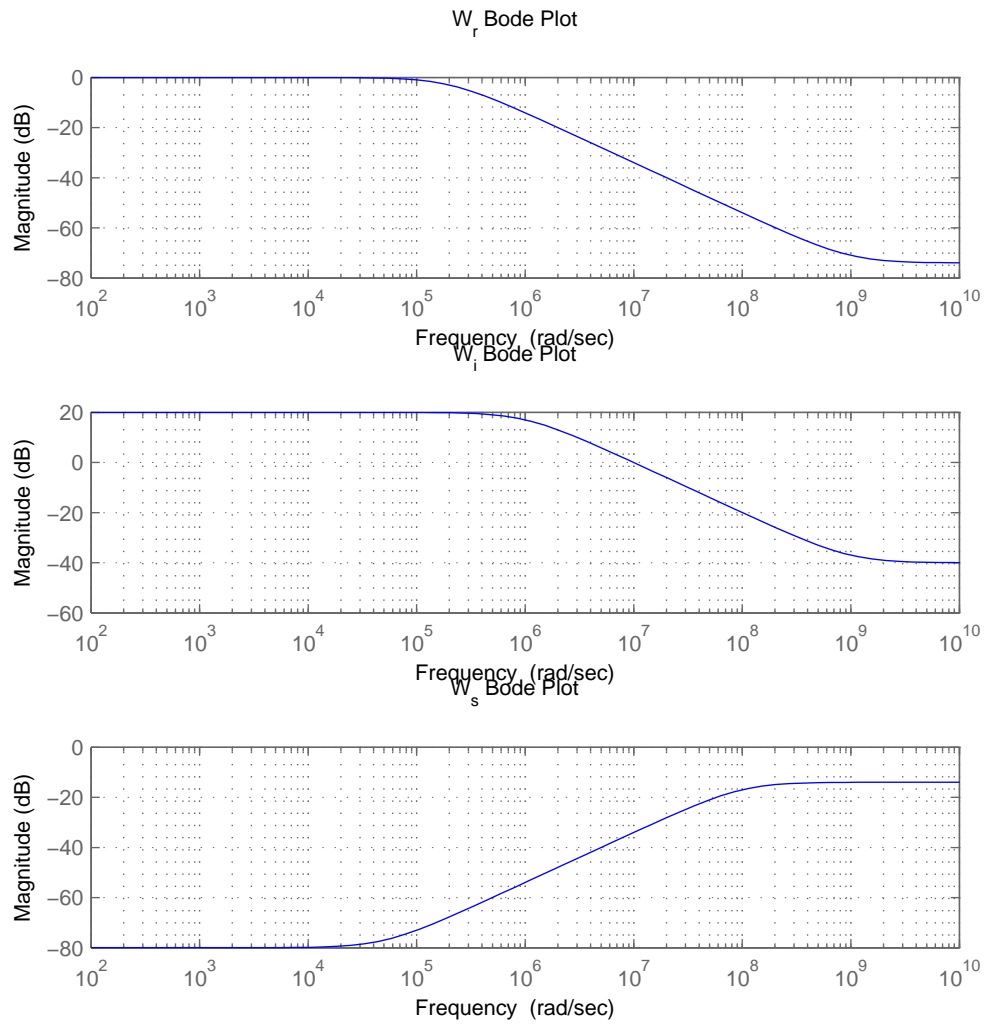


Figure 6.10: Weighting functions for the inputs.

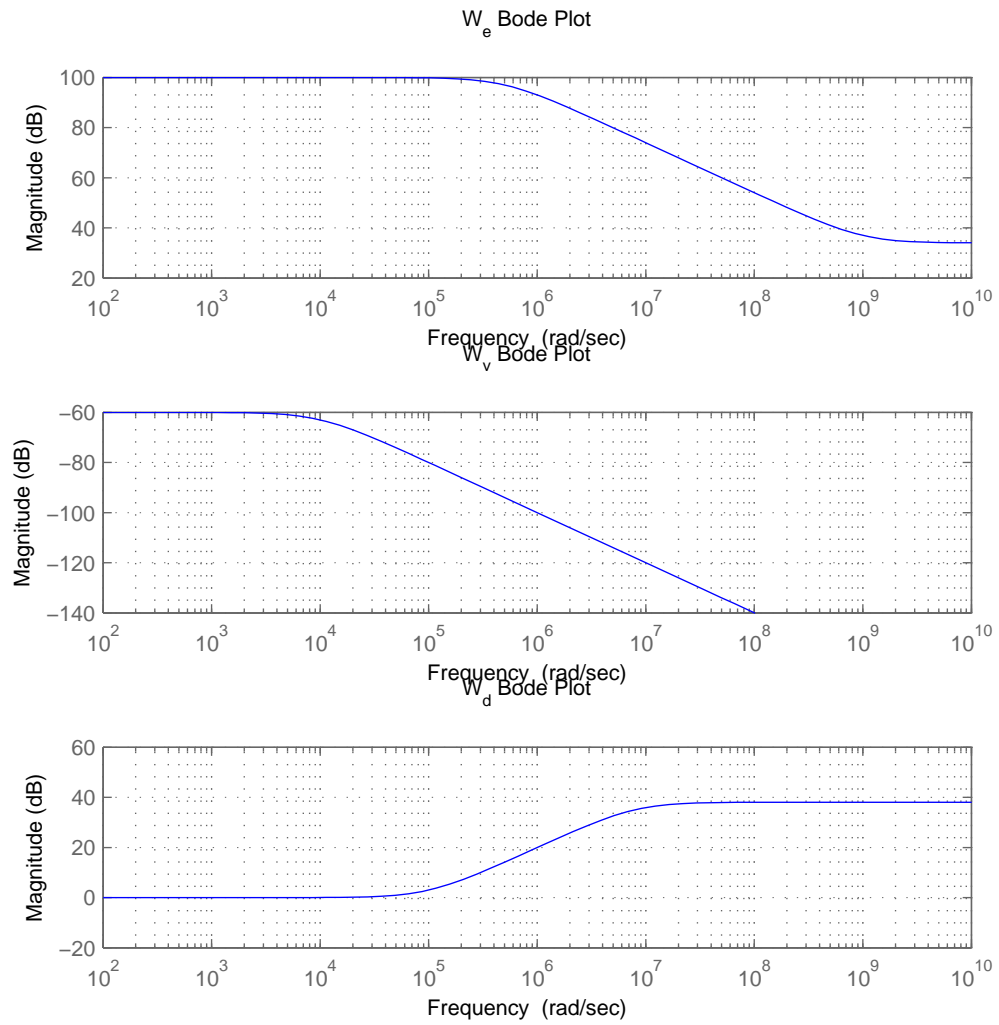


Figure 6.11: Weighting functions for the outputs.

previous section (PID feedback and input voltage feedforward). It can be seen that the μ controller has a much lower gain, especially in the region of the resonant frequency of the input filter. The loop transfer function Bode plot is shown in Fig. 6.13 and the Nyquist plot in Fig. 6.14. The loop magnitude is less than $0dB$ for all frequencies, this means that effectively the feedback loop is not present and performance of the system is very poor. As evidenced by the Nyquist plot, the system is stable. One possible interpretation of this result is that the controller tries to suppress the frequencies in which an abrupt phase change occurs due to the undamped filter. As a consequence, the Nyquist plot does not encircle the point $(-1,0)$ because the magnitude of the loop transfer function is less than unity.

6.2.6 Conclusions

It can be concluded by the previous analysis and the examples shown that there does not seem to be a control strategy that permits a stable operation of a DC/DC converter with an undamped input filter, while achieving a bandwidth above the resonance of the filter. The strategy of damping the input filter that is standard practice at the present seems to be the only feasible solution to the problem. The next section proposes an alternative way of damping the input filter without using physical resistors.

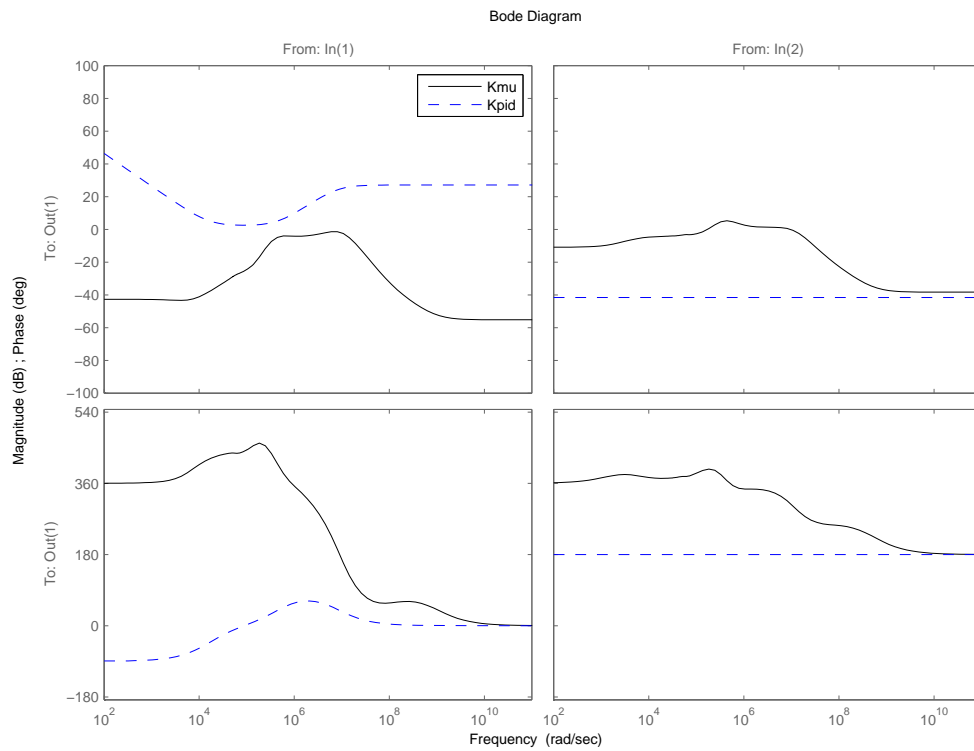


Figure 6.12: Bode plot of the μ controller (solid) compared with the PID controller (dashed). Left: error voltage to duty-cycle transfer function. Right: input voltage to duty-cycle transfer function. Top: magnitude. Bottom: phase.

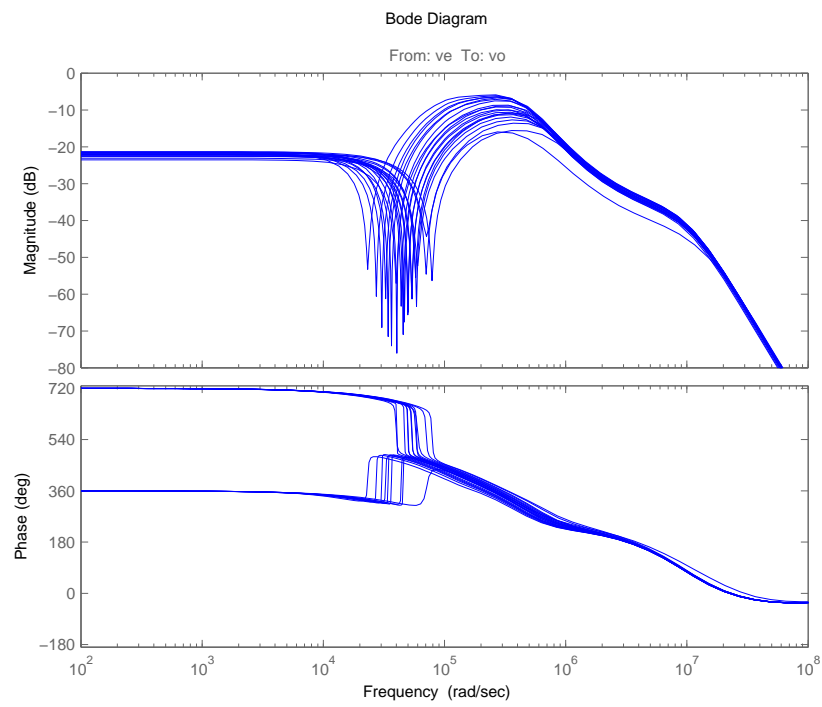


Figure 6.13: Set of Bode plots of the loop with the μ controller for different input filter parameter values.

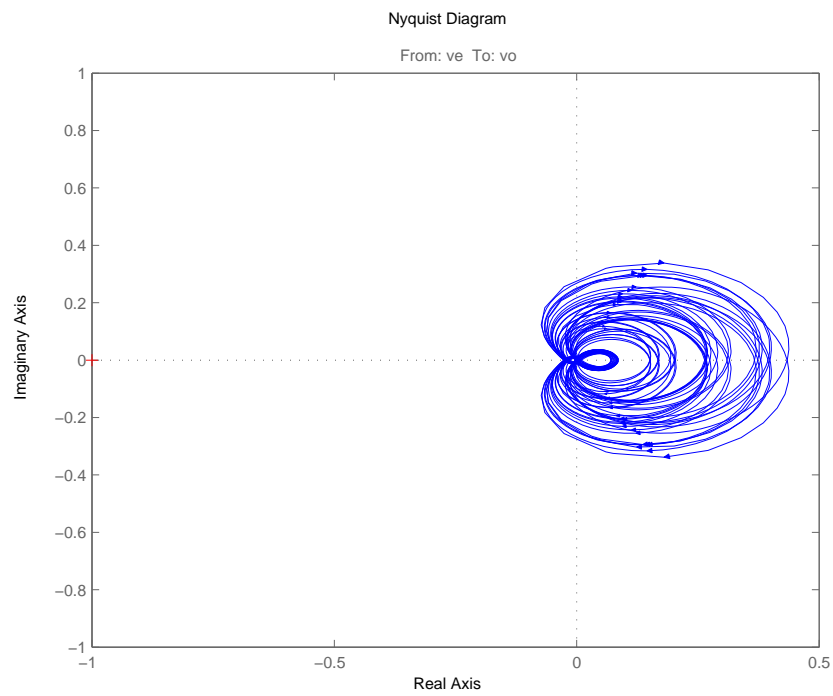


Figure 6.14: Nyquist plot of the loop with the μ controller for different input filter parameter values.

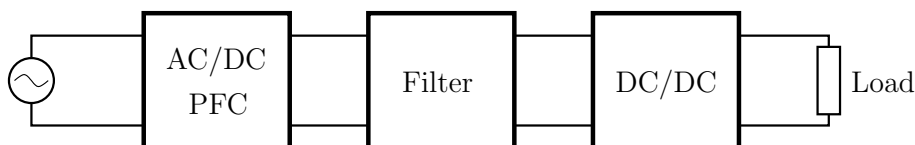


Figure 6.15: Simple DPS architecture.

6.3 Virtual damping of input filter

It has been shown in the previous sections that the presence of an input filter in a power converter under certain conditions could affect the stability of the system, and no control strategy in the converter can solve the problem. The most a control system can achieve is to stabilize the system at the expense of performance. In this section, a different approach from a systems perspective is explored.

Consider the simple DPS architecture shown in Fig. 6.15. A front-end converter performs power factor correction (PFC) and provides a mildly regulated DC bus. A point-of-load (POL) DC/DC converter provides a tightly regulated voltage to the load from this intermediate bus. An EMI filter is used at the input of the POL converter to reduce the frequency content of its input current.

It has been shown that the effects of the filter on the dynamics of the POL converter can be reduced by adding damping. Instead of adding physical damping, the output impedance of the front-end converter can be adjusted to provide the necessary damping. The idea is illustrated in Fig. 6.16. The output impedance of the front-end converter can be made resistive (R_o) over a wide frequency range in

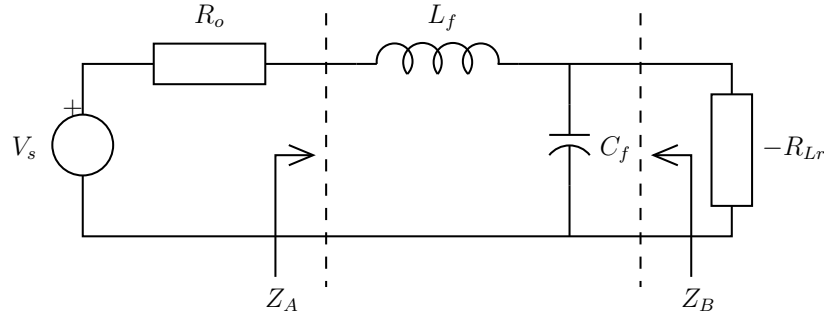


Figure 6.16: Equivalent circuit of simple DPS architecture.

order to damp the input filter and counteract the negative input resistance of the POL converter $-R_{Lr} = -\frac{R_L}{\eta D^2}$.

The system can be viewed as two two-ports interconnected: one is the filter with impedances Z_A and Z_B , and the other one is composed by the two independent resistances $-R_{Lr}$ and R_o . However, the system can also be viewed as two stable one-ports interconnected: one is the filter with resistance R_o in series, and the other is the DC/DC converter with impedance $-R_{Lr}$. This permits a simpler yet still rigorous analysis, because the special case described in Section 5.3 can be used. The location of the zeros of $1 - Z_B Y_{Lr}$ with $Y_{Lr} = \frac{1}{R_{Lr}}$ determine the stability of the interconnection.

Impedance Z_B can be computed as

$$Z_B = (L_f s + R_{dc} + R_o) \parallel \left(\frac{1}{C_f s} + R_{es} \right) \quad (6.8)$$

$$= \frac{(L_f s + R_{dc} + R_o) \cdot (R_{es} C_f s + 1)}{L_f C_f s^2 + (R_{dc} + R_{es} + R_o) C_f s + 1}. \quad (6.9)$$

Stability can be analyzed using the Routh-Hurwitz criterion on the numerator of

$1 - Z_B Y_{Lr}$, which is

$$\left(1 - \frac{R_{es}}{R_{Lr}}\right) L_f C_f s^2 + \left[\left(R_{dc} + R_o + R_{es} - \frac{R_{es}(R_{dc} + R_o)}{R_{Lr}} \right) C_f - \frac{L_f}{R_{Lr}} \right] s + 1 - \frac{R_{dc} + R_o}{R_{Lr}} \quad (6.10)$$

The coefficient $\left(1 - \frac{R_{es}}{R_{Lr}}\right)$ is positive for representative values of the parameters, but the term $\left(1 - \frac{R_{dc} + R_o}{R_{Lr}}\right)$ may not be always positive depending on the value of R_o . The stability conditions can be written as:

$$\left(1 - \frac{R_{dc} + R_o}{R_{Lr}}\right) > 0 \text{ and} \quad (6.11)$$

$$\left[\left(R_{dc} + R_o + R_{es} - \frac{R_{es}(R_{dc} + R_o)}{R_{Lr}} \right) C_f - \frac{L_f}{R_{Lr}} \right] > 0. \quad (6.12)$$

These conditions impose bounds on the values of R_o :

$$\frac{Z_C^2 - R_{es} R_{Lr}}{R_{Lr} - R_{es}} - R_{dc} < R_o < R_{Lr} - R_{dc} \quad (6.13)$$

Under the usual assumptions that $R_{Lr} \gg R_{es}, R_{dc}$, the expressions can be simplified to the following

$$\frac{Z_C^2}{R_{Lr}} - (R_{es} + R_{dc}) < R_o < R_{Lr}. \quad (6.14)$$

Notice that the most constrained case is given by the lowest value of R_{Lr} , i.e., under a high-load condition.

For the typical values reported in Tables 6.1 and 6.2, the assumptions are valid and the worst-case value for R_{Lr} is $640m\Omega$, then the bounds would be

$$1.4m\Omega < R_o < 640m\Omega. \quad (6.15)$$

The designer has a wide range of options for selecting R_o .

The circuit in Fig. 6.16 was simulated using LTspice/SwCADIII [57]. The value for R_{Lr} used was $640m\Omega$ and the input filter values were taken from 6.2. A voltage step was introduced at the input and the capacitor voltage was observed. Several values of R_o were used, spanning the range indicated in (6.15). The results are shown in Fig. 6.17 and corroborate the theoretical results. For $R_o = 1m\Omega$ the system is unstable. For $R_o = 1.4m\Omega$ it is marginally stable. For $R_o = 2, 20,$ and $500m\Omega$ the system is stable with different damping characteristics. For $R_o = 640m\Omega$ and above the system becomes unstable. These results are in agreement with the range predicted in (6.15).

6.4 Conclusions

This chapter has analyzed the input filter problem from the fundamentals of control system theory. It has been illustrated by examples that there exist fundamental limits to the performance of a DC/DC converter in the presence of an undamped input filter. The only stabilizing controller that could be found using an optimizing algorithm was shown to have poor performance due to the fact that it suppresses the frequency range in which the input filter resonance occurs.

A virtual damping technique has been proposed that allows for stable operation without compromising the performance of the system. The technique is based on

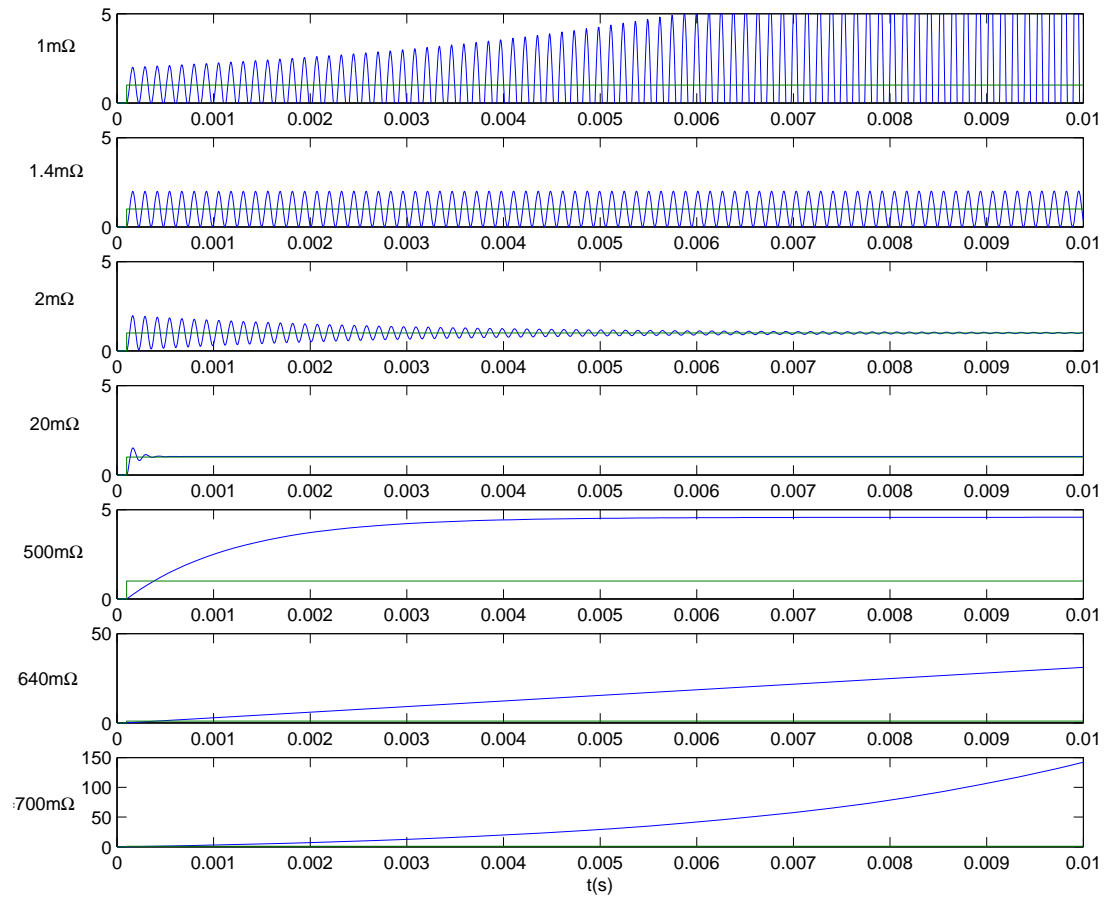


Figure 6.17: Simulation of the virtual damping example with different values of R_o . Response to an input voltage step.

a system-level design in which the system interconnected to the input of the input filter has a resistive output impedance. Simulations corroborate the design equations derived analytically.

In DPS designs, techniques like the one described above could be used to guarantee stability and performance of the interconnection without adding physical components that increment the size, weight, and cost of the system.

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Appendix C

Robust design Matlab code

```
% Robust design of buck converter controller with input filter

% nominal parameters
Vin_nom = 12; % input voltage
Vref_nom = 1.2; % reference voltage
N = 4; % number of phases
L_nom = 400e-9/N; % total inductance
Rdcr_nom = 4e-3/N; % inductor DC resistance
C_nom = 800e-6; % output cap
Resr_nom = 1e-3; % cap series resistance
Io_nom = 100; % output current
Rref = 1.25e-3; % droop

% actual values
Vin = ureal('Vin',Vin_nom,'Range',[10 13]);
Vref = Vref_nom;
L = L_nom;
Rdcr = Rdcr_nom;
C = C_nom;
Resr = Resr_nom;
Io = Io_nom;

% derived values
```

```

Vo = Vref;
D = Vref_nom/Vin_nom;
R = .01; % 1 for light load, .01 for high load

% input voltage feedforward
F = -D/Vin;

% input filter
Lin = 800e-9;
Rdcin = .1e-3;
Cin = ureal('Cinreal',500e-6,'Range',[200e-6 3000e-6]) + ...
      ultidyn('Cinlti',[1 1],'Bound',0.05*800e-6);
Resin = ureal('Resinreal',1e-3,'Range',[.2e-3 20e-3]) + ...
        ultidyn('Resinlti',[1 1],'Bound',0.05*3e-3);

% controller
Kp = 32; % proportional gain
Kd = 256; % derivative gain
Ki = 0.125; % integral gain
fsw = 1e6; % switching frequency
T = 1/fsw; % switching period
fsamp = fsw*N; % sampling frequency
Tsamp = 1/fsamp; % sampling period

% converter averaged continuous-time model
Gvd = Vin*R/(R+Rdcr)*tf([Resr*C 1], ...
    [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);
Gvv = D*R/(Rdcr+R)*tf([Resr*C 1], ...
    [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);
Gvi = -R*Rdcr/(R+Rdcr)*tf([Resr/Rdcr*L*C Resr*C+L/Rdcr 1], ...
    [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);
Gid = D*Vin/(R+Rdcr)*(1+tf([(Resr+R)*C 1], ...
    [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]));
Giv = D^2/(R+Rdcr)*tf([(Resr+R)*C 1], ...
    [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);
Gii = D*R/(R+Rdcr)*tf([Resr*C 1], ...
    [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);

% PID controller
Ad = 1/2/Vin_nom * (tf(Kd.*[1 -1],[1 0],Tsamp) + ...

```

```

        tf(Kp,1,Tsamp)+tf(Ki.*[1 0],[1 -1],Tsamp));
A = d2c(Ad,'tustin');

% reference impedance (load-line)
Zref = Rref*tf([Resr*C 1],[Rref*C 1]);

% input filter
Zo = tf([Resin*Lin*Cin Lin+Resin*Rdcin*Cin Rdcin], ...
        [Lin*Cin (Rdcin+Resin)*Cin 1]);

% weights
We = tf(1e5*[1/1e9 1],[1/5e5 1]); % minimize error up to BW
Wr = tf([1/1e9 1],[1/2e5 1]); % reference BW around 33kHz
Wd = tf(10*[1/1e9 1],[1/1e6 1]); % more weight on output current disturbance
Wu = tf([1/1e5 1],[1/8e6 1]); % penalize actuator input for well-posedness
Wv = tf(1e-2*[1/1e9 1],[1/1e4 1]); % penalize input voltage for stability
Ws = tf(1e-2*[1/1e5],[1/1e8 1]); % disturbance due to switching

% interconnection for mu design
systemnames = 'Gvd Gvv Gvi Giv Gid Gii Zo Zref We Wr Wd Wu Wv Ws';
inputvar = '[vr;io;vs;d]';
outputvar = '[We;Wu;Wv;Wr-Zref-Gvd-Gvv-Gvi-Ws;-Zo]';
input_to_Gvd = '[d]';
input_to_Gvv = '[-Zo]';
input_to_Gvi = '[Wd]';
input_to_Gid = '[d]';
input_to_Giv = '[-Zo]';
input_to_Gii = '[Wd]';
input_to_Zo = '[Giv+Gid+Gii]';
input_to_Zref = '[Wd]';
input_to_We = '[Wr-Zref-Gvd-Gvv-Gvi-Ws]';
input_to_Wr = '[vr]';
input_to_Wd = '[io]';
input_to_Wu = '[d]';
input_to_Wv = '[-Zo]';
input_to_Ws = '[vs]';
cleanupsysic = 'yes';
P = sysic;
P.InputName={'vr' 'io' 'vs' 'd'};
P.OutputName={'vet' 'vut' 'vint' 've' 'vin'};

```

```

% interconnection for CL analysis
systemnames = 'Gvd Gvv Gvi Giv Gid Gii Zo Zref';
inputvar = '[vr;io;d]';
outputvar = '[Gvd+Gvv+Gvi;vr-Zref-Gvd-Gvv-Gvi;-Zo]';
input_to_Gvd = '[d]';
input_to_Gvv = '[-Zo]';
input_to_Gvi = '[io]';
input_to_Gid = '[d]';
input_to_Giv = '[-Zo]';
input_to_Gii = '[io]';
input_to_Zo = '[Giv+Gid+Gii]';
input_to_Zref = '[io]';
cleanupsysic = 'yes';
P2 = sysic;
P2.InputName={'vr' 'io' 'd'};
P2.OutputName={'vo' 've' 'vin'};

% traditional controllers
Kfb = [A 0]; % only feedback
Kff = [A F]; % standard controller w/feedforward

% mu design
opt = dkitopt('NumberOfAutoIterations',4);
[Kmu,CLmu,bnd] = dksyn(P,2,1,opt);

% closed-loop systems
CL2fb = lft(P2,Kfb);
CL2ff = lft(P2,Kff);
CL2mu = lft(P2,Kmu);

% interconnections for OL analysis
systemnames = 'Gvd Gvv Giv Gid Zo Kfb';
inputvar = '[ve]';
outputvar = '[Gvd+Gvv]';
input_to_Gvd = '[Kfb]';
input_to_Gvv = '[-Zo]';
input_to_Gid = '[Kfb]';
input_to_Giv = '[-Zo]';
input_to_Zo = '[Giv+Gid]';

```

```
input_to_Kfb = '[ve;-Zo]';
cleanupsysic = 'yes';
Pfb = sysic;
Pfb.InputName={'ve'};
Pfb.OutputName={'vo'};

systemnames = 'Gvd Gvv Giv Gid Zo Kff';
inputvar = '[ve]';
outputvar = '[Gvd+Gvv]';
input_to_Gvd = '[Kff]';
input_to_Gvv = '[-Zo]';
input_to_Gid = '[Kff]';
input_to_Giv = '[-Zo]';
input_to_Zo = '[Giv+Gid]';
input_to_Kff = '[ve;-Zo]';
cleanupsysic = 'yes';
Pff = sysic;
Pff.InputName={'ve'};
Pff.OutputName={'vo'};

systemnames = 'Gvd Gvv Giv Gid Zo Kmu';
inputvar = '[ve]';
outputvar = '[Gvd+Gvv]';
input_to_Gvd = '[Kmu]';
input_to_Gvv = '[-Zo]';
input_to_Gid = '[Kmu]';
input_to_Giv = '[-Zo]';
input_to_Zo = '[Giv+Gid]';
input_to_Kmu = '[ve;-Zo]';
cleanupsysic = 'yes';
Pmu = sysic;
Pmu.InputName={'ve'};
Pmu.OutputName={'vo'};
```