# ECE446/546
# Project 2

**Aim**: Design and simulate a Cuk regulator. Use the techniques discussed in class.

Both the power stage and the feedback loop frequency compensation need to be designed. The following specifications are to be met.

$V_g = 12$

$V_o = -24$

$V_{o,ripple} = 5\%$

$f_s = 100kHz$

$R_L = 12\Omega - 120\Omega$

$V_M = 5$

$V_{g,step} = 20$

An evaluation of the efficacy of the frequency compensation will be made by the nature of the step response of the input voltage, from $V_g$ to $V_{g,step}$ and from $V_{g,step}$ to $V_g$. Be sure that your report clearly shows the simulation results of the output voltage for these input steps.

Your report should show your compensation design using Bode asymptotes. After your design is completed obtain an accurate loop gain plot using the Matlab *margin* command.
For this, the transfer function of the converter can be directly obtained from the state equations or from the analytically determined transfer function before any approximation is undertaken. From the *margin* command the gain and phase margins should be noted.

Your report should be written in the form of a technical paper. Your report should include (but be not limited to) the following:

a) Your complete design in a schematic annotated with the component values,
b) Your Matlab determined loop gain plot, noting your gain and phase margins, (provide your actual Matlab code in appendix).
c) Your output voltage step responses, using the PECS simulator.

Further discussion on the content on the report is given on the next page.

Your report should present the following:

- Derivation of the control-to-output voltage transfer function. For simplicity, have no parasitics present.
- The resulting transfer function features a $4^{th}$ order denominator and a $2^{nd}$ order numerator. To make sense of the denominator it is symbolically factored. This factorization involves certain restrictions on the component values. As a first try use the 'Cuk factorization', as discussed in class.
- Examine the Bode plot (magnitude and phase) of the above transfer function. Specifically discuss the three possibilities that exist, and pick the most desired form.
- Examine the inconsistency of the desired Bode plot with the factorization used. This then motivates a second factorization, discussed next.
- Obtain an alternative factorization and determine the component restrictions which need to be satisfied for it to be true.
- The alternative factorization leads to a complex pole pair with infinite Q. Discuss the issues this causes with feedback implementation.
- Overcoming the infinite Q problem is tackled in two ways:
    1) Introduce the parasitic resistances that exist in the converter which have been ignored so far. Specifically the inductor and capacitor ESR's. Only consider practical values for these parasitic.
    2) Introduce lossless damping across the middle capacitor. Mathematically show how damping is introduced using this method.
- Show the Bode plots for the two different approaches. Make sure you do not use any approximations at this stage. The easiest way to do this is to reformulate the state equations for the two designs.
- To determine the *L* and *C* values in the converter the following leads to component constraints:
    - Avoidance of DCM mode. (Leads to a constraint on the input inductor).
    - Avoidance of DVM (discontinuous voltage mode). (Leads to a constraint on the middle capacitor).
    - Output voltage ripple. (Leads to a constraint on the output LC value).
    - Factorization used (and in the case of lossless damping the constraint on the validity of using it).
    - Acceptable current ripple in the inductors. (Leads to constraints on the inductor values).
- Check that all constraints are met by the actual component values used in your design.
- Compare the two designs by simulation on PECS.