ECE446/546

Project – Droop control design for Buck Converter

Aim: To design and compare two different droop control design approaches with the more usual control approach for Buck converters. The performance of each is compared through simulation.

The parameters of the Buck converter are: V_g = 28*V*, *V*= 15*V*, *L*=50 μH, *C=500* μF, V_M =*4V* (V_M is the peak-to-peak amplitude of the sawtooth waveform used in the *PWM* modulator), and f_s = 100*kHz*, as before, in last term's project. We now also include a couple of parasitic elements: ESR of output capacitor, $r_C = 50m\Omega$ and the ESR of the inductor, $r_L = 250m\Omega$. The load should be represented by a current source which is stepped from 0.1A to 5A. (The input voltage will also be stepped as outlined in the "deliverables" handout to assess input source disturbance response). Also to avoid DCM operation use a two quadrant switch implementation in your simulation.

Three designs should be presented:

1) Voltage mode droop control as presented in the paper "Design Considerations for VRM Transient Response Based on the Output Impedance" by K. Yao et. al.

2) Current mode droop control as presented in the paper "Optimal Design of the Active Droop Control Method for the Transient Response", by K Yao et. al.

3) To compare the effectiveness of the above two design approaches a third design should be implemented. Design a compensator based on the approach given in the "Notes for single loop feedback" handout posted on the class website. Note your design needs to take into consideration any poles/zeros that the parasitic elements have introduced. This design is typical of a single loop approach that aims to produce a zero output impedance converter.

Report: The specific deliverables that need to be handed in are outlined in a separate handout.