# *ECE446/546*

## *Project – Converter and control design for Converter C1 and a Buck converter with input filter*

**Aim:** To design a switching regulator which uses converter C1 and compare its performance with a Buck regulator for which an input filter has been designed. The performance of each is compared through simulation.

Both the power stage and the feedback loop frequency compensation for converter C1 regulator need to be designed. The following specifications are to be met:

$V_g$ = 28*V*, *V*= 15*V*, $V_M$ =*4V* ($V_M$ is the peak-to-peak amplitude of the sawtooth waveform used in the *PWM* modulator), feedback resistive divider gain is *1/3* (use resistor values: *2K* and *1K*) and $f_s$ = 100*kHz*. The maximum and minimum load currents are *5A* and *0.3A*, respectively. A one quadrant switch implementation is to be used. Also include parasitic elements: ESR of capacitors, and the ESR of the inductors.

An evaluation of the efficacy of the frequency compensation will be made by the nature of the step response of the input voltage, from *28 V* to *30V* and from *30V* to *28V*

Be sure to show the PECS schematics and the corresponding step input voltage response simulations. Also, include in an appendix all Matlab code used.

**Report:** Your report should be written in the form of a technical paper. So choose a suitable title and write your paper in the usual technical paper format: abstract, introduction, various intermediate sections, conclusion and references. Use a one column per page format. Your presentation should be self-contained, thus provide all appropriate design details, equations etc. in your report.

**Grading**: Grading will be based heavily on the level of compliance with the requirements given above as well as the professionalism in your written content and written presentation.

Further discussion on the content on the report is given on the next page

Your report should include the following:

**For C1 design:**

- Your design procedure used to determine the *L* and *C* values in converter C1. This involves satisfaction of a number of competing requirements:
  - Avoidance of DCM (discontinuous current mode).
  - Avoidance of DVM (discontinuous voltage mode).
  - Acceptable current ripple in the inductors under full load conditions.
  - Output voltage ripple.
  - Avoidance of RHP zero.
  - Convenience of having symbolic denominator factorization.

  Note these requirements come from
  i. steady state operating conditions
  ii. small-signal properties
- Derivation of the steady-state, first-order ripple and second-order ripple state vectors. For simplicity, have no parasitics present.
- Derivation of the control-to-output voltage transfer function. For simplicity, have no parasitics present.
- The resulting transfer function features a $4^{th}$ order denominator and a $2^{nd}$ order numerator. To make sense of the denominator it is symbolically factored. This factorization involves certain restrictions on the component values. Present the derivation of this factorization in an appendix which leads to the final component constraints.
- For your chosen component values, compare on a Matlab Bode plot (magnitude and phase) on the same graph the unfactored and the factorized responses to confirm the validity of your results.
- Use your factorized transfer function to approximately determine the location of any poles and zeros introduced by inclusion of the *ESR* for each *L* and *C*.
- Check that all constraints are met by the actual component values used in your design.
- Show the input step response by simulation on PECS.

**For Buck converter with input filter design:**

- The Buck power stage should feature a single quadrant switch implementation.
- Design an input filter where the components have been determined optimally as seen in the class notes.
- Provide input step responses for the following three cases:
    i. Buck regulator, no input filter.
    ii. Buck regulator with input filter and no damping.
    iii. Buck regulator with input filter with proper damping.