Applied Classical and Modern Control System Design

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Preface

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Contents

Part I

Classical Control

Chapter 1

Introduction

1.1 Introduction(ADD CONTENT)

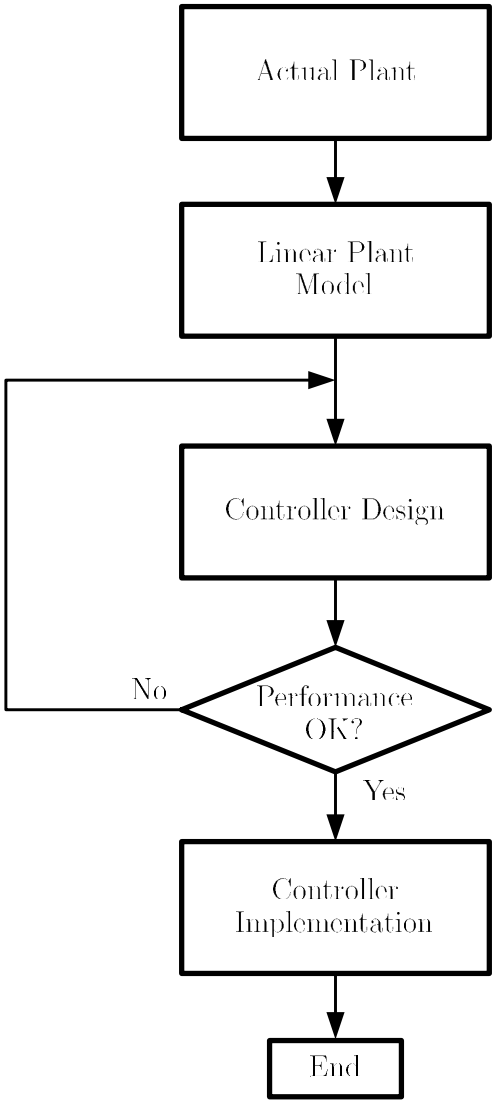


Figure 1.1: Design Flow Diagram

Chapter 2

The System

2.1 Introduction

In this chapter, the parameters for an example control system will be defined and derived. From the parameters of this example system, subsequent chapters will be devoted to applying control design techniques to optimize system performance parameters.

A control system begins with a model for plant, that has at least one particular parameter to be controlled. To control the plant, the parameter to be controlled is compared to a stable reference value and the difference is input to an error amplifier. The error amplifier then commands the plant, controlling the desired plant parameter. A basic diagram illustrating this architecture is shown in Figure 5.8.

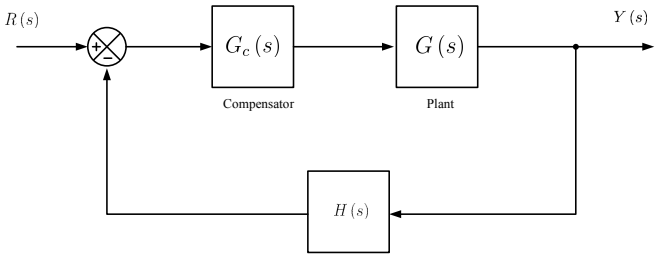


Figure 2.1: Feedback System Block Diagram

2.2 The Plant: Buck Converter

2.2.1 Introduction

The fundamental item in every control system is the plant, the item that is to be controlled. In this section, the plant will be defined as a buck converter, a switched mode DC power supply.

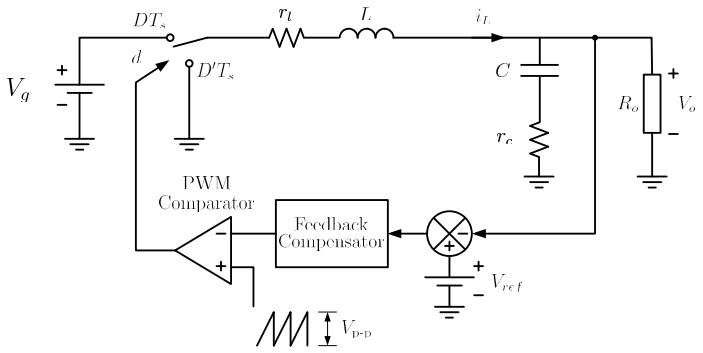


Figure 2.2: Buck Converter Circuit System Diagram

The buck regulator, which is shown complete in Figure 2.2 including circuit losses and feedback compensation, is a basic switched mode power supply. The buck regulator acts to reduce the steady state output voltage based on an applied duty cycle of applied input voltage. The duty cycle is switched at a frequency higher than the resonant frequency LC tank on the output. The output filter allows the circuit to convert the input voltage to a lower output voltage with minimal circuit losses.

The complete system block diagram for the buck regulator is shown in Figure 4.1. The output voltage of the system is fed back to a reference (reduced by $H(s)$), and the difference (error signal) is fed to a compensator which drives a pulse-width modulator to control the output voltage. Additionally, this model includes disturbance inputs in terms of step loading and input voltage variation for design characterization.

2.2.2 Transfer Function Derivations

To model the plant based on the diagram of Figure 4.1, three transfer functions are required to be derived. The transfer function are the control to output $G_{vd}(s)$, input voltage to output $G_{vg}(s)$, and the output current to output

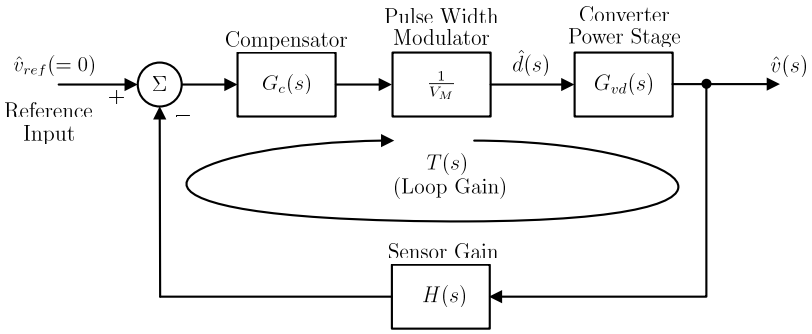


Figure 2.3: Simplified System Diagram

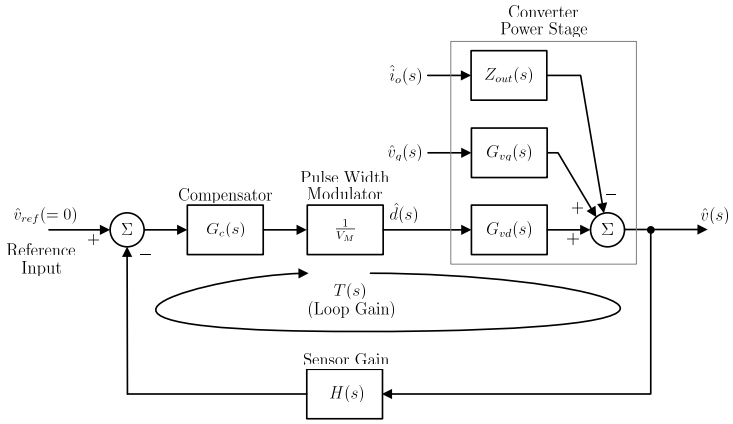


Figure 2.4: Generalized Power System Model

voltage, or open loop output impedance $Z_{out}(s)$. Additional transfer functions will be derived in the section, such as the control to inductor current $G_{id}(s)$, output current to inductor current $G_{ii}(s)$, and the input voltage to inductor current $G_{ivg}(s)$. These transfer functions will be utilized in following chapters.

Using the state space analysis approach, the complete set of transfer functions will be derived for the buck converter shown in Figure 2.5.

$G_{vd}(s)$ Analysis

To analyze the small signal control to output transfer function of the buck converter, an output load change is modeled with a current source, as shown in Figure 2.5. In terms of the state space analysis, this additional source will be modeled as another input variable to the system.

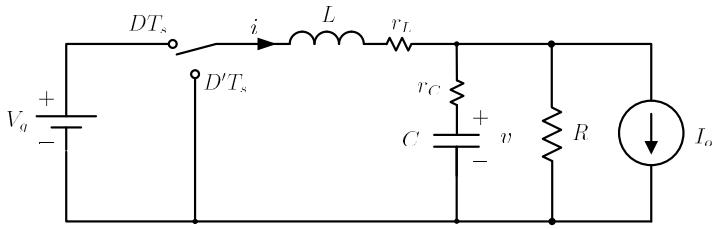


Figure 2.5: Buck Converter Circuit with Non-Ideal Circuit Elements

Listed below are the fundamental equations for state space analysis. x defines the state variables of the system and the u variables define the inputs. The number of states is defined by the number of storage elements in the system. For the buck converter, there are two states. The output voltage of the converter is the voltage across the capacitor and the corresponding parasitic resistance.

$$x = \begin{bmatrix} i \\ v \end{bmatrix}$$

$$u = \begin{bmatrix} v_g \\ i_o \end{bmatrix}$$

$$\dot{x} = Ax + Bu$$

$$y = Cx + Eu$$

Applying the principles of superposition to the buck converter, the capacitor current and inductor voltage equations are found and summarized below for both switch positions.

During DTs,

$$L\frac{\mathrm{d}i_L}{\mathrm{d}t} = -(r_l + r_c \,||\, R)i_L - \frac{R}{R + r_c}V_c + V_g + I_o\,(R \,||\, r_c)$$

$$C\frac{\mathrm{d}V_c}{\mathrm{d}t} = \frac{R}{R + r_c}i_L - \frac{1}{R + r_l}V_c + 0V_g - \left(\frac{R}{R + r_c}\right)I_o$$

$$V_{out} = (r_c \,||\, R)\, i_L + \frac{R}{R + r_c}V_c + 0V_g - (R \,||\, r_c)\, I_o$$

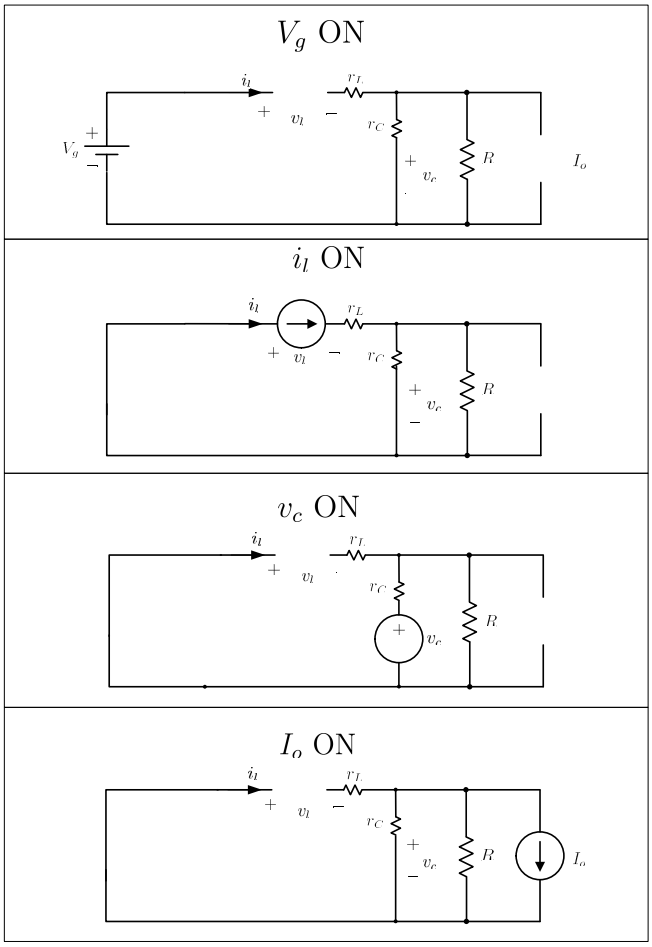


Figure 2.6: Buck Converter Superposition Analysis: DTs

During D'Ts,

$$L\frac{\mathrm{d}i_L}{\mathrm{d}t} = -(r_l + r_c \,||\, R)i_L - \frac{R}{R+r_c}V_c + 0V_g + I_o\,(R \,||\, r_c)$$

$$C\frac{\mathrm{d}V_c}{\mathrm{d}t} = \frac{R}{R+r_c}i_L - \frac{1}{R+r_l}V_c + 0V_g - \left(\frac{R}{R+r_c}\right)I_o$$

$$V_{out} = (r_c \,||\, R)\, i_L + \frac{R}{R+r_c}V_c + 0V_g - (R \,||\, r_c)\, I_o$$

With the circuit defined over the two subintervals, the A, B, C, and E matrices can be defined as shown below:

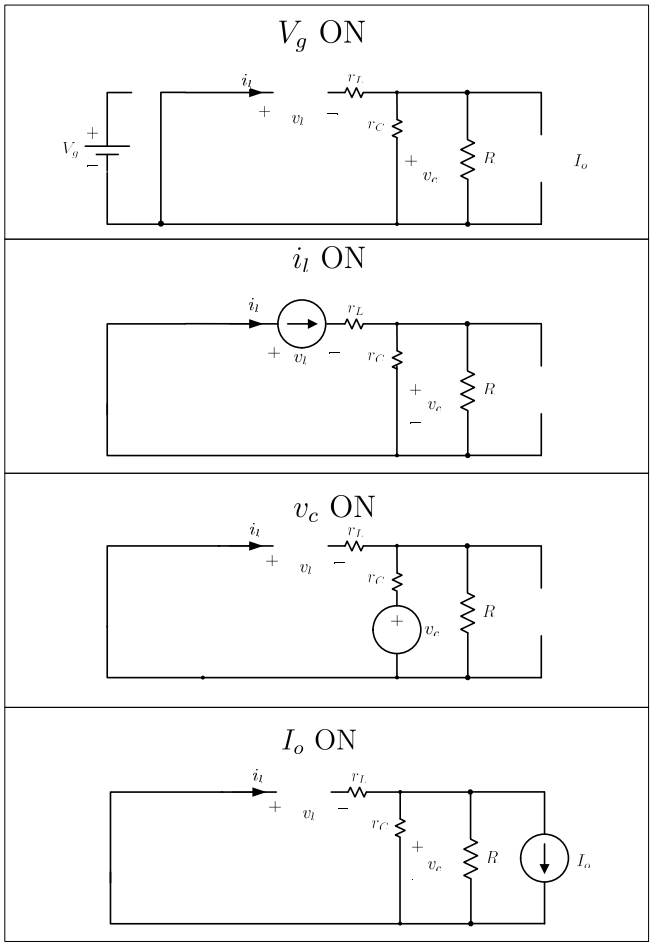


Figure 2.7: Buck Converter Superposition Analysis: D'Ts

$$A_1 = A_2 = A = \begin{bmatrix} -\frac{(r_c \| R + r_l)}{L} & -\frac{R}{(R+r_c)L} \\ \frac{R}{(r_c+R)C} & -\frac{1}{(r_c+R)C} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix}$$

$$C_1 = C_2 = C = \begin{bmatrix} (r_c \,||\, R) & \frac{R}{R+r_c} \end{bmatrix}$$

$$E_1 = E_2 = E = \begin{bmatrix} 0 & -(r_c \,||\, R) \end{bmatrix}$$

With the state space matrices defined, the control to output transfer function can be calculated as $G_{vd}(s) = C(sI - A)^{-1}Bd + Ed$, where $B_d = (A_1 - A_2)X + (B_1 - B_2)U$ and $E_d = (C_1 - C_2)X + (E_1 - E_2)U$. Applying basic matrix manipulation techniques, $G_{vd}(s)$ is calculated below.

$$X = -A^{-1}BU = \begin{bmatrix} \frac{DVg}{R+r_l} - Io\left(\frac{R^2}{(R+r_c)(R+r_l)} - \frac{Rr_c}{(R+r_c)(R+r_l)}\right) \\ Io\left(\frac{R^2 r_c}{(R+r_c)(R+r_l)} + \frac{R(Rr_c+Rr_l+r_c r_l)}{(R+r_c)(R+r_l)}\right) + \frac{DRV_g}{R+r_l} \end{bmatrix}$$

$$B_d = (A_1 - A_2)X + (B_1 - B_2)U = \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix}$$

$$E_d = (C_1 - C_2)X + (E_1 - E_2)U = 0$$

$$G_{vd}(s) = C(sI-A)^{-1}Bd+Ed = \frac{V_g\,(1 + sRC)}{\frac{r_c+R}{R}s^2LC + s\left(\frac{L}{R} + \left(r_l + r_c + \frac{r_c r_l}{R}\right)C\right) + \frac{(R+r_l)}{R}}$$

$G_{ii}(s)$ Analysis

When calculating the output load to inductor current transfer function, it can be noticed that the inductor voltage and capacitor current equations will be identical to those used in calculating $G_{vd}(s)$ above. Using this fact, only the output equation is needed to be derived to find the C and E matrices.

$$y = i$$

$$C_1 = C_2 = C = \begin{bmatrix} 1 & 0 \end{bmatrix}$$

$$E_1 = E_2 = E = \begin{bmatrix} 0 & 0 \end{bmatrix}$$

Using the values found above, the output load to inductor current function is equal to $G_{ii}(s) = -(C(sI - A)^{-1}B + E)$, with the negative sign due to the defined current direction.

$$G_{ii}(s) = C(sI-A)^{-1}B+E = \frac{\left(\frac{R-r_c}{R+r_l} + sr_cC\right)}{\frac{r_c+R}{R}s^2LC + s\left(\frac{L}{R} + \left(r_l + r_c + \frac{r_c r_l}{R}\right)C\right) + \frac{(R+r_l)}{R}}$$

$G_{id}(s)$, $G_{vv_g}(s)$, and $G_{iv_g}(s)$ Analysis

To calculate $G_{id}(s)$, the control to inductor current transfer function, $G_{vv_g}(s)$, the input voltage to output voltage transfer function and $G_{iv_g}(s)$, the input voltage to inductor current transfer function, the same parameters derived above can be used to solve each equation.

$$G_{id}(s) = C(sI-A)^{-1}Bd+Ed = \frac{V_g}{R}\frac{(1+s(R+r_c)C)}{\frac{r_c+R}{R}s^2LC+s\left(\frac{L}{R}+\left(r_l+r_c+\frac{r_cr_l}{R}\right)C\right)+\frac{(R+r_l)}{R}}$$

$$G_{vv_g}(s) = C(sI-A)^{-1}B+E = \frac{D(1+sr_cC)}{\frac{r_c+R}{R}s^2LC+s\left(\frac{L}{R}+\left(r_l+r_c+\frac{r_cr_l}{R}\right)C\right)+\frac{(R+r_l)}{R}}$$

$$G_{iv_g}(s) = C(sI-A)^{-1}B+E = \frac{\frac{D}{R}(1+s(R+r_c)C)}{\frac{r_c+R}{R}s^2LC+s\left(\frac{L}{R}+\left(r_l+r_c+\frac{r_cr_l}{R}\right)C\right)+\frac{(R+r_l)}{R}}$$

$Z_o(s)$ Analysis

To calculate the output impedance of the Buck converter, it is possible to use state space analyses techniques. However, due to the input voltage connection of the Buck converter we can take advantage of the fact that the impedance of the buck on the output looks the same regardless of the switch location.

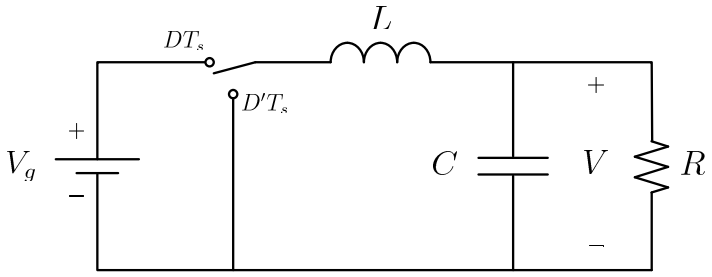


Figure 2.8: Ideal Buck Converter Circuit

$$Z_o(s) = SL\|\frac{1}{sC}\|R = \frac{sL}{1+s\frac{L}{R}+s^2LC}$$

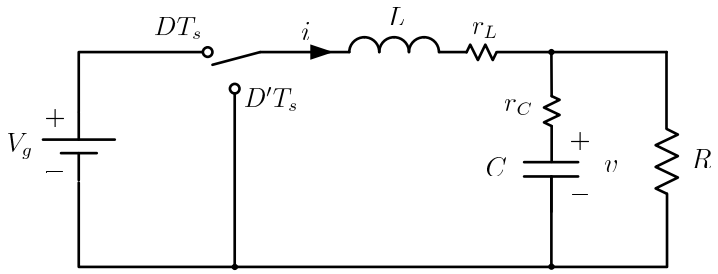


Figure 2.9: Buck Converter Circuit with Non-Ideal Circuit Elements

One way to incorporate losses into the impedance function is to replace the energy storage element in the impedance equation with the sum of the element and its non-ideal resistive component. Starting with the inductor, every instance of sL is replaced with $sL + r_l$ in $Z_o(s)$.

$$Z_o(s) = \frac{sL + r_l}{1 + \frac{r_l}{R} + s\left(\frac{L}{R} + r_l C\right) + s^2 LC}$$

Assuming $\frac{r_l}{R} << 1$

$$Z_o(s) = \frac{sL + r_l}{1 + s\left(\frac{L}{R} + r_l C\right) + s^2 LC}$$

Now, adding the ESR of the capacitor:

$$sC \Rightarrow \frac{sC}{1 + SR_c}$$

$$Z_o(s) = \frac{(sL + r_l)(1 + sr_c C)}{1 + s\left(\frac{L}{R} + (r_l + r_c)C\right) + s^2\left(1 + \frac{r_c}{R}\right)LC}$$

The complete output impedance of the Buck converter is found to be:

$$Z_o(s) = \frac{r_l\left(1 + s\frac{L}{r_l}\right)(1 + sr_c C)}{1 + s\left(\frac{L}{R} + (r_l + r_c)C\right) + s^2 LC}$$

Assuming $(\frac{r_c}{R} << 1)$.

To summarize the results of this section, Figure 2.10 shows the results of the state space analysis for the buck converter presented in this chapter. The results of the analysis will be leveraged throughout the text.

Buck Converter Transfer Functions		
	Ideal Case	Losses Included
	$Q = \frac{R}{l}\sqrt{LC}$ $r_l = 0$ $\omega_0 = \frac{1}{\sqrt{LC}}$ $r_c = 0$	$Q = \frac{\sqrt{LC}}{(r_c+r_l)C+\frac{L}{R}}$ $r_l \neq 0,$ $\frac{r_l}{R} << 1$ $\omega_0 = \frac{1}{\sqrt{LC}}$ $r_c \neq 0,$ $\frac{r_c}{R} << 1$
	$\triangle(s) = 1 + \frac{s}{\omega_0 Q} + \left(\frac{s}{\omega_0}\right)^2$	
$G_{vd} \triangleq \frac{\hat{v}}{\hat{d}}$	$\frac{V_g}{\triangle(s)}$	$\frac{V_g(1+sr_cC)}{\triangle(s)}$
$G_{vv_g} \triangleq \frac{\hat{v}}{\hat{v_g}}$	$\frac{D}{\triangle(s)}$	$\frac{D(1+sr_cC)}{\triangle(s)}$
$Z_{out} = G_{vi_o} \triangleq \frac{\hat{v}}{\hat{i_o}}$	$\frac{sL}{\triangle(s)}$	$\frac{r_l\left(1+\frac{sL}{R}\right)(1+sr_cC)}{\triangle(s)}$
$G_{id} \triangleq \frac{\hat{i}}{\hat{d}}$	$\frac{\frac{V_g}{R}}{\triangle(s)}$	$\frac{\frac{V_g}{R}(1+sRC)}{\triangle(s)}$
$G_{iv_g} \triangleq \frac{\hat{i}}{\hat{v_g}}$	$\frac{\frac{D}{R}(1+sRC)}{\triangle(s)}$	$\frac{\frac{D}{R}(1+sRC)}{\triangle(s)}$
$G_{ii_0} \triangleq \frac{\hat{i}}{\hat{i_0}}$	$\frac{1}{\triangle(s)}$	$\frac{(1+sr_cC)}{\triangle(s)}$

Figure 2.10: Summary of Plant Transfer Functions

2.3 Pulse-width Modulator

With a complete model in place for the Buck regulator, the next item in the system diagram to derive is the pulse-width modulator.

From inspection of Figure 2.11, it can be approximated that the duty cycle can be represented by the following relationship:

$$d(t) = \frac{V_c(t)}{V_M} \text{ for } 0 \leq V_c(t) \leq V_M$$

Rearranging, $\frac{d(t)}{V_c(t)} = \frac{1}{V_M}$. For a complete derivation confirming the PWM conversion gain can be approximated to this equation, refer to the analysis presented in [?].

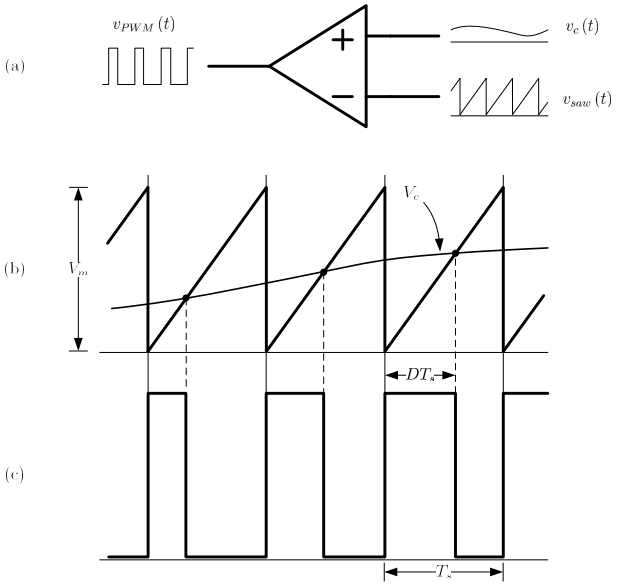


Figure 2.11: PWM Conversion Diagram

2.4 Summary

Now that the basic system has been defined, the final block to be derived in the Buck converter system model is the compensator, $G_c(s)$. The compensator will be the primary topic of the next several chapters, as it will be leveraged to improve the closed-loop performance of the derived buck regulator system. The equations in this chapter will be heavily leveraged in the remainder of the text.

Bibliography

[1] M. Xu K. Yao and F. Lee. Design considerations for vrm transient response based on the output impedance. *IEEE*, 18(6):1270–1277, November 2003.

[2] M. Xu K. Yao, K. Lee and F. Lee. Optimal design of the active droop control method for the transient response. *IEEE*, pages 718–723, 2003.

[3] RD Middlebrook. Predicting modulator phase lag in pwm converter feedback loops. *Powercon*, 1981.

Chapter 3

Bode Plots

Introduction

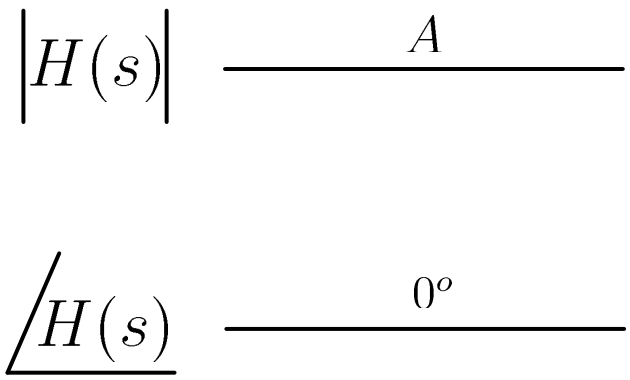


Figure 3.1: Simple Gain

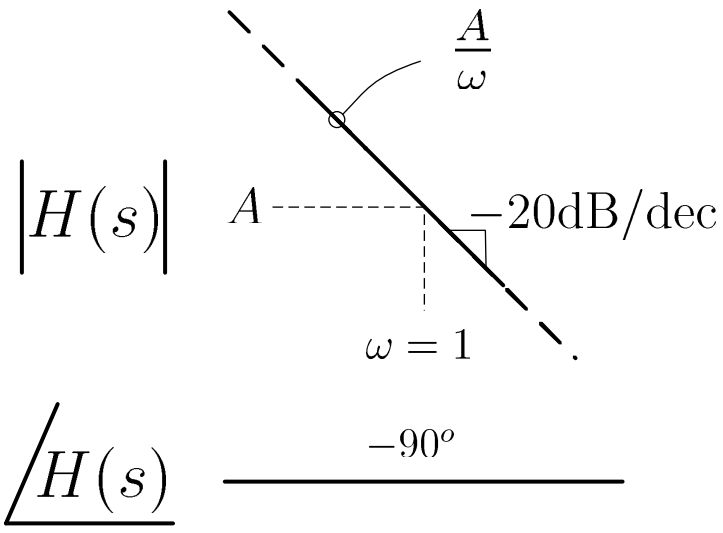


Figure 3.2: Pole at Zero

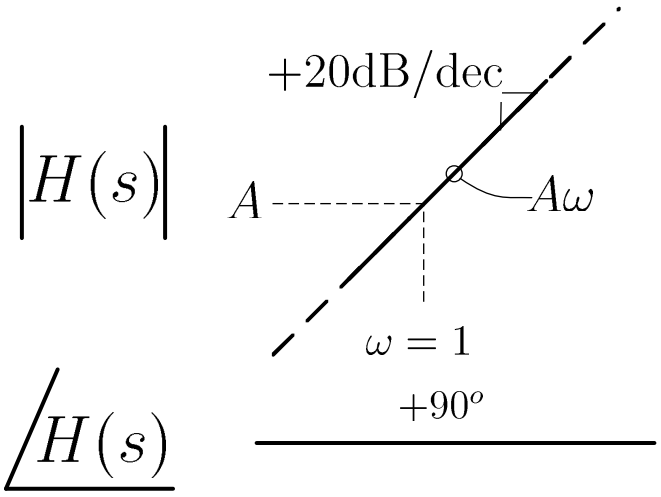
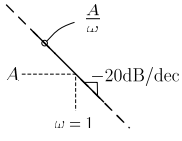
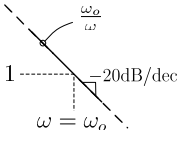


Figure 3.3: Zero at Zero

3.0.1 Bode Plots

$H(s) = A$	$\lvert H(s)\rvert$ — A
Simple Gain	$\angle H(s)$ — 0^o
$H(s) = \frac{A}{s}$	$\lvert H(s)\rvert$  Or: $H(s) = \frac{\omega_o}{s}$, $\omega_o = A$ $\lvert H(s)\rvert$ 
Pole at Zero	$\angle H(s)$ — -90^o
$H(s) = As$	 $H(s) = \frac{s}{\omega_o}$ 

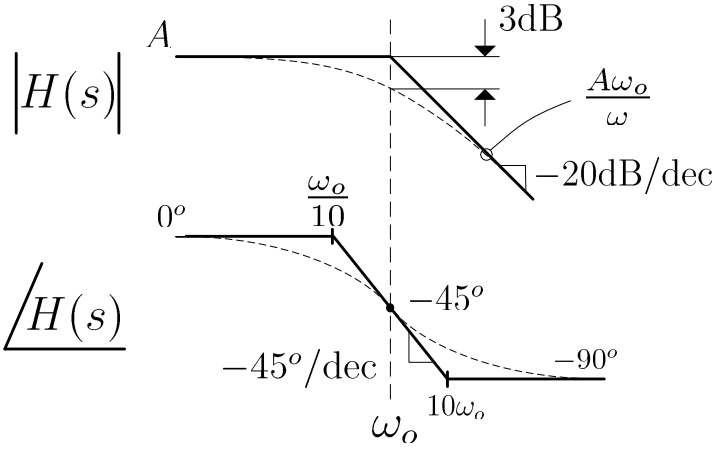


Figure 3.4: Pole at ω_o

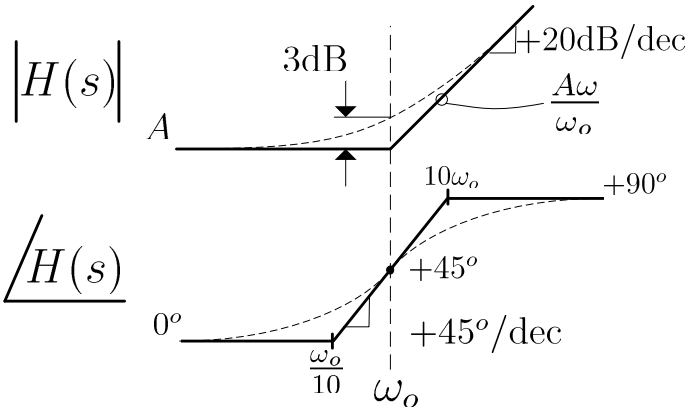


Figure 3.5: Zero at ω_o

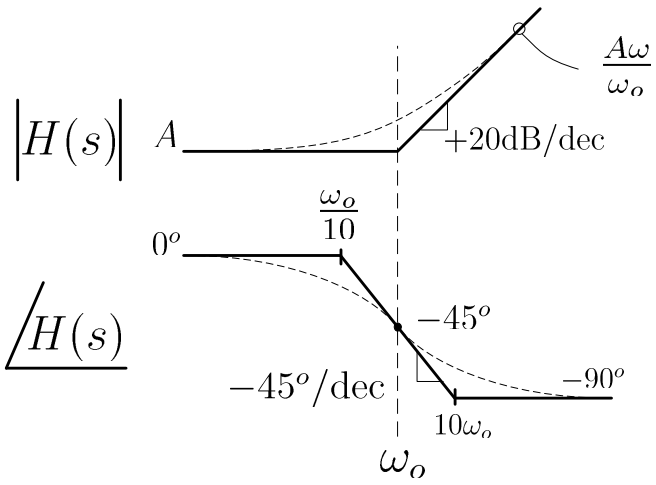


Figure 3.6: Right Half Plane Zero at ω_o

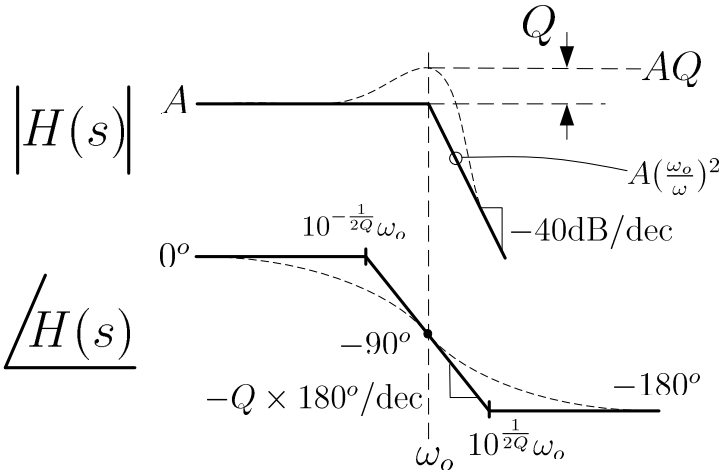


Figure 3.7: Second Order Complex Pole at ω_o

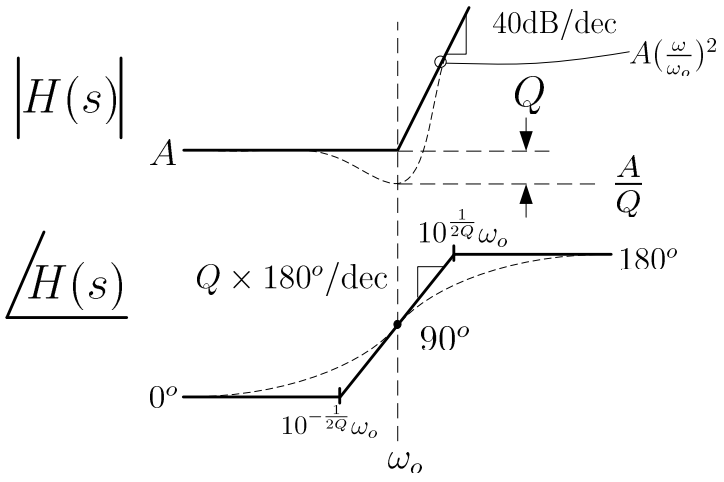


Figure 3.8: Second Order Complex Zero at ω_o

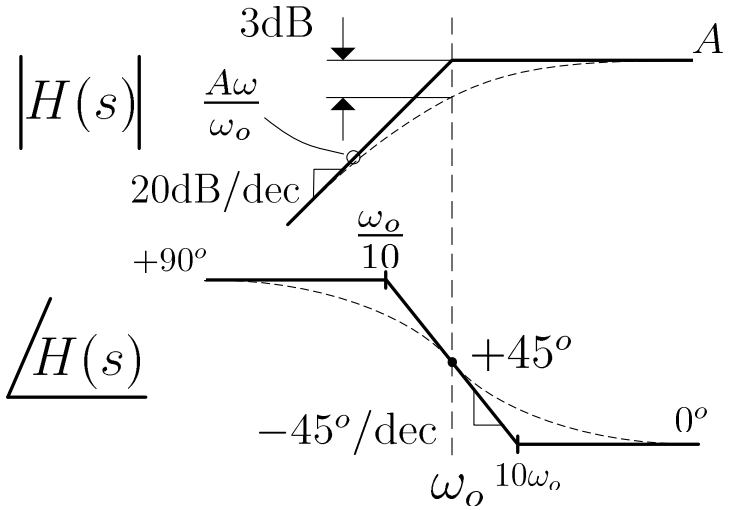


Figure 3.9: Inverted Pole at ω_o

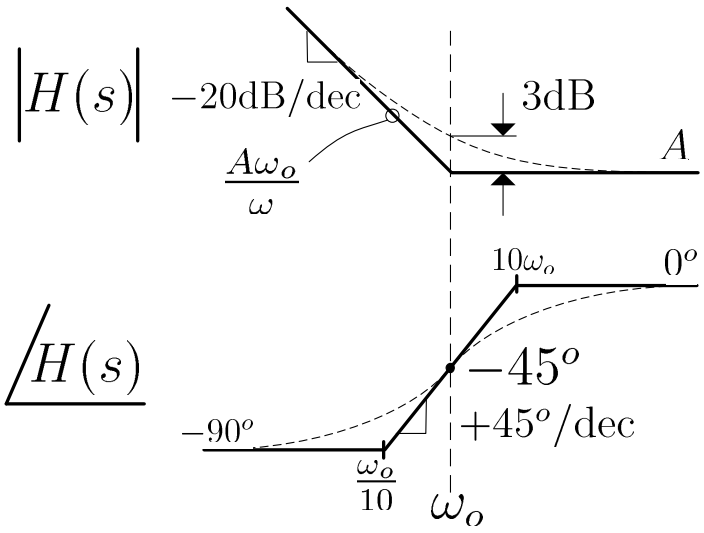
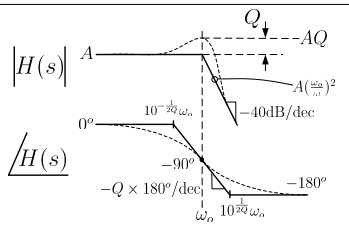
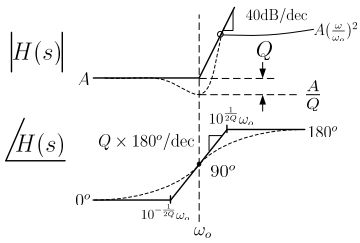


Figure 3.10: Inverted Zero at ω_o

$H(s) = \frac{A}{1+\frac{s}{Q\omega_o}+\left(\frac{s}{w_o}\right)^2}$ Second Order Complex Pole		ω_o=Corner Frequency $Q > \frac{1}{2} \implies$ Complex Roots Q=Quality Factor: Exact Gain @ ω_o Approximate Maximum Value Exact Phase: $-tan^{-1}\left[\frac{\frac{1}{Q}\frac{\omega}{\omega_o}}{1-(\frac{\omega}{\omega_o})^2}\right], \forall\omega$
$H(s) = A\left(1+\frac{s}{Q\omega_o}+\left(\frac{s}{w_o}\right)^2\right)$ Second Order Complex Zero		ω_o=Corner Frequency $Q > \frac{1}{2} \implies$ Complex Roots Exact Phase: $tan^{-1}\left[\frac{\frac{1}{Q}\frac{\omega}{\omega_o}}{1-(\frac{\omega}{\omega_o})^2}\right], \forall\omega$
		Maximum Error @ ω_o = 3dB

Chapter 4

Single Loop Voltage Mode Control

This paper develops a buck converter design example using different compensation methods to ensure closed loop stability and to optimize system performance. Various compensators are designed using asymptotic Bode plots based primarily on loop bandwidth and stability margins. Computer simulation results are included to show time domain step response behavior and to verify performance improvements.

4.1 Introduction

The buck converter is a switch mode, DC-DC, power supply. It accepts a source voltage, V_g and produces a lower output voltage, V with high efficiency. An important component of a practical buck converter is control feedback which assures a constant output voltage and attenuates unwanted disturbances. The feedback loop of a buck converter presents several challenges which are explored in the compensation examples.

In this paper we present a series of example buck converter feedback compensation approaches. The design of the buck converter circuit is kept constant to allow comparison of the effects of different compensation schemes. The primary tool that will be applied to evaluate the different compensation approaches are asymptotic Bode plots which are drawn based on corner frequencies of each block in the regulator system. This methodology provides a quick and efficient assessment of circuit performance and an intuitive sense for the trade offs for each compensation approach. Bode plots also directly illuminate the two critical loop stability characteristics, gain and phase margin (GM and PM respectively).

Additional analysis of each compensation approach is undertaken through computer simulation. The PECS [1] circuit simulator is used to evaluate the

effects of V_g transients, a common problem in real power supply designs. A Matlab [2] simulation is also performed to validate the manual Bode analysis and to determine the exact gain and phase margin. Finally a closed loop Matlab simulation is used to show the ability of the feedback system to attenuate undesired effects as a function of frequency.

4.2 Buck Converter System Models

4.2.1 General Model

Figure 4.1 is a block diagram of the system components of a buck converter with feedback. The converter power stage accepts V_g as its power source and the control input $d(s)$ to produce the output voltage V. The feedback sensor $H(s)$, monitors the converter output voltage which is then compared with a reference voltage V_{ref}. The difference output of these two voltages is provided to the feedback compensation circuit $G_c(s)$ and then to the pulse width modulator (PWM) which produces the control waveform for the switching converter $d(s)$. THe resulting loop gain is thus given by

$$T(s) = G_c(s)\left(\frac{1}{V_M}\right)G_{vd}(s)H(s) \tag{4.1}$$

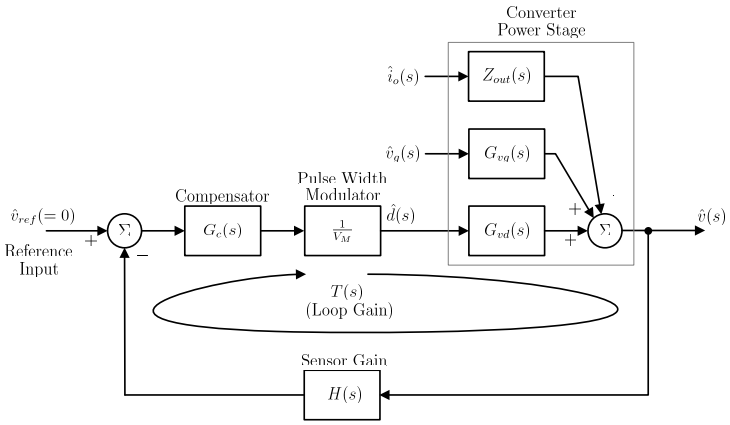


Figure 4.1: Generalized Power System Model

4.2.2 Simplified System Model

The general buck converter block diagram provides a complete model for analysis of converter. However, for our analysis we will use a simplified model show in Fig. 4.2 which includes only the elements required for the analysis we will provide. We do not evaluate any source of disturbance except V_g transients.

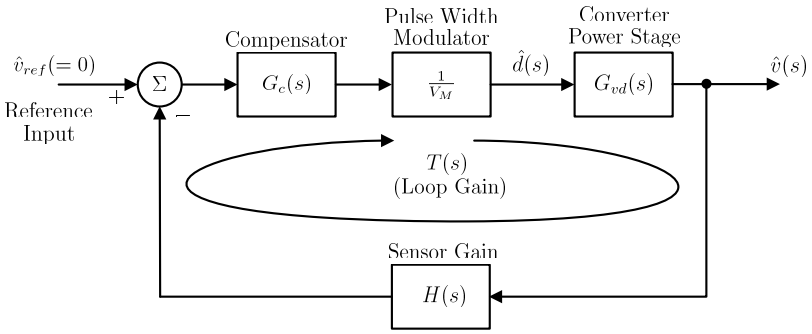


Figure 4.2: Simplified System Diagram

4.2.3 Design Targets

To facilitate easy comparison between the selected compensation schemes, the design of the buck converter is fixed with specified values. These values are specified in Table 4.1.

Table 4.1: Specified values

Name	Value	Description
V_g	28V	Input Voltage
V	15V	Output Voltage
I_{load}	5A	Load current
L	50uH	Buck inductor value
C	500uF	Buck capacitor value
V_m	4V	PWM ramp amplitude
$H(s)$	1/3	Sensor gain
f_s	100kHz	PWM frequency

4.2.4 Buck Converter Model Analysis

Figure 4.3 shows a schematic model for the power converter block. The LCR is a second order circuit with a transfer function described by equation (4.2). It has a resonant frequency value, $\omega_o = 6.28$k rad/s or $f_o(= \frac{\omega_o}{2\pi}) = 1.0$ kHz from (4.3) and a Q of 9.5 from (4.4). The low frequency gain of the converter is equal to V_g which is specified to be 28V.

$$G_{vd}(s) = V_g \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{4.2}$$

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{4.3}$$

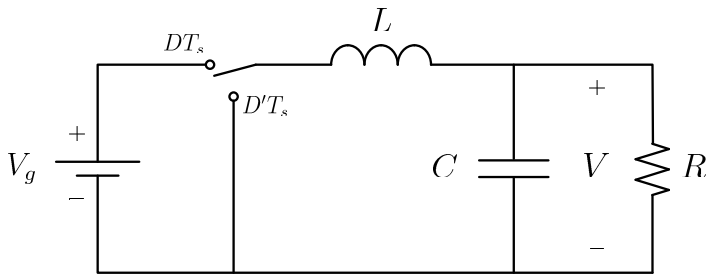


Figure 4.3: Converter Power Stage

$$Q = R\sqrt{\frac{C}{L}} \tag{4.4}$$

Consider the transfer function $v(s)/v_d(s)$ of the low pass filter formed by the LCR network. The switching frequency $f_s = 100$kHz is much higher than the resonant frequency $f_0 = 1$kHz of the LCR network. During circuit operation, the switch toggles the LCR input between V_g and ground with a duty cycle D determined by the feedback loop. A Fourier analysis of the LCR input waveform includes an average DC component $V = DV_g$ and an f_s fundamental component and its harmonics as typified by a rectangular waveform. The LCR acts as a low pass filter with a cut off frequency equal to f_o. It passes the DC component to the output but attenuates f_s and its harmonics.

4.3 Uncompensated System

It is instructive to start our evaluation with an uncompensated open loop converter, one with a $G_c(s) = 1$. The loop gain is then given from (4.1) as

$$T(s) = \frac{T_o}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_o}\right)^2} \tag{4.5}$$

where

$$T_o = \frac{V_g H(0)}{V_m} \tag{4.6}$$

To construct a Bode plot we use the values from equations (4.2)-(4.4) to establish the shape of the Bode magnitude plot. The low frequency gain given by (4.6) has a value of 2.33. The magnitude around f_o peaks due to the resonant Q of 9.5. At frequencies above f_o the gain declines at -40dB/decade.

The Bode phase plot is determined only by $G_{vd}(s)$. It has a low frequency phase shift of 0°. At $f_o 10^{-\frac{1}{2Q}}$ or 886Hz ($\approx$ 900Hz), the phase turns negative and at f_0 the phase has reached $-90°$. The phase continues to become more negative until it reaches $-180°$ at $10^{\frac{1}{2Q}}$ or 1129Hz ($\approx$ 1.1kHz). At frequencies higher than 1.1kHz the phase remains at $-180°$.

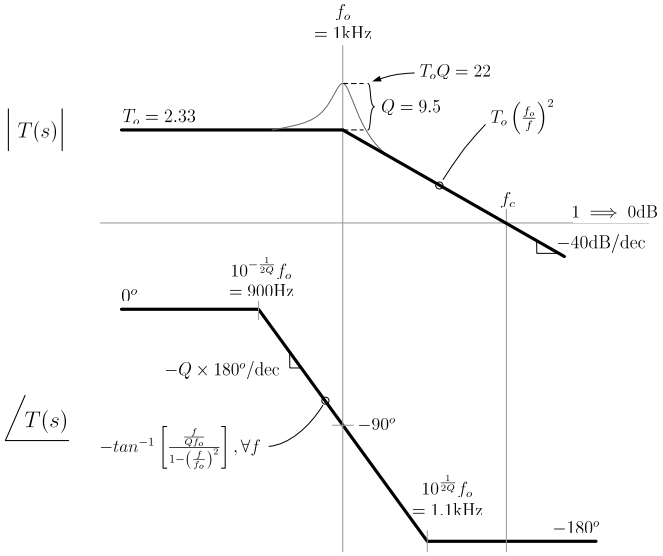


Figure 4.4: Uncompensated Gain and Phase Plot

From the Bode plot it can be determined that unity gain occurs at a frequency, $f = f_c$ such that

$$T_o \left(\frac{f_o}{f_c}\right)^2 = 1 \tag{4.7}$$

which with T_o=2.33 and f_o=1kHz, results in f_c=1.5kHz. At this frequency the phase is $-180°$ providing zero phase margin. The phase asymptotes show that phase does not cross the $-180°$ phase level (but is asymptotic to it) which implies that the gain margin is infinite. Figure 4.5 is a Matlab margin plot indicating the actual unity gain frequency to be 1.8 kHz with a phase margin of 4.7°. Also, the Matlab analysis indicates an infinite gain margin.

Figure 4.6 shows a PECS implementation of the open loop buck converter system. The input to the modulator is set to 2.1V which results in the target

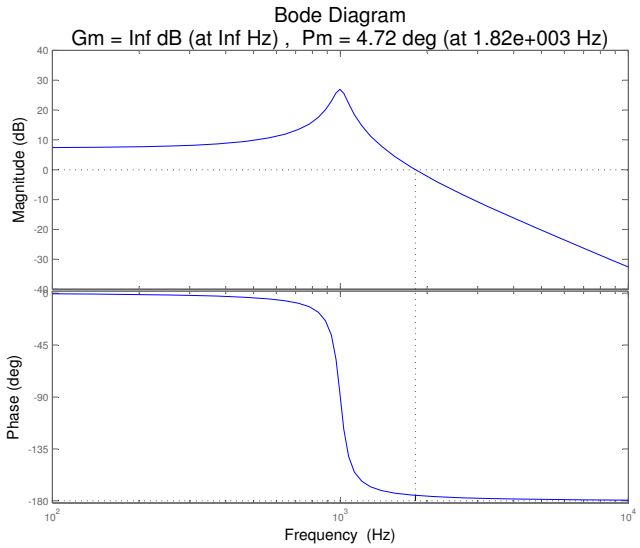


Figure 4.5: Matlab Uncompensated Bode plot

steady state duty ratio of $D = \frac{V}{V_g} = \frac{15}{28} = 0.54$ required to set the output voltage at $V = 15$V for a nominal input voltage of $V_g = 28$V.

Figure 4.7 shows the output voltage response of the open loop system shown in Figure 4.6 for voltage steps in V_g of 28V→30V→28V. The response is indicative of the high resonance Q of 9.5 at the resonant frequency f_o=1kHz. Note also that at an input voltage of V_g=30V the output voltage settles at $V = DV_g$ =0.54×30 = 16.2V, as shown in Fig. 4.7.

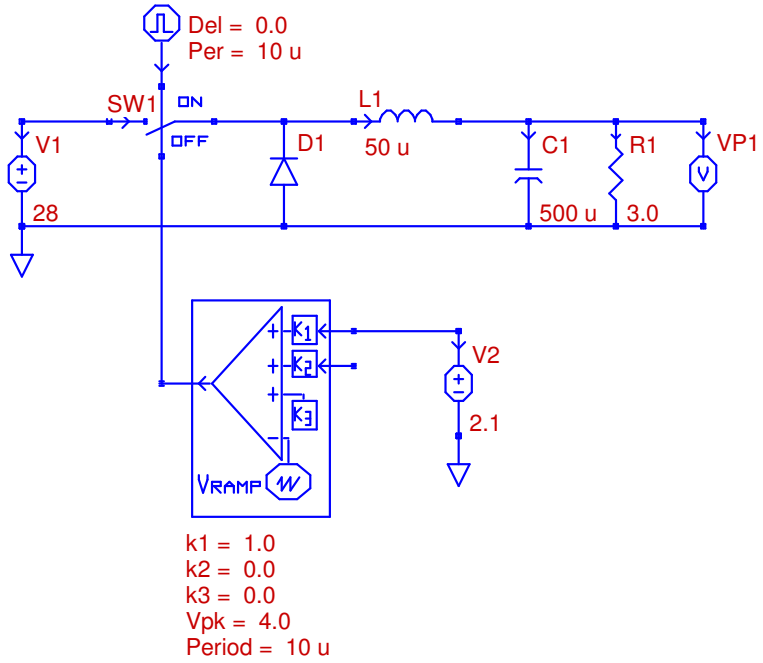


Figure 4.6: PECS Schematic of Open Loop System

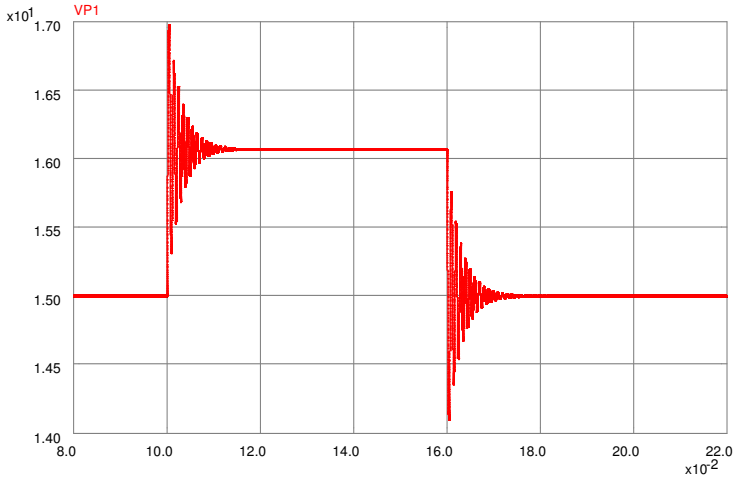


Figure 4.7: PECS Simulation of Open Loop System

4.4 Dominant Pole Compensation

Dominant pole compensation is one of the simplest and most common forms of feedback compensation. The motivating idea behind this type of feedback control is to shape the open loop gain of the system such that two objectives are achieved:

1. High gain is achieved at DC and low frequencies. This condition ensures low steady state error.
2. The gain at the plant's lowest frequency pole is less than or equal to 0dB. This condition ensures a positive phase margin and, consequently, stability.

In the case of dominant pole compensation, these objectives are achieved using a compensator consisting of a single pole at a frequency well below those of the plant's poles. For the purposes of this example, an integrator, which is just a pole at DC, is employed

$$G_c(s) = \frac{\omega_I}{s} \tag{4.8}$$

where $\omega_I (= 2\pi f_i)$ is an appropriately chosen design constant. Figure 4.8 shows the Bode plot asymptotes for the magnitude and phase of this compensator.

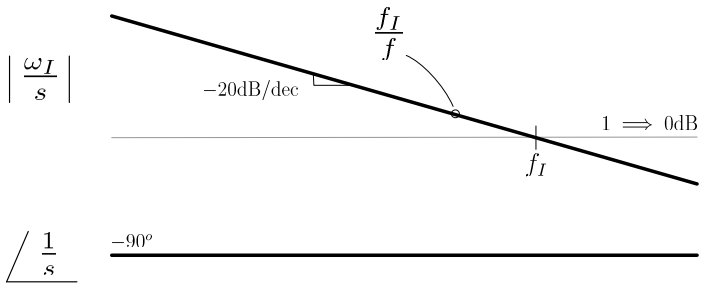


Figure 4.8: Bode Plot of Dominant Pole Compensator

Design of the compensator now consists of selecting an appropriate compensator parameter, f_I. Following the previously stated criteria, this is a matter of choosing the largest compensator gain such that the total gain at the lowest frequency plant pole(s) is less than 0dB. The loop gain of the system with this compensator is given by

$$T(s) = \frac{\omega_I T_o}{s\left[1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right]} \tag{4.9}$$

Figure 4.9 shows the graphical construction of the phase asymptotes for the loop gain with the compensator. Note that because the plant's dominant pole is second order, it contributes a phase shift of $-180°$ at high frequencies and a shift of exactly $-90°$ at f_o. Furthermore, the compensator contributes its own $-90°$ phase shift and does so for all frequencies. Consequently, the total phase shift of the compensated open loop transfer function is $-180°$ at the dominant pole frequency, f_o. For this reason it is prudent to design in some additional gain margin. A value of 3dB is initially chosen for this analysis.

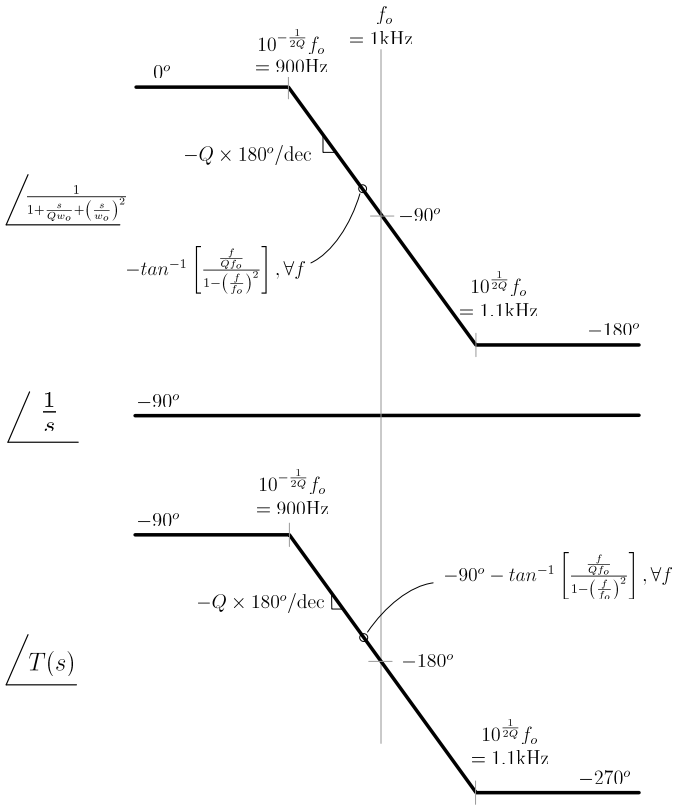


Figure 4.9: Graphical Construction of Phase Asymptotes for Dominant Pole Compensated Open Loop

Figure 4.10 shows how the plant and compensator transfer functions combine to produce the gain of the compensated open loop. To achieve a loop gain that is -3dB at f_o, we require the magnitude at f_o to equal 0.7

$$\frac{f_I T_o Q}{f_o} = 0.7 \tag{4.10}$$

For $T_o = 2.33$ and $f_o = 1.0$kHz, we find $f_I = 32$.

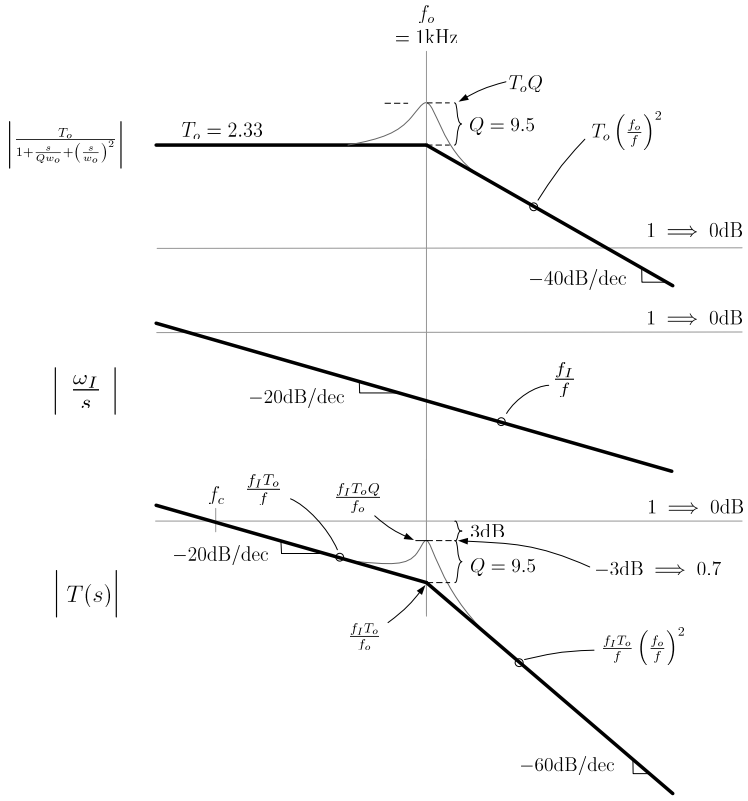


Figure 4.10: Graphical Construction of Gain Asymptotes for Dominant Pole Compensated Open Loop

Figure 4.11 shows the Bode plot of the resulting gain and phase asymptotes and Figure 4.12 shows a Matlab margin analysis which confirms the design.

With a compensator designed and verified via Matlab, the next stage is to design a circuit that implements the compensator. Figure 4.13 shows the general

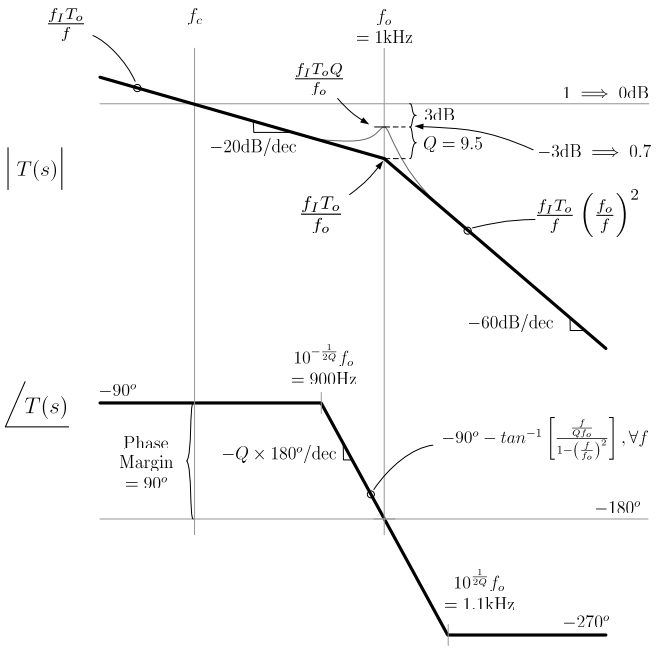


Figure 4.11: Open Loop System Gain and Phase with Dominant Pole Compensation

form of an operational amplifier in a integrator configuration. The transfer function for this circuit is given by:

$$G(s) = \frac{-1}{(s/\omega_o)} \tag{4.11}$$

where

$$\omega_o = \frac{1}{RC} \tag{4.12}$$

where ω_o is the frequency at which the integrator gain is unity.

A capacitor value of 50nF is chosen for C. This value is within the range of low-cost, commercially available ceramic capacitors and is small enough to avoid any op-amp slew rate issues. Equating ω_o with the compensator parameter, ω_I $(= 2\pi f_I)$ and solving for R gives

$$R = \frac{1}{\omega_I C} = \frac{1}{2\pi(32)(50\text{nF})} \approx 100\text{k}\Omega \tag{4.13}$$

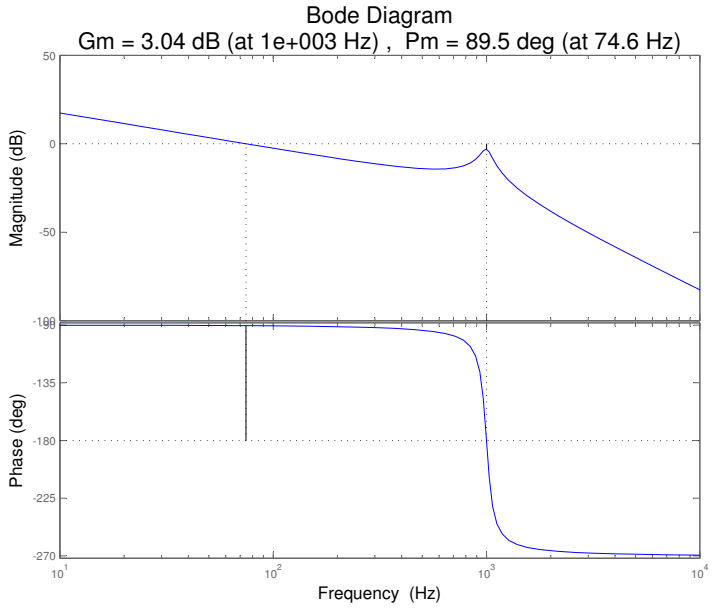


Figure 4.12: Matlab Analysis of Dominant Pole Compensator

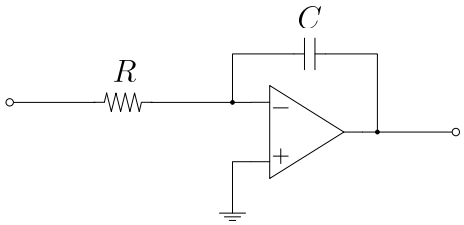


Figure 4.13: Op-Amp Integrator Circuit

A PECS simulation is created to verify the time domain performance of the implementation. Figure 4.14 shows the complete PECS circuit model for the design.

Figure 4.15 shows the results of the PECS simulation for a 2V disturbance on the supply voltage, V_g. The input voltage steps are 28V→30V→28V. The simulation exhibits several undesirable characteristics:

1. The regulator does a poor job of rejecting the input voltage disturbance. Nearly all of the input voltage excursion shows up as a transient on the output.

2. The regulator exhibits a substantial amount of ringing in response to the

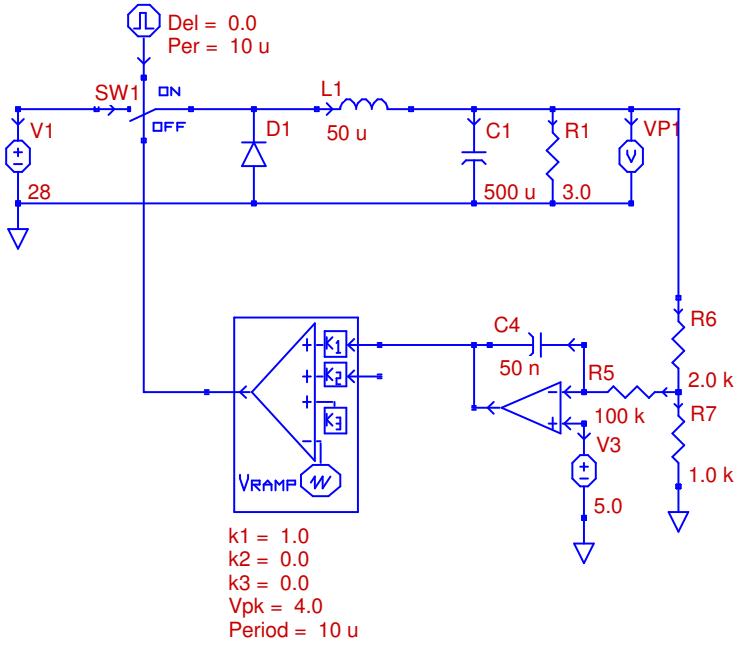


Figure 4.14: PECS Schematic of Dominant Pole Compensated System

input disturbance. Closer examination of the ringing, as shown in Figure 4.16, reveals that the frequency of the oscillations is the same as the resonant frequency of the plant, f_o, and is not the result of defective control loop design.

It is clear from the simulation results that, although the design is stable and exhibits zero steady-state error, there is much room for improvement, particularly with respect to its transient response.

One additional experiment is performed using the dominant pole compensation scheme. The Q of the plant's dominant pole is reduced by placing a large capacitor in series with a small damping resistance. Figures 4.17 and 4.18 show the PECS circuit schematic and simulation results, respectively.

One can see clearly that the ringing of the previous design has been eliminated. Unfortunately, the poor rejection of input voltage transients remains.

Furthermore, this is probably not an ideal solution from a practical standpoint. The large value capacitor will be relatively expensive in terms of com-

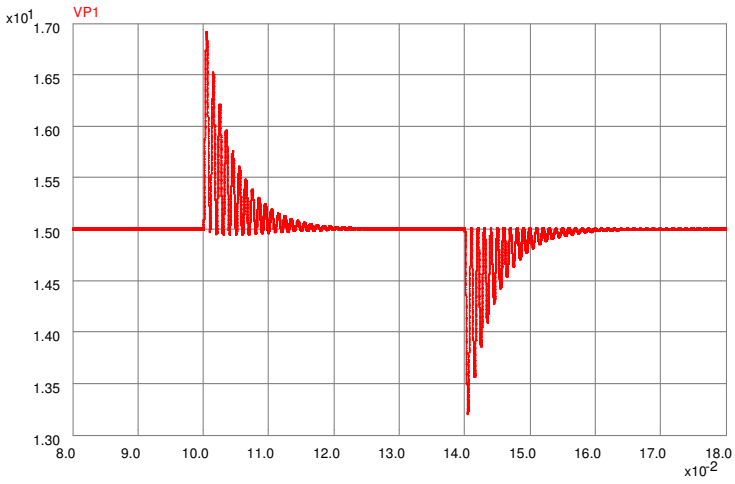


Figure 4.15: PECS Simulation of Dominant Pole

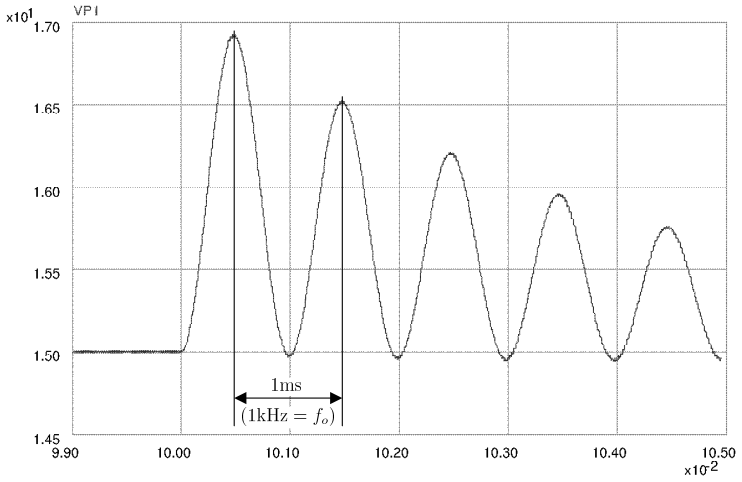


Figure 4.16: Pole of Dominant Pole Simulation Showing Oscillation at Resonant Frequency

ponent price and physical space. Alternate compensation schemes still offer the potential for better performance at lower cost.

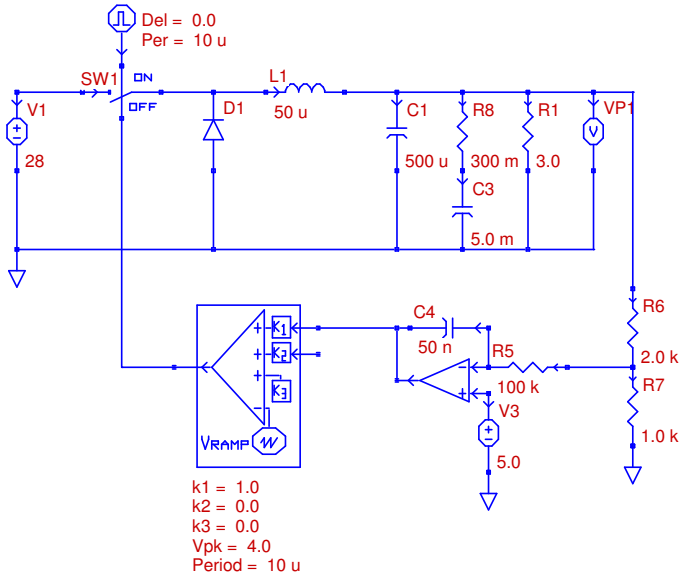


Figure 4.17: PECS Schematic of Dominant Pole with Damping

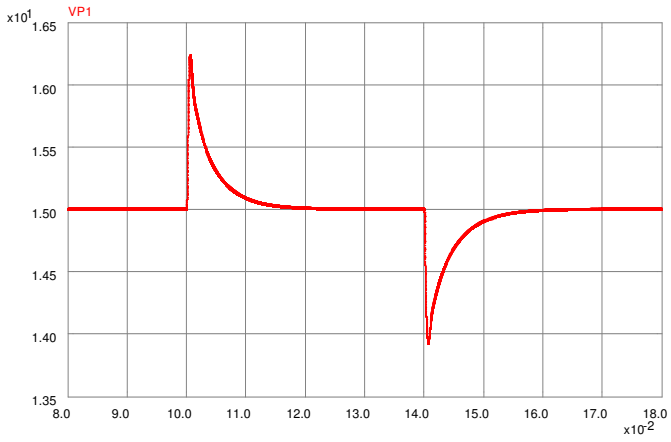


Figure 4.18: PECS Simulation of Dominant Pole with Zero Compensation and Damping

4.5 Dominant Pole Compensation with Zero

The dominant pole compensator of the previous section, while stable and having zero steady state error, exhibits several undesirable characteristics including poor rejection of input supply voltage excursions and pronounced ringing in response to transients. One might assume that these issues are related to the minimal, 3dB, gain margin for which the compensator was designed. This section explores that line of reasoning by modifying the compensator of the previous section in order to substantially increase the gain margin.

The dominant pole compensator is modified by adding a zero at the resonant frequency of the plant and by reducing the gain to -10dB. Overall gain margin is improved in two ways:

1. by directly increasing the gain margin at the resonant frequency, f_o, from 3dB to 10dB.
2. by shifting the frequency at which the phase reaches $-180°$ beyond the resonant frequency and the gain peak due to the plant's Q.

The form of the modified compensator transfer function is:

$$G_c(s) = \omega_I \frac{1 + s/\omega_z}{s} \tag{4.14}$$

We will use $\omega_z = \omega_o$ or $f_z \left(= \frac{\omega_z}{2\pi}\right) = f_o$. Which results in a loop gain of

$$T(s) = \omega_I \frac{1 + s/\omega_o}{s} \frac{T_o}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2} \tag{4.15}$$

Figure 4.19 shows the resulting Bode plot asymptotes. We would like to set the gain at f_o to $1/\sqrt{10}$ (which corresponds to -10dB). From the magnitude plot we see that we want

$$\frac{f_I T_o Q}{f_o} = \frac{1}{\sqrt{10}} \tag{4.16}$$

which given $T_o = 2.33$, $Q = 9.5$, $f_o = 1kHz$, results in $f_I = 14.3$. Figure 4.20 shows a Matlab confirmation of the Bode plot. Note that a gain margin of 11dB is predicted at a phase cross-over frequency of 1.06kHz, slightly higher than the plant's resonant frequency.

Figure 4.21 shows a standard op-amp implementation with the desired transfer function. The transfer characteristics of the circuit are given by:

$$G(s) = -A \frac{1 + s/\omega_1}{\frac{s}{\omega_1}} \tag{4.17}$$

where:

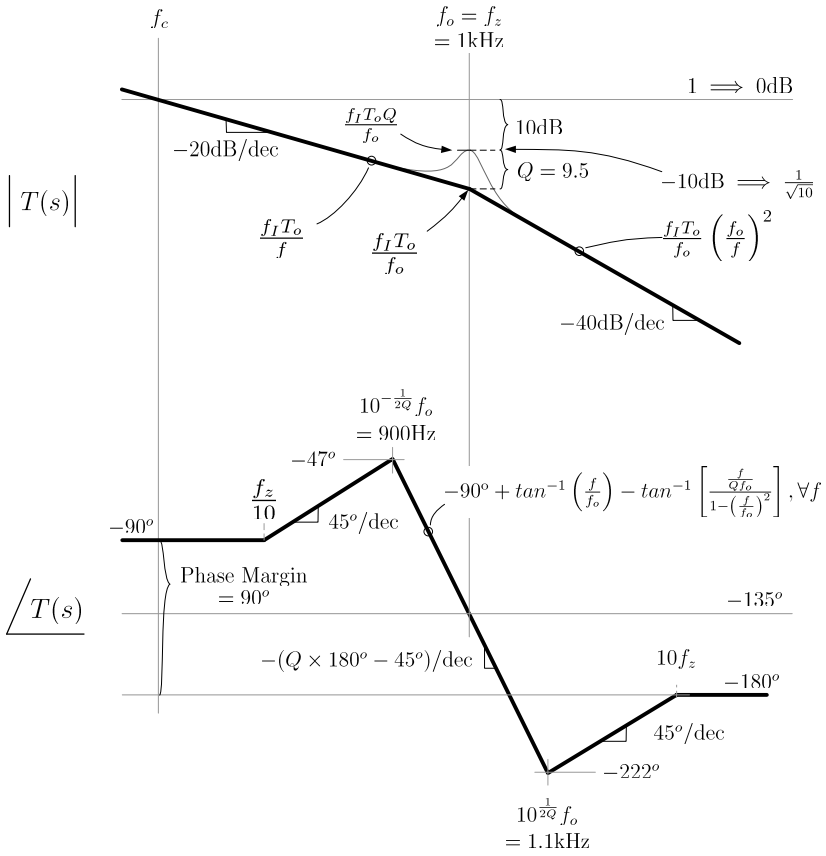


Figure 4.19: Open Loop System Gain and Phase with pole-zero Compensation (10dB GM)

$$A = \frac{R_2}{R_1} \quad \text{and} \quad \omega_1 = \frac{1}{R_2 C_1} \tag{4.18}$$

Equating $f_1 (= \frac{\omega_1}{2\pi})$ to the plant resonant frequency, f_o and ω_I to $A\omega_1$ provides two equations with three unknowns. Choosing, somewhat arbitrarily, a value of 100k for R1, leads to the following values.

$$R_2 = \frac{f_I R_1}{f_1} = \frac{(14.3)(100\text{k}\Omega)}{(1\text{k}\Omega)} = 1.4\text{k}\Omega \tag{4.19}$$

$$C_1 = \frac{1}{\omega_1 R_2} = \frac{1}{2\pi(1\text{kHz})(1.4\text{k}\Omega)} = 110\text{nF} \tag{4.20}$$

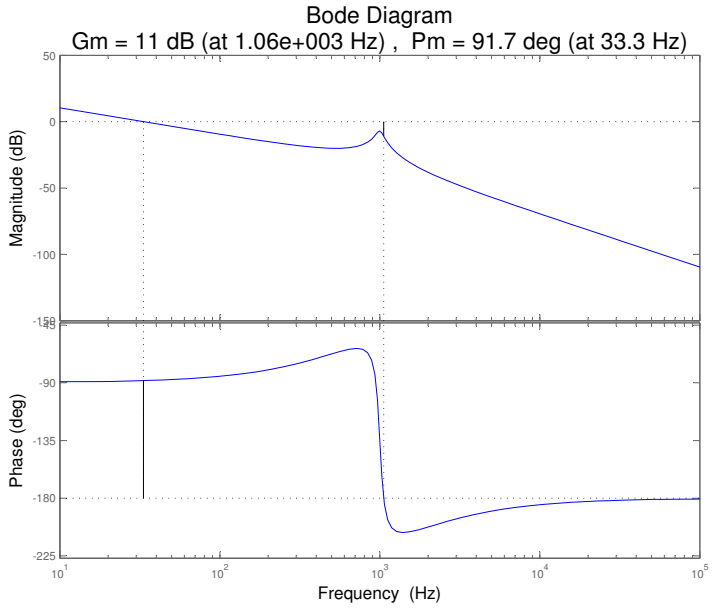


Figure 4.20: Matlab Analysis of Dominant Pole Compensator with Zero

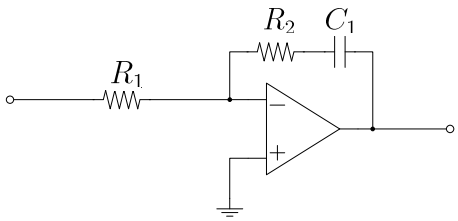


Figure 4.21: op-amp Integrator with Zero

Figure 4.22 shows a PECS circuit implementation of the system with the new compensator. Figure 4.23 shows the response of the system to a transient on the input voltage.

The modified compensator shows little improvement over the original circuit. It still fails to provide good rejection of input voltage transients and the previously observed ringing is still present.

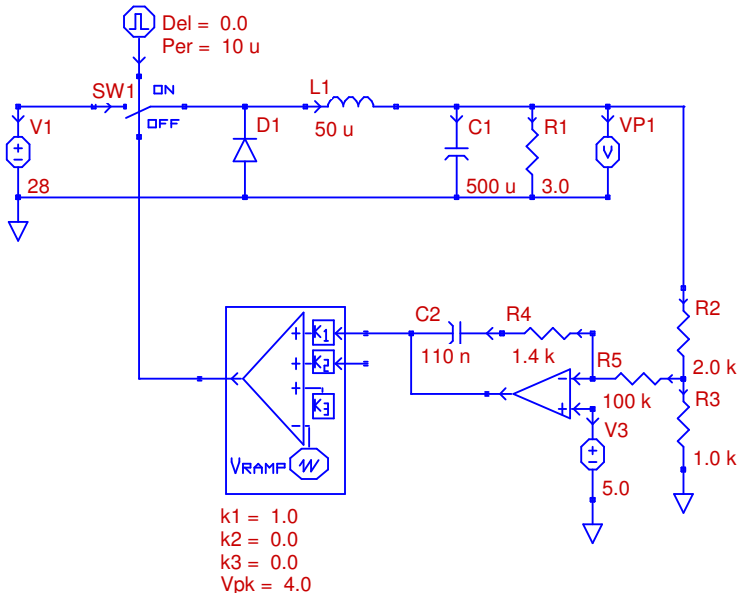


Figure 4.22: PECS Schematic of Dominant Pole with Zero Compensation (10 dB GM)

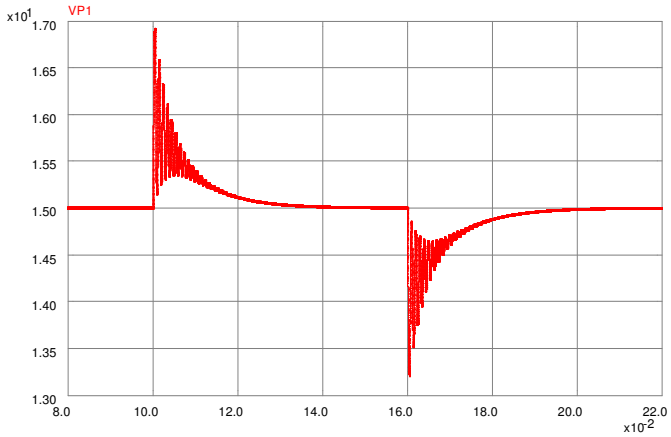


Figure 4.23: PECS Simulation of Dominant Pole with Zero Compensation (10 dB GM)

4.6 Lead Compensation

A more sophisticated way to improve the performance of the buck converter is with a lead compensator. The transfer function of this compensator is

$$G_c(s) = G_{c_o} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \ , \tag{4.21}$$

where $\omega_z < \omega_p$. As can be seen from the plot of the transfer function shown in Figure 4.24, the lead compensator provides both a phase boost that is adjustable based on the pole and zero frequencies, and a gain boost at higher frequencies that can result in a higher crossover frequency for a lead-compensated buck converter. Generally, a lead compensator is used to provide a phase boost, the level of which is chosen to improve the phase margin to a desired value. The new crossover frequency can be chosen arbitrarily. The design shown here will be to obtain a 45° phase margin and a crossover frequency of 5 kHz for the loop gain with a lead compensator.

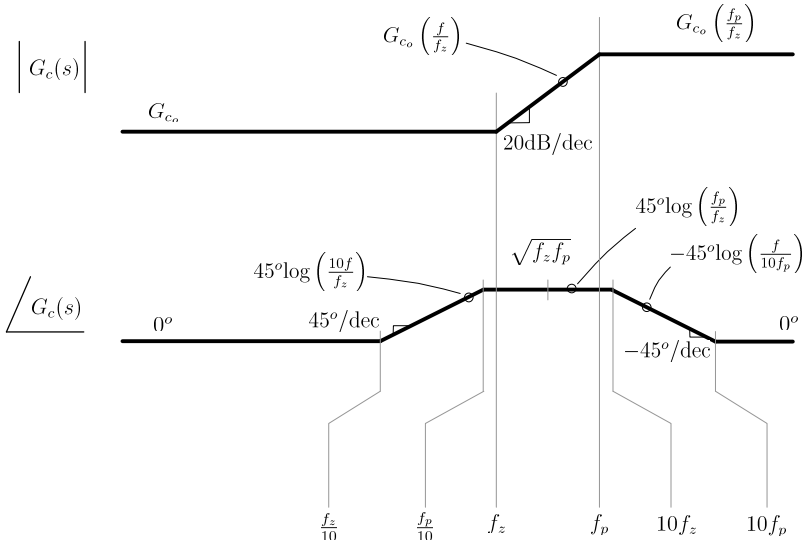


Figure 4.24: Bode Plot of Lead Compensator

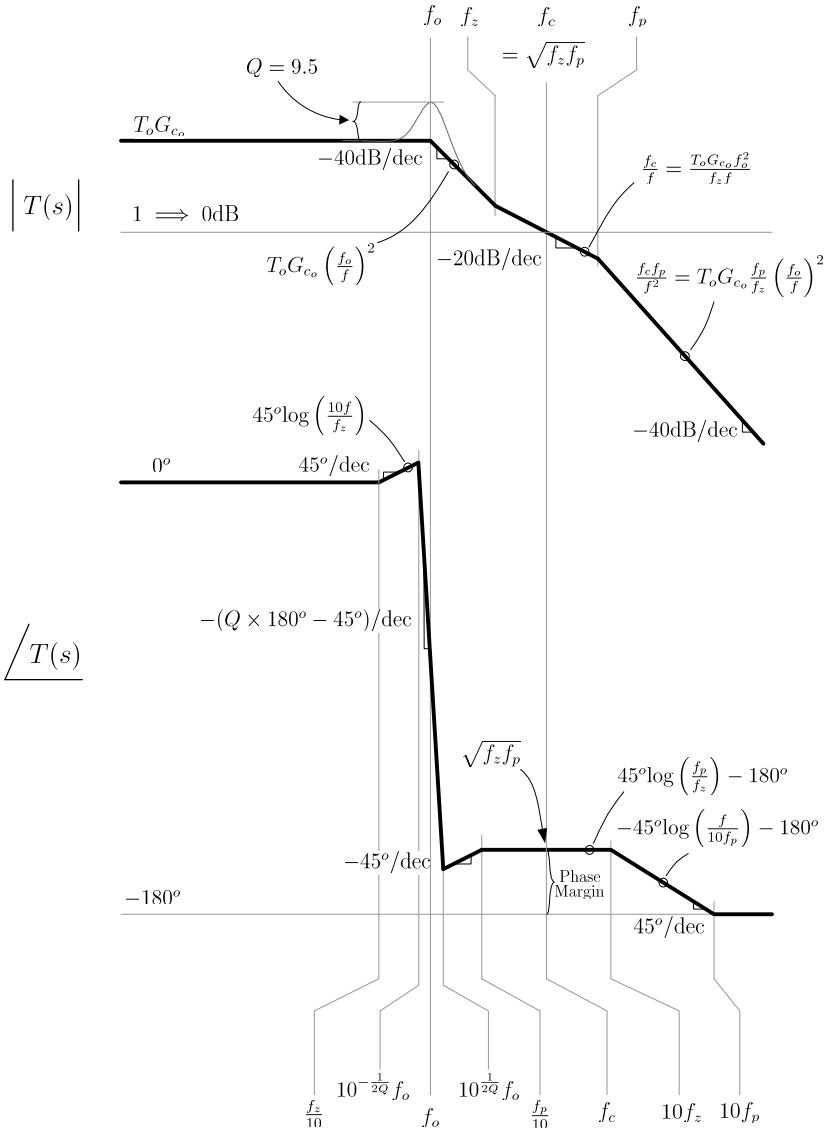


Figure 4.25: Bode Plot of Lead Compensated System

When the compensator is placed in the loop, the loop gain of the buck converter system becomes

$$T(s) = T_0 G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{4.22}$$

The asymptotic Bode plot of this loop gain is shown in Fig. 4.25. The expressions shown can be used to place the pole and zero frequencies of the compensator to obtain the desired phase margin and unity-gain crossover frequency. As can be seen, the phase margin of the lead compensated system is given by

$$\phi_M = 45^\circ \log\left(\frac{f_p}{f_z}\right)$$

For a desired phase margin of 45° we have

$$45^\circ = 45^\circ \log\left(\frac{f_p}{f_z}\right)$$

or

$$f_p = 10 f_z$$

Also, the crossover frequency, f_c will necessarily be the geometric mean of the pole and the zero frequency. Since the phase margin condition gives a relationship between the pole and zero frequencies, this can be used to solve for both.

$$f_c = \sqrt{f_z f_p}$$

$$5 \text{ kHz} = \sqrt{10 f_z^2}$$

$$f_z = \frac{5 \text{ kHz}}{\sqrt{10}}$$

$$f_z = 1.58 \text{ kHz and } f_p = 15.8 \text{ kHz}$$

These relationships result in the pole and zero frequencies for the lead compensator. To complete the design, the required low-frequency gain G_{c_o} of the compensator to place the unity-gain point at the appropriate frequency must be determined. This can be found by equating the values of the gain asymptotes at f_z.

$$T_0 G_{c0} \left(\frac{f_0}{f_z}\right)^2 = \frac{f_c}{f_z}$$

Substituting the values of f_o and T_o for the example converter, and the values of f_z and f_c as previously calculated, the gain G_{c_o} of the compensator is

$$G_{c_o} = \frac{1}{T_0}\left(\frac{f_z}{f_0}\right)^2 \frac{f_c}{f_z}$$

$$G_{c_o} = \frac{1}{2.33}\left(\frac{1.58 \text{ kHz}}{1 \text{ kHz}}\right)^2 \frac{5 \text{ kHz}}{1.58 \text{ kHz}}$$

$$G_{c_o} = 3.4$$

As seen in previous designs and now in the phase plot of Fig. 4.25, the phase response is asymptotic to -180° at high frequencies and so does not cross through this level which implies an infinite gain margin.

In summary, we have designed a lead compensator which, using asymptotic Bode plot approximations, result in a 45^circ phase margin with a unity gain frequency of 5kHz and an infinite gain margin. The Matlab simulation in Figure 4.26 verifies the results, above.

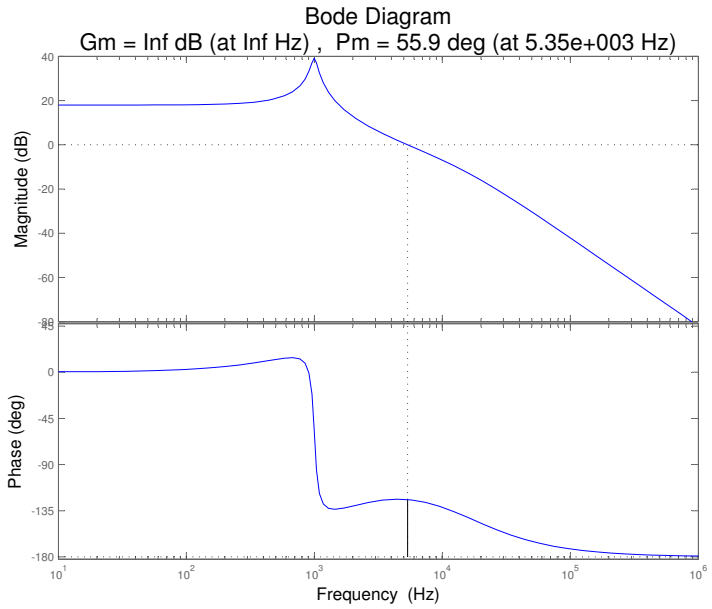


Figure 4.26: Matlab Lead Compensator

With all of the parameters of the lead compensator determined, what remains is to implement the compensator using an op-amp circuit and simulate the closed-loop converter to evaluate its performance. A general circuit that can be used to implement any lead or lag compensator is shown in Fig. 4.27. The transfer function of this circuit is

$$G_c(s) = G_{c_o} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \tag{4.23}$$

where

$$G_{c_o} = -\frac{R_2}{R_1} \tag{4.24}$$

$$f_z = \frac{\omega_z}{2\pi} = \frac{1}{2\pi R_1 C_1} \tag{4.25}$$

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi R_2 C_2} \tag{4.26}$$

The resistor ratio sets the low frequency gain, and the two resistor-capacitor pairs set the pole and zero frequencies. Using standard resistor values of $R_1 = 100\ \text{k}\Omega$ and $R_2 = 330\ \text{k}\Omega$ results in the required low frequency gain of close to $G_{c_o} = 3.4$. Using (4.23) we find

$$C_1 = \frac{1}{2\pi\,(1.58\ \text{kHz})\,(100\ \text{k}\Omega)} \Rightarrow C_1 = 1.0\ \text{nF}$$

$$C_2 = \frac{1}{2\pi\,(15.8\ \text{kHz})\,(330\ \text{k}\Omega)} \Rightarrow C_2 = 33\ \text{pF}$$

It it also necessary to derive a value for the reference voltage on the non-inverting input of the op-amp. The sensed voltage from the output will be 5 V in steady-state as before, and the control voltage should be 2.14 V. Using these in combination with the resistor values for the lead compensator, the reference voltage can be found.

$$V_{ref} = \frac{R_2}{R_1 + R_2} V_{sense} + \frac{R_1}{R_1 + R_2} V_{control}$$

$$V_{ref} = \frac{330\ \text{k}\Omega}{100\ \text{k}\Omega + 330\ \text{k}\Omega}\,(5\ \text{V}) + \frac{100\ \text{k}\Omega}{100\ \text{k}\Omega + 330\ \text{k}\Omega}\,(2.14\ \text{V}) = 4.33\ \text{V}$$

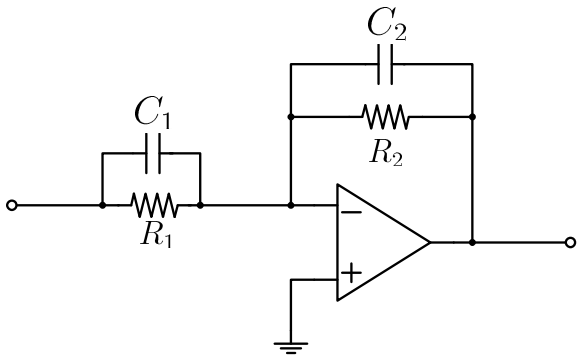


Figure 4.27: op-amp circuit implementation of lead compensator

Using these values in the PECS simulator (see Figure 4.28 for PECS schematic), the response of the lead-compensated buck converter to a step in the input voltage was simulated as before. The results of the simulation are shown in Figure 4.29. The lead compensator is quite effective in increasing the phase margin of the system. The oscillatory behavior evident in the output voltage of the uncompensated converter is not present, and the magnitude of the steady-state error due to the step is reduced, though not eliminated. Thus, the system with the lead compensator is very stable, but will still exhibit steady-state errors to

a step disturbance. To fix this problem, the system type number must be increased by adding a pole at $s = 0$, as was seen previously. This is the approach taken in the design of the subsequent compensators.

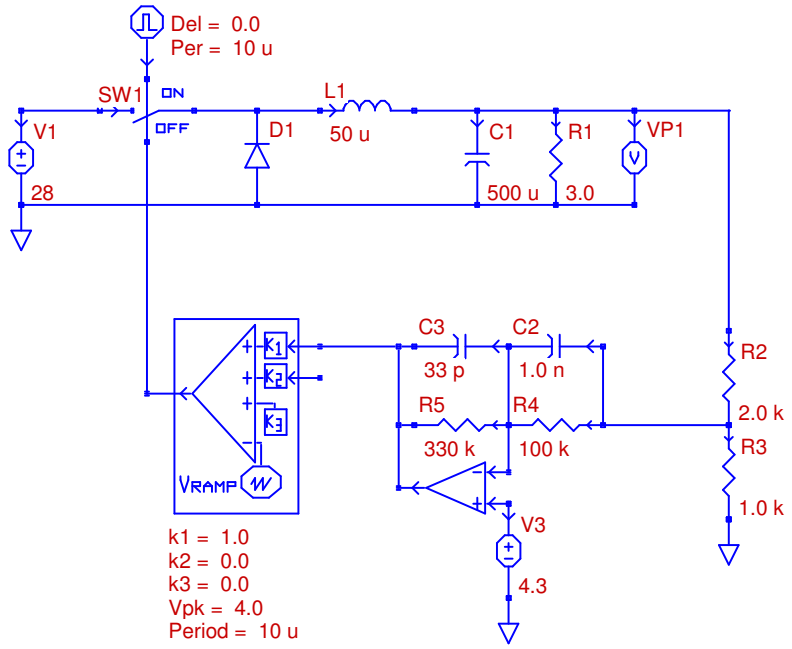


Figure 4.28: PECS Schematic of Lead System

4.7 Dominant Pole with Lead Compensation

So far we have seen that with a dominant pole integral compensation a zero steady state error can be achieved at the expense of limited bandwidth with resulting large overshoot in the step response. In contrast lead compensation is able to extend bandwidth thus reducing step response overshoot. However, due to severely curtailed low frequency loop gain, a non-zero steady state error is seen.

In this section a compensator which is a composite of the two previous compensators is examined. The exact form of the compensator is:

$$G_c(s) = \frac{\omega_I \left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_z}\right)}{s\left(1 + \frac{s}{\omega_p}\right)} \tag{4.27}$$

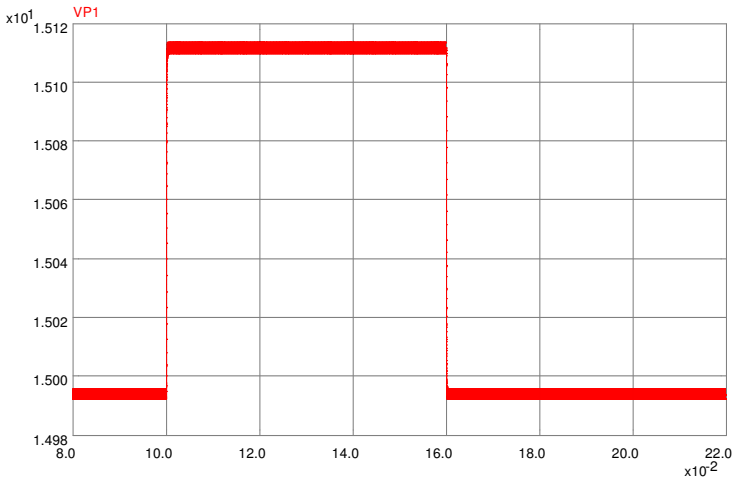


Figure 4.29: PECS Simulation of Lead System

Effectively, to the lead compensator design of the previous section we are adding an integrator pole, i.e. a pole at zero frequency, and a zero at $f_1 (= \frac{\omega_1}{2\pi})$. In the following we will consider two different values for the zero frequency f_1.

In the first case f_1 will be chosen to be the largest frequency which, based on the phase asymptote, contributes $+90°$ to the crossover frequency f_c, thus fully cancelling the $-90°$ contribution from the integrator pole. This effectively leaves the phase margin unchanged from the lead compensator design of the previous section. From the phase asymptotes plots of a zero, we see that the zero frequency f_1 should be at $\frac{f_c}{10}$ which is 500Hz.

In the second design considered here we will lower the zero frequency to $f_1 = 150$Hz and examine the effect on the closed loop performance.

In either case the expression for the loop gain is

$$T(s) = T_o \frac{\omega_I \left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_z}\right)}{s\left(1 + \frac{s}{\omega_p}\right)\left[1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2\right]} \tag{4.28}$$

where f_1 is either 500Hz or 150Hz, as discussed above and $f_I \left(= \frac{\omega_I}{2\pi}\right)$ is the only design variable to be determined.

4.7.1 Design 1: Zero $f_1 = 500$Hz

As before, asymptotic plots for the loop gain are drawn. As the construction of the phase plot is more involved than that of the magnitude plot, its construction is shown separately in Fig. 4.30. In Fig. 4.30, the top plot is that of the previous lead compensation design, as seen in Fig. 4.25. The plot of the phase of the component $\frac{1}{s}\left(1+\frac{s}{\omega_1}\right)$ is shown in the center plot where $f_1 = 500$Hz. The final phase plot for the new loop gain is shown in the bottom plot. Both magnitude and phase plots for the new loop gain are shown together in Fig. 4.31.

To determine, f_I, the one unknown variable in the loop gain, we note that at the frequency f_1 the magnitude is set equal to the low frequency loop gain of the lead compensation design of the last section.

$$T_0 \frac{f_I}{f_1} = T_0 \; G_{c_o}|_{lead} \tag{4.29}$$

For $f_1 = 500$ we find $f_I = 1770$. Thus the expression for the compensator is as given in (4.27) with the following values

$$\begin{aligned} \omega_I &= 2\pi(1770) \\ \omega_1 &= 2\pi(800) \\ \omega_z &= 2\pi(1580) \\ \omega_p &= 2\pi(15800) \end{aligned} \tag{4.30}$$

To confirm the accuracy of the design, the Bode plot of the exact loop gain was evaluated using Matlab. This is shown in Fig. 4.32. Our asymptotic design values of crossover frequency f_c and phase margin of 5kHz and 45°, respectively were determined by Matlab as given by the Matlab "margin" command to be more precisely 5,370Hz and 50.5°, respectively, thus confirming the design procedure.

A compensator which realizes the transfer function is shown in Fig. 4.33 where we find

$$\begin{aligned} \omega_I &= \frac{1}{R_1(C_2+C_3)} \\ \omega_1 &= \frac{1}{R_2 C_2} \\ \omega_z &= \frac{1}{R_1 C_1} \\ \omega_p &= \frac{1}{R_2 \frac{C_2 C_3}{C_2+C_3}} \end{aligned} \tag{4.31}$$

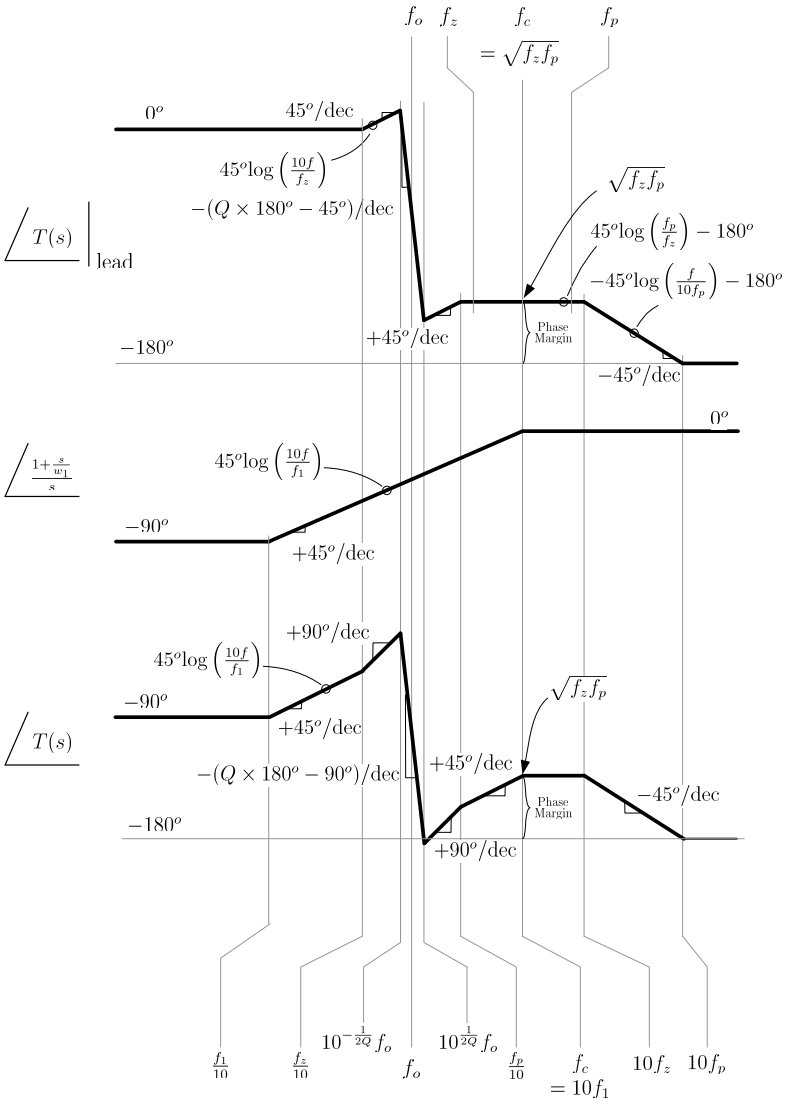


Figure 4.30: Bode Plot of Lead Compensator (500Hz)

Setting $R_1 = 100\text{K}$ and using the approximation $C_3 \ll C_2$ we find the component values:

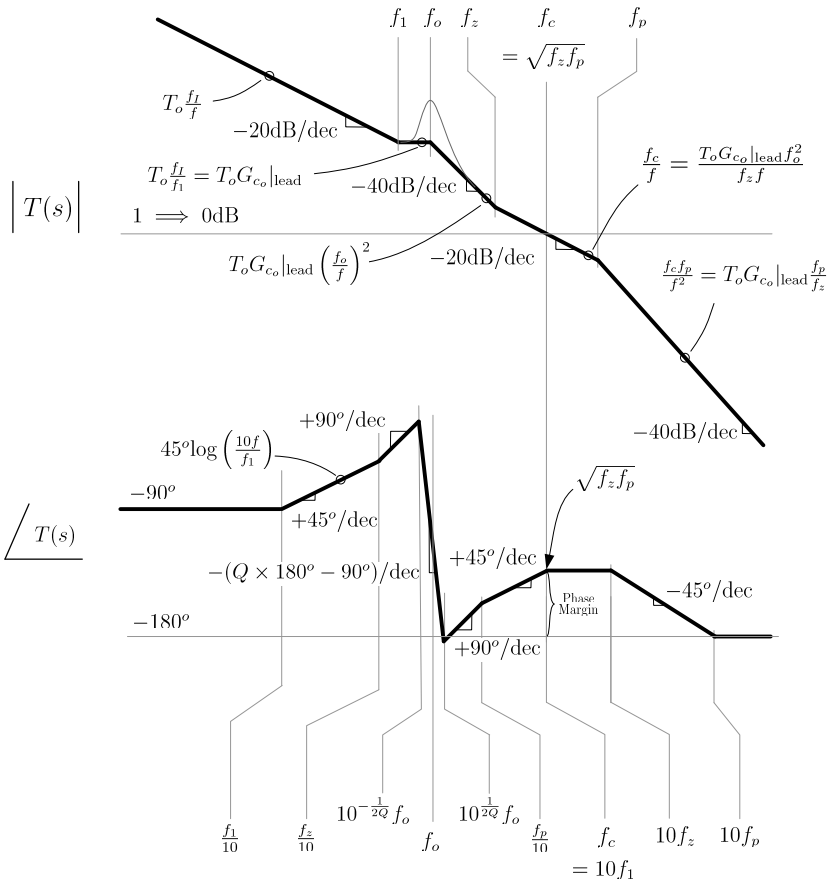


Figure 4.31: Bode Plot of System with Lead plus Integral Compensation (500Hz)

$$
\begin{aligned}
C_1 &= \frac{1}{\omega_z R_1} = 2.2\text{nF} \\
C_2 &= \frac{1}{\omega_I R_1} = 1\text{nF} \\
R_2 &= \frac{1}{\omega_1 C_2} = 330\text{k}\Omega \\
C_3 &= \frac{1}{\omega_p R_2} = 33\text{pF}
\end{aligned}
\tag{4.32}
$$

A PECS implementation of the closed loop system is shown in Fig. 4.34. The simulated response of input voltage steps $26V \rightarrow 30V \rightarrow 28V$ is shown in Fig. 4.35. Clearly seen here is the zero steady state error and a maximum voltage

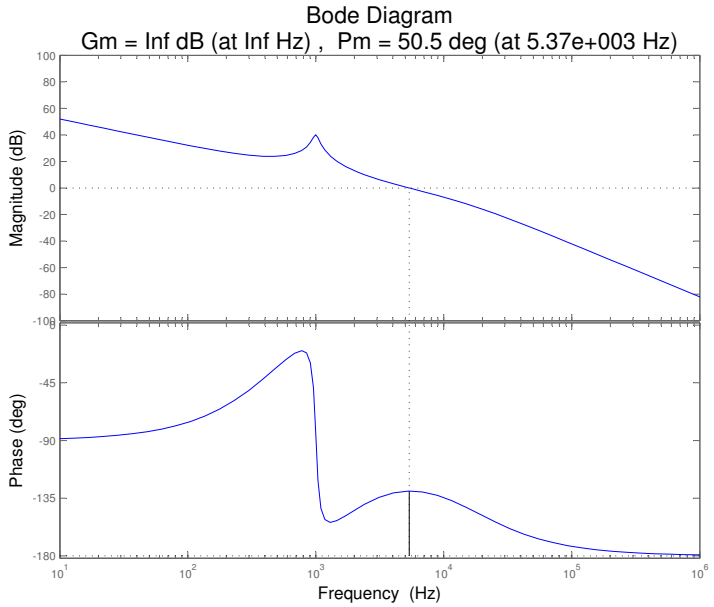


Figure 4.32: Matlab Lead Compensator with Integrator and Zero at 500Hz

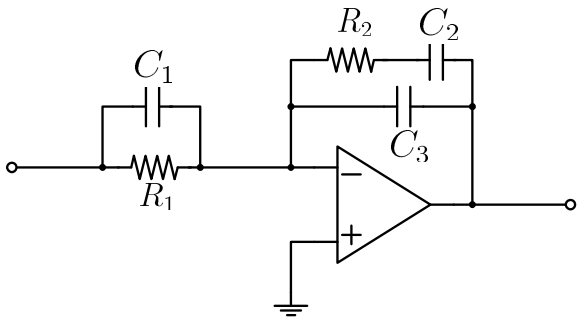


Figure 4.33: Compensator Circuit for Dominant Pole with Lead Compensation

deviation of around 80 mV with a settling time of around 1 ms.

4.7.2 Design 2: Zero $f_1 = 150$ Hz

The above design procedure will now be repeated for the case of the zero $f_1 = 150$ Hz. The resulting asymptotic phase plot construction is shown in Fig. 4.36. The final magnitude and phase asymptotic plots are given in Fig. 4.37. The new f_I is now found to be from (4.33)

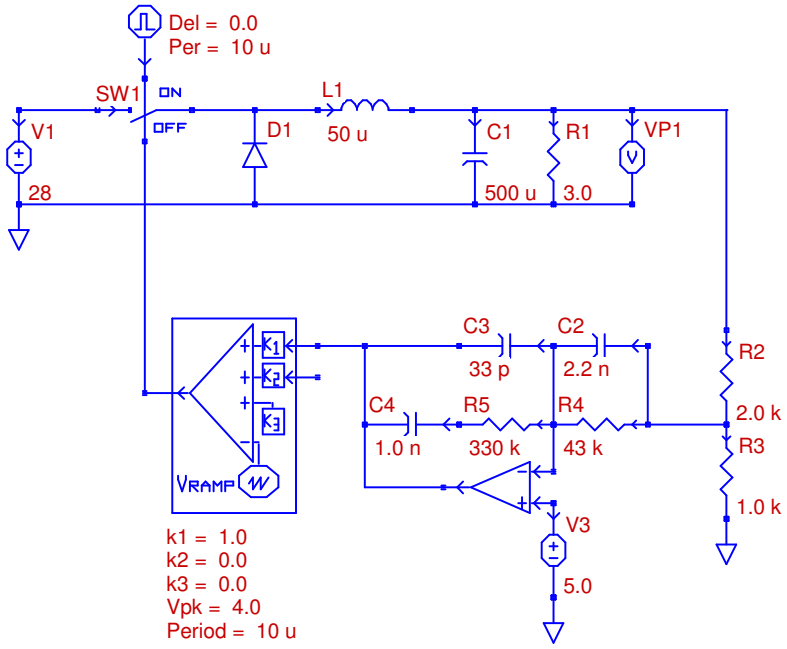


Figure 4.34: PECS Schematic of Lead Compensated System with Zero at 500Hz

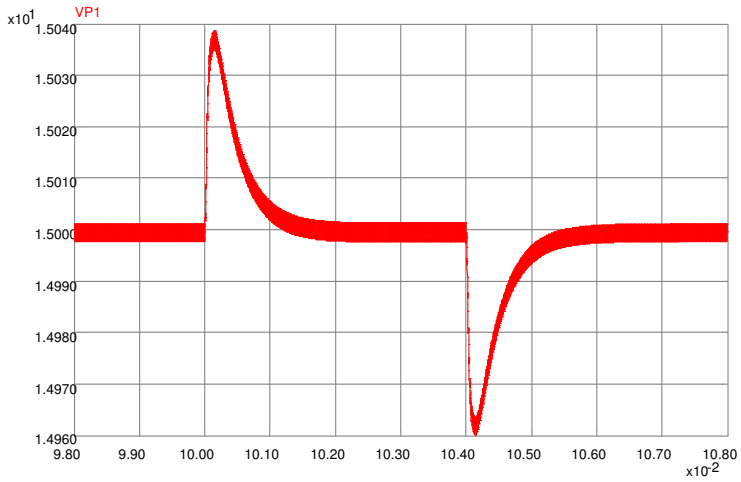


Figure 4.35: PECS Simulation of Lead Compensated System with Zero at 500Hz

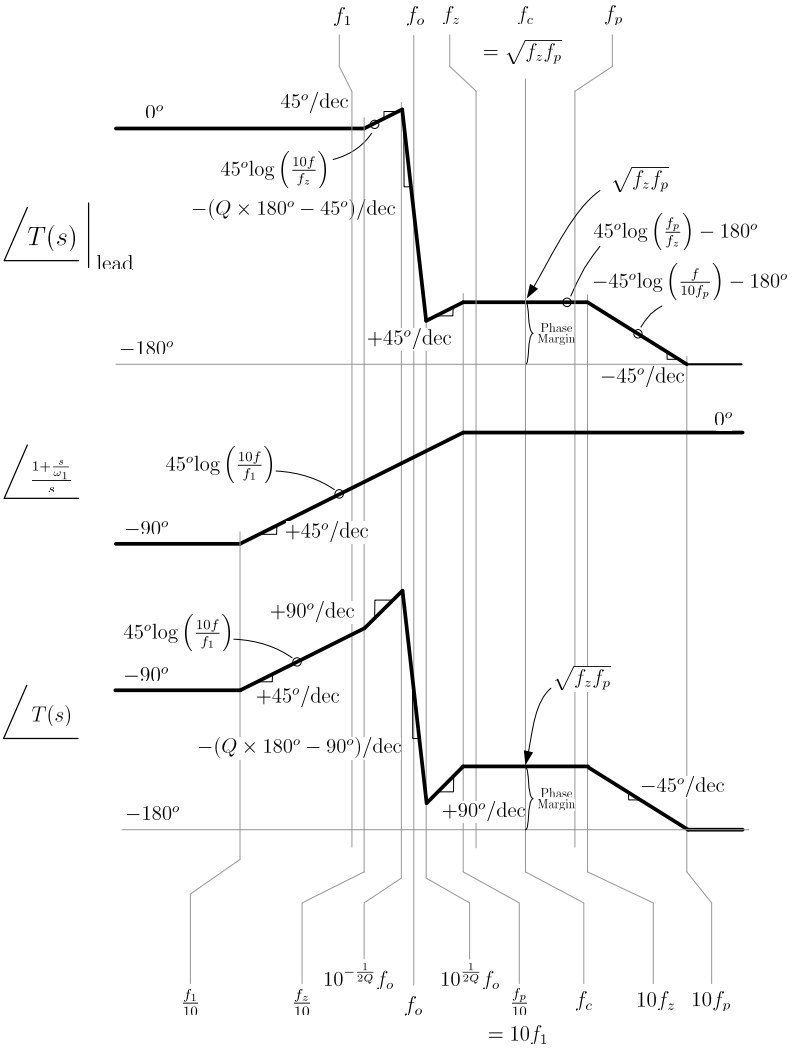


Figure 4.36: Bode Plot of Lead Compensator (150Hz)

$$f_I = f_1 T_o = 150 \times 3.4 = 351 \tag{4.33}$$

Using the new values of $f_I = 351$ and $f_1 = 150$, a more precise value of crossover frequency and phase margin is found from Matlab to be 5,350Hz and 54.3°, respectively, as seen in Fig. 4.38. Recall that the asymptotic plots indicate 5kHz and 45°, respectively.

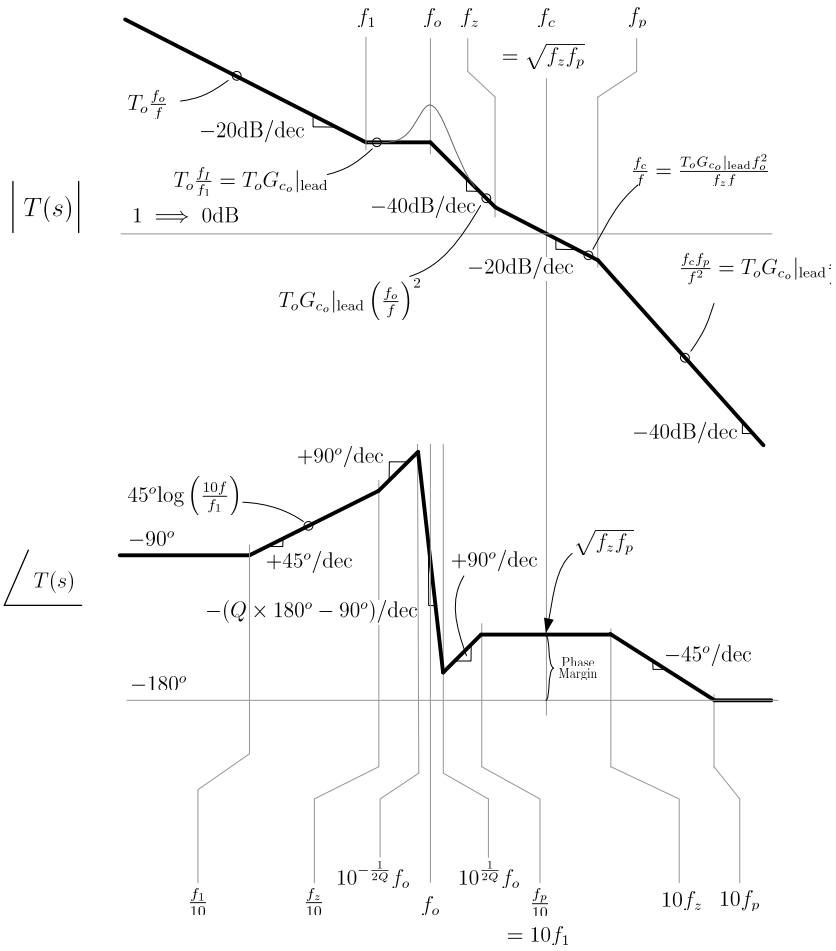


Figure 4.37: Bode Plot of System with Lead plus Integral Compensation (150Hz)

The change of $f_1 = 150$Hz to $f_1 = 150$Hz results in only a change in one capacitor value in the compensator. The resulting PECS implementation is shown in Fig. 4.39 along with the response of input voltage steps of $28V \rightarrow 30V \rightarrow 28V$, in Fig. 4.40. We now see that the peak voltage variation has slightly increased to 90 mV but the settling time has tripled to around 3ms.

4.8 Extended Bandwidth Design

In the following we examine the performance of a compensator (closely related to the previous two) which is designed to produce an extended loop bandwidth. To this end a unity gain crossover frequency $f_c = 40$kHz is, somewhat arbitrarily,

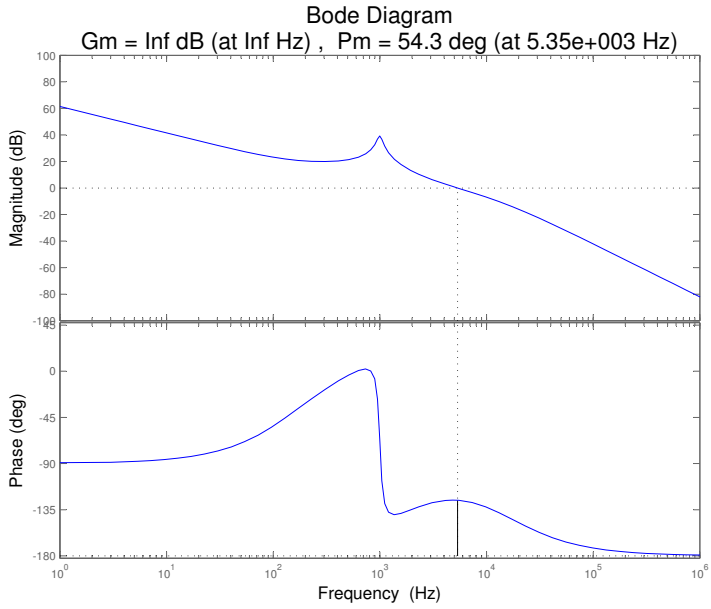


Figure 4.38: Matlab Lead Compensator with Integrator and Zero at 150Hz

chosen. The compensator used is

$$G_c(s) = \frac{\omega_I \left(1 + \frac{s}{\omega_{z_1}}\right)\left(1 + \frac{s}{\omega_{z_2}}\right)}{s} \tag{4.34}$$

The zeros $f_{z_1}(= \frac{\omega_{z_1}}{2\pi}$ and $f_{z_2} = \frac{\omega_{z_2}}{2\pi}$ are simply chosen as follows. Zero f_{z_2} is set so $f_{z_2} = f_o$ so as to counter the effects of the plant complex pole pair. The lower frequency zero f_{z_1} is set so that $f_{z_1} = \frac{f_o}{10}$ to minimize the phase drop at f_o. The resulting loop gain expression is given by

$$T(s) = \omega_I T_o \frac{(1 + \frac{s}{\omega_{z_1}})(1 + \frac{s}{\omega_{z_2}})}{s\left[1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2\right]} \tag{4.35}$$

The asymptotic magnitude and phase responses of the resulting loop gain are shown in Fig. 4.41, where the phase contributions of the different factors are individually drawn and then summed at the bottom plot to produce the overall asymptotic loop gain phase plot.

To determine the quantity $\omega_I(= 2\pi f_I)$ in (4.34) the high frequency asymptotes of the magnitude plot is used. At the crossover frequency f_c we have

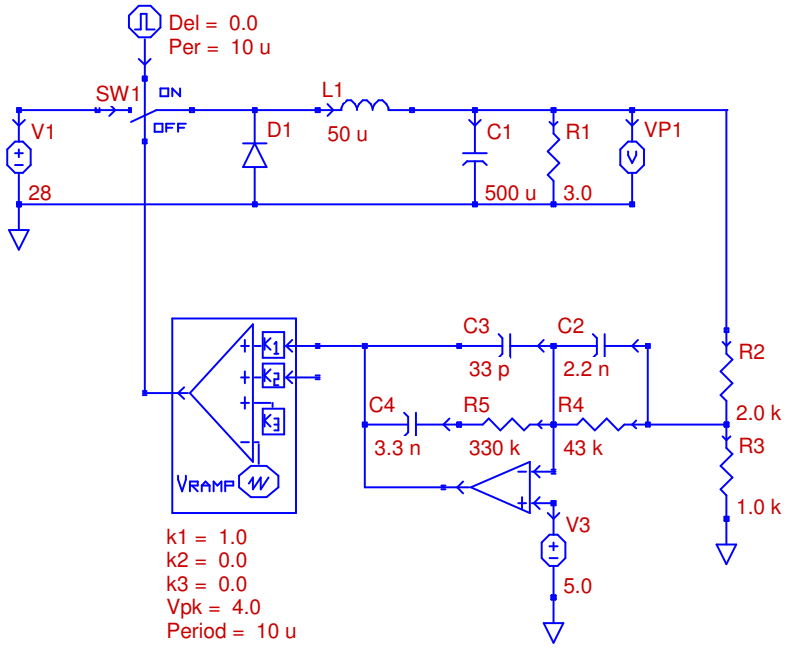


Figure 4.39: PECS Schematic of Lead Compensated System with Zero at 150Hz

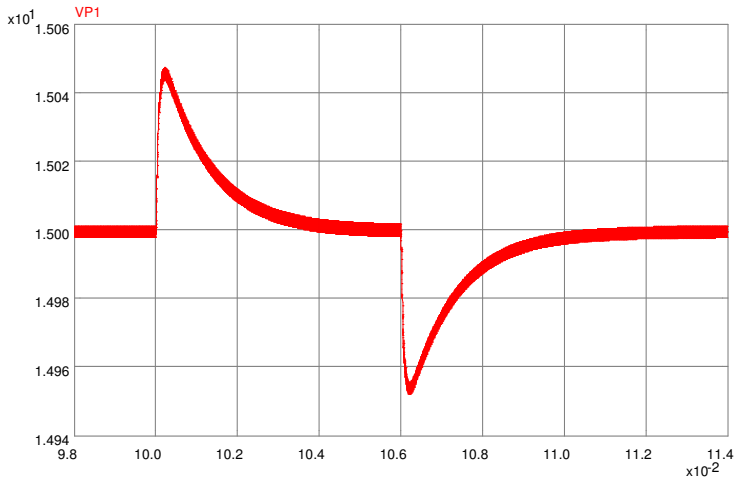


Figure 4.40: PECS Simulation of Lead Compensated System with Zero at 150Hz

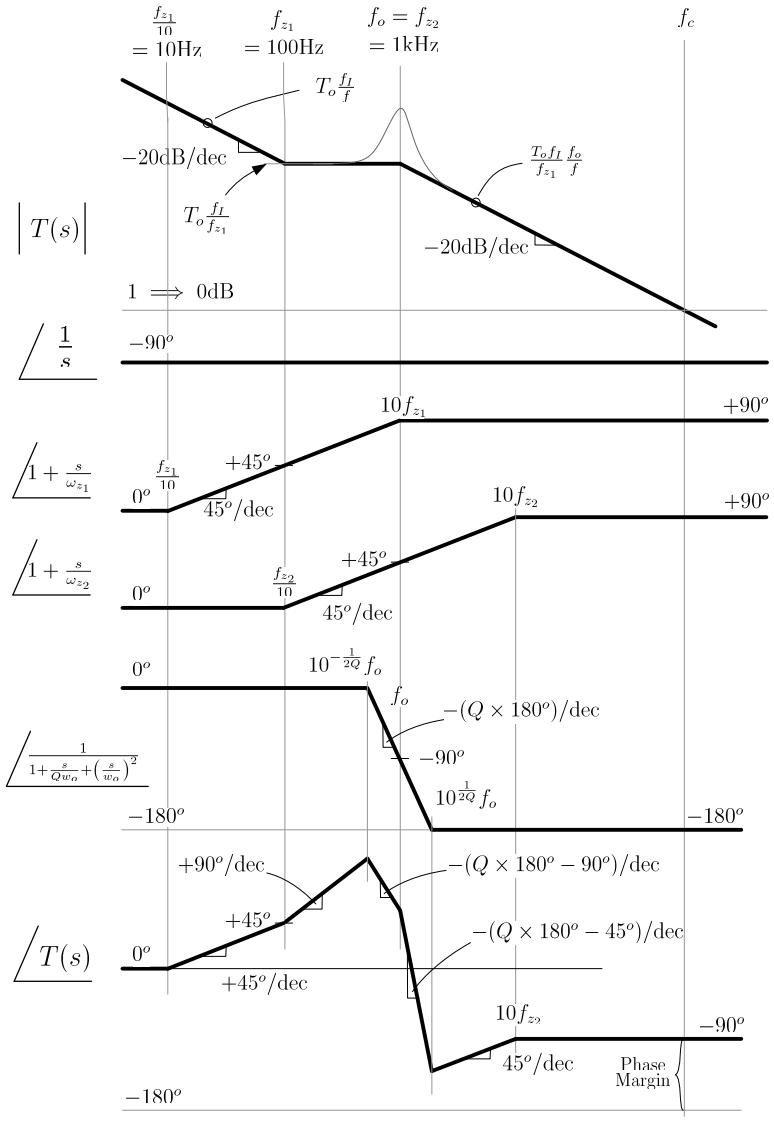


Figure 4.41: Extended Bandwidth Bode Plot and Phase Construction

$$\frac{T_o f_I}{f_{z_1}} \frac{f_o}{f_c} = 1 \tag{4.36}$$

so that we have

$$f_I = \frac{f_{z_1} f_c}{T_o f_o} \tag{4.37}$$

with the values at hand we find

$$f_I = 172 \tag{4.38}$$

From the phase asymptotic plot of Fig. 4.41 we can clearly see that the expected phase margin is 90°. Using Matlab we more precisely find with the design values used $f_c = 40$kHz and phase margin is 88.6° as shown in Fig. 4.42.

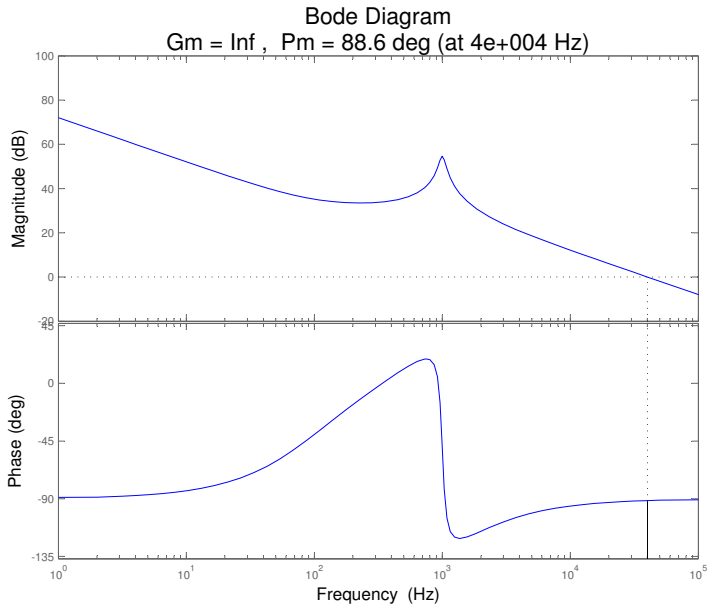


Figure 4.42: Matlab Analysis of Extended Compensator

The resulting PECS implementation is shown in Fig. 4.43 along with the response of input voltage steps of $28V \rightarrow 30V \rightarrow 28V$, in Fig. 4.44. We now see that the peak voltage variation has greatly reduced to just 30mV.

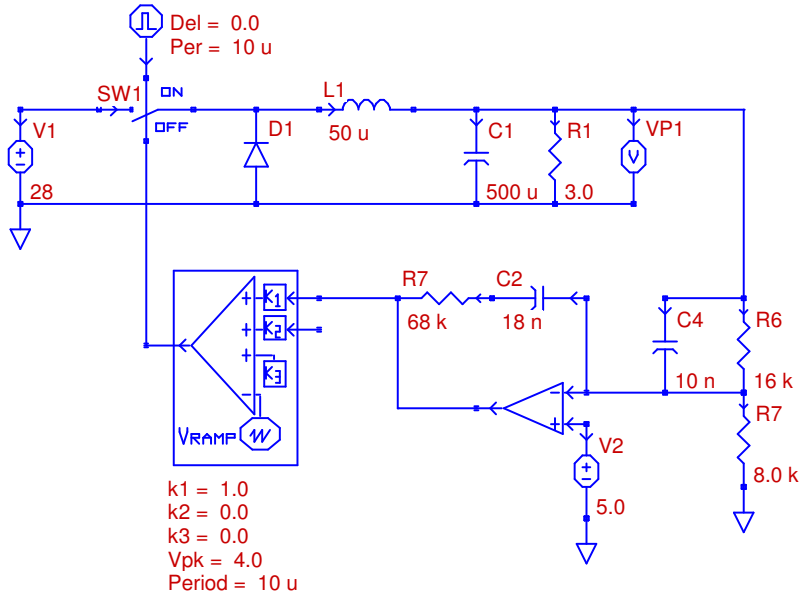


Figure 4.43: PECS Schematic of Extended System

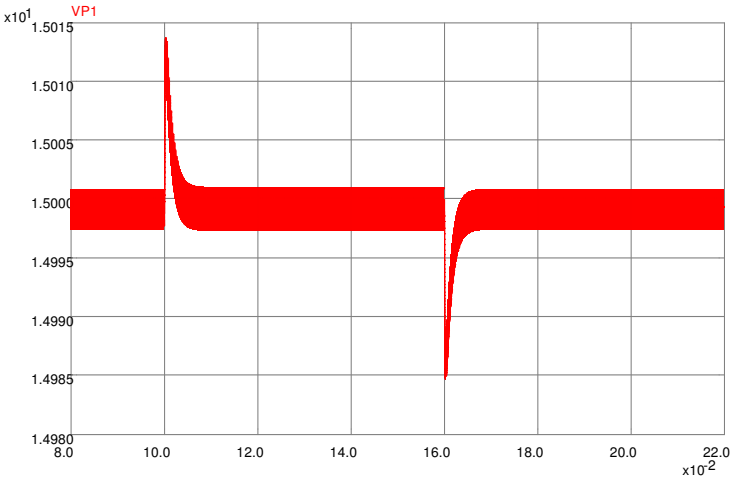


Figure 4.44: PECS Simulation of Extended System

4.9 Conclusion

The following table shows the summary of all of the results.

Table 4.2: Summary of Compensators
Loop Gain $T(s) = G_c(s)\frac{T_o}{1+\frac{s}{Q\omega_o}+\left(\frac{s}{\omega_o}\right)^2}$,

where $T_o = 2.33$, $Q = 9.5$, and $\omega_o = 2\pi(1kHz)$

Compensator Design	Compensator Transfer Function $G_c(s)$	ϕ_M Asymptote (Matlab) (degrees)	f_c Asymptote (Matlab) (kHz)	Δv (mV)
Uncompensated Open Loop	G_{c_o} $G_{c_o} = 1$	0 (5)	1.5 (1.82)	2,800
Dominant Pole (3dB gain margin)	$\frac{\omega_I}{s}$ $\omega_I = 2\pi(32)$	90 (90)	0.0744 (0.0746)	3,700
Dominant Pole + Zero (10db gain margin)	$\frac{\omega_I(1+\frac{s}{\omega_1})}{s}$ $\omega_I = 2\pi(14.3)$ $\omega_1 = 2\pi(1,000)$	90 (92)	0.0333 (0.033)	3,700
Lead	$G_{c_o}\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}}$ $G_{c_o} = 3.4$ $\omega_z = 2\pi(1,580)$ $\omega_p = 2\pi(15,800)$	45 (56)	5.0 (5.35)	120
Lead + Integrator + Zero at 500Hz	$\frac{\omega_I(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_z})}{s(1+\frac{s}{\omega_p})}$ $\omega_I = 2\pi(1,770)$ $\omega_1 = 2\pi(500)$ $\omega_z = 2\pi(1,580)$ $\omega_p = 2\pi(15,800)$	45 (51)	5.0 (5.37)	80
Lead + Integrator + Zero at 150Hz	$\frac{\omega_I(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_z})}{s(1+\frac{s}{\omega_p})}$ $\omega_I = 2\pi(351)$ $\omega_1 = 2\pi(150)$ $\omega_z = 2\pi(1,580)$ $\omega_p = 2\pi(15,800)$	45 (54)	5.0 (5.35)	90
Extended Bandwidth	$\frac{\omega_I(1+\frac{s}{\omega_{z_1}})(1+\frac{s}{\omega_{z_2}})}{s}$ $\omega_I = 2\pi(172)$ $\omega_{z_1} = 2\pi(100)$ $\omega_{z_2} = 2\pi(1000)$	90 (89)	40 (40)	30

References

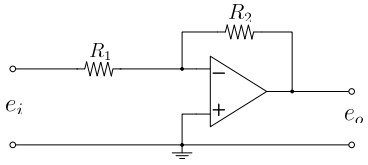
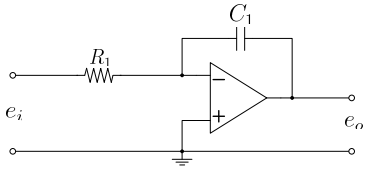
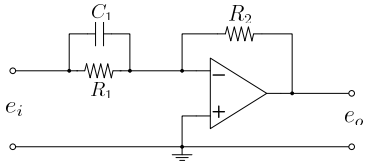
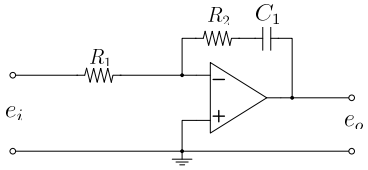
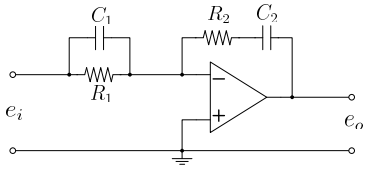
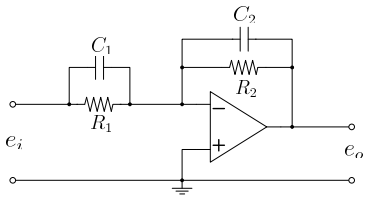
[1] Richard Tymerski, PECS Simulator ©1999-2009, Portland, Oregon,tymerski@ece.pdx.edu

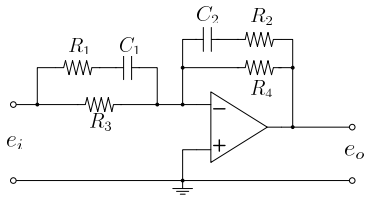
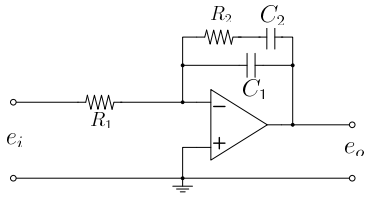
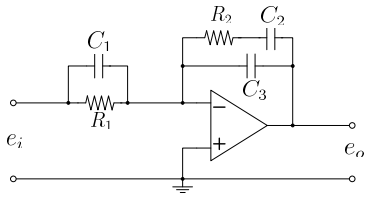
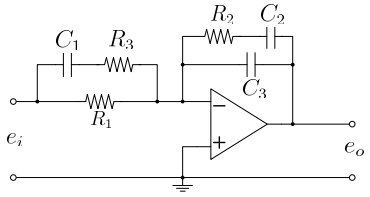
[2] Matlab, ©1984-2007, The MathWorks Inc., www.mathWorks.com

[3] Robert W. Erickson and Dragan Maksimovic, Fundamentals of Power Electronics Second Edition. Springer Science+Business Media, LLC, 233 Spring Street, New York, NY 10013, USA, 2001.

Appendix

4.9.1 Compensator Circuits

	Control Action	$G(s) = \frac{E_o(s)}{E_i(s)}$	Operational Amplifier Circuits
1	P Proportional	$-A$ where: $A = \frac{R_2}{R_1}$	
2	I Integral	$-\frac{1}{s/\omega_0}$ where: $\omega_0 = \frac{1}{R_1 C_1}$	
3	PD Proportional-Derivative	$-A(1+\frac{s}{\omega_1})$ where: $A = \frac{R_2}{R_1}, \quad \omega_1 = \frac{1}{R_1 C_1}$	
4	PI Proportional-Integral	$-A\frac{1+\frac{s}{\omega_1}}{\frac{s}{\omega_1}}$ where: $A = \frac{R_2}{R_1}, \quad \omega_1 = \frac{1}{R_2 C_1}$	
5	PID Proportional -Integral- Derivative	$-A\frac{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})}{\frac{s}{\omega_2}}$ where: $A = \frac{R_2}{R_1}, \quad \omega_1 = \frac{1}{R_1 C_1}, \quad \omega_2 = \frac{1}{R_2 C_2}$	
6	Lead if $\omega_1 < \omega_2$ or Lag if $\omega_1 > \omega_2$	$-A\frac{1+\frac{s}{\omega_1}}{1+\frac{s}{\omega_2}}$ where: $A = \frac{R_2}{R_1}, \quad \omega_1 = \frac{1}{R_1 C_1}, \quad \omega_2 = \frac{1}{R_2 C_2}$	

	Control Action	$G(s) = \frac{E_o(s)}{E_i(s)}$	Operational Amplifier Circuits
7	Lead-Lag	$-A\frac{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})}{(1+\frac{s}{\omega_3})(1+\frac{s}{\omega_4})}$ where: $A = \frac{R_4}{R_3}$, $\omega_1 = \frac{1}{(R_1+R_3)C_1}$, $\omega_2 = \frac{1}{R_2C_2}$, $\omega_3 = \frac{1}{R_1C_1}$, $\omega_4 = \frac{1}{(R_2+R_4)C_2}$	
8	Integrator with Lead or Lag	$-\frac{\omega_0}{s}\frac{(1+\frac{s}{\omega_1})}{(1+\frac{s}{\omega_2})}$ where: $\omega_0 = \frac{1}{R_1(C_1+C_2)}$, $\omega_1 = \frac{1}{R_2C_2}$, $\omega_2 = \frac{1}{R_2\frac{C_1C_2}{C_1+C_2}}$	
9	Integrator with Lead	$-\frac{\omega_0}{s}\frac{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})}{(1+\frac{s}{\omega_3})}$ where: $\omega_0 = \frac{1}{R_1(C_2+C_3)}$, $\omega_1 = \frac{1}{R_2C_2}$, $\omega_2 = \frac{1}{R_1C_1}$, $\omega_3 = \frac{1}{R_2\frac{C_2C_3}{C_2+C_3}}$	
10	Integrator with Lead-Lag	$-\frac{\omega_0}{s}\frac{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})}{(1+\frac{s}{\omega_3})(1+\frac{s}{\omega_4})}$ where: $\omega_0 = \frac{1}{R_1(C_2+C_3)}$, $\omega_1 = \frac{1}{R_2C_2}$, $\omega_2 = \frac{1}{C_1(R_1+R_3)}$, $\omega_3 = \frac{1}{R_3C_1}$, $\omega_4 = \frac{1}{R_2\frac{C_2C_3}{C_2+C_3}}$	

4.10 MATLAB Code

```
clear all
close all

f0 = 1000;
Q = 9.5;
T0 = 2.33;
w0 = 2*pi*f0;

s = tf('s');
Ts = T0/((s/w0)^2 + s/(Q*w0) + 1);

%%%%%%%%%%%%%%%%%
```

```
%  Open loop

figure(1)
margin(Ts)
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;

%%%%%%%%%%%%%%%%%%
%  Lead compensation

Gc0 = 3.4;
wz = 2*pi*1500;
wp = 2*pi*15000;

Gc1 = Gc0*(1+s/wz)/(1+s/wp);

Ts1 = Gc1*Ts;

figure(2)
margin(Ts1)
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;


%%%%%%%%%%%%%%%%%%
%  500

wi = Gc0*2*pi*500;
wz2 = 2*pi*500;
wz = 2*pi*1500;
wp = 2*pi*15000;

Gc2 = wi/s*(1+s/wz2)*(1+s/wz)/(1+s/wp);
Ts2 = Gc2*Ts;

figure(3)
margin(Ts2)
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;


%%%%%%%%%%%%%%%%%%
%  150

wi = Gc0*2*pi*150;
wz2 = 2*pi*150;
wz = 2*pi*1500;
wp = 2*pi*15000;
```

```
70
71 Gc3 =wi/s*(1+s/wz2)*(1+s/wz)/(1+s/wp);
72 Ts3 = Gc3*Ts;
73
74 figure(4)
75 margin(Ts3)
76 h = gcr;
77 h.AxesGrid.Xunits = 'Hz';
78 h.AxesGrid.TitleStyle.FontSize = 16;
79 h.AxesGrid.XLabelStyle.FontSize = 12;
80 h.AxesGrid.YLabelStyle.FontSize = 12;
81
82
83 %%%%%%%%%%%%%%%%%%
84 % Extended bandwidth
85
86 %wi = Gc0*2*pi*100;
87 wi = 2*pi*100*40000/(T0*1000); %  fc = 40000
88 wz1 = 2*pi*100;
89 wz2 = 2*pi*1000;
90
91 Gc4 = wi/s*(1+s/wz2)*(1+s/wz1);
92 Ts4 = Gc4*Ts;
93
94 figure(5)
95 margin(Ts4)
96 h = gcr;
97 h.AxesGrid.Xunits = 'Hz';
98 h.AxesGrid.TitleStyle.FontSize = 16;
99 h.AxesGrid.XLabelStyle.FontSize = 12;
100 h.AxesGrid.YLabelStyle.FontSize = 12;
101
102 %%%%%%%%%%%%%%%%%%
103 %  Dominant pole
104
105 Gcd0 = 200;
106
107 Gc5 = Gcd0/s;
108
109 Ts5 = Gc5*Ts;
110
111 figure(6)
112 margin(Ts5)
113 h = gcr;
114 h.AxesGrid.Xunits = 'Hz';
115 h.AxesGrid.TitleStyle.FontSize = 16;
116 h.AxesGrid.XLabelStyle.FontSize = 12;
117 h.AxesGrid.YLabelStyle.FontSize = 12;
118
119 %%%%%%%%%%%%%%%%%%
120 %  Dominant pole with zero
121
122 Gcdz0 = 1/sqrt(10)*w0/(T0*Q);  %  89.76
123 wz = 2*pi*1000;
124
125 Gc6 = Gcdz0*(1+s/wz)/s;
126
```

```
127 Ts6 = Gc6*Ts;
128
129 figure(7)
130 margin(Ts6)
131 h = gcr;
132 h.AxesGrid.Xunits = 'Hz';
133 h.AxesGrid.TitleStyle.FontSize = 16;
134 h.AxesGrid.XLabelStyle.FontSize = 12;
135 h.AxesGrid.YLabelStyle.FontSize = 12;
```

Chapter 5

Worked Examples

5.1 Stability Analysis

5.1.1 Introduction

In this chapter, analysis of system stability will be explored through a worked example. At the end of the chapter, the reader will be able to apply the techniques that have been presented thus far to confirm system stability.

5.1.2 Stability Analysis

Consider an arbitrary system with the following loop gain

$$T(s) = A\frac{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_1}\right)}{s^3}$$

where $A = 300$, $\omega_z = 40rad/s$, and $\omega_z = 1rad/s$

Using the methodology that has been developed to this point, the loop gain, $T(s)$ will be analyzed to determine whether the system is stable.

The stability analysis begins by constructing an asymptotic bode plot of the given system, as shown in Figure 5.1.

Using the asymptotic bode plot, the phase margin is calculated by utilizing the magnitude to determine the crossover frequency:

$\frac{A}{\omega_c^2} = 1$ or $\omega_c = \sqrt{A} = 17.3rad/s$

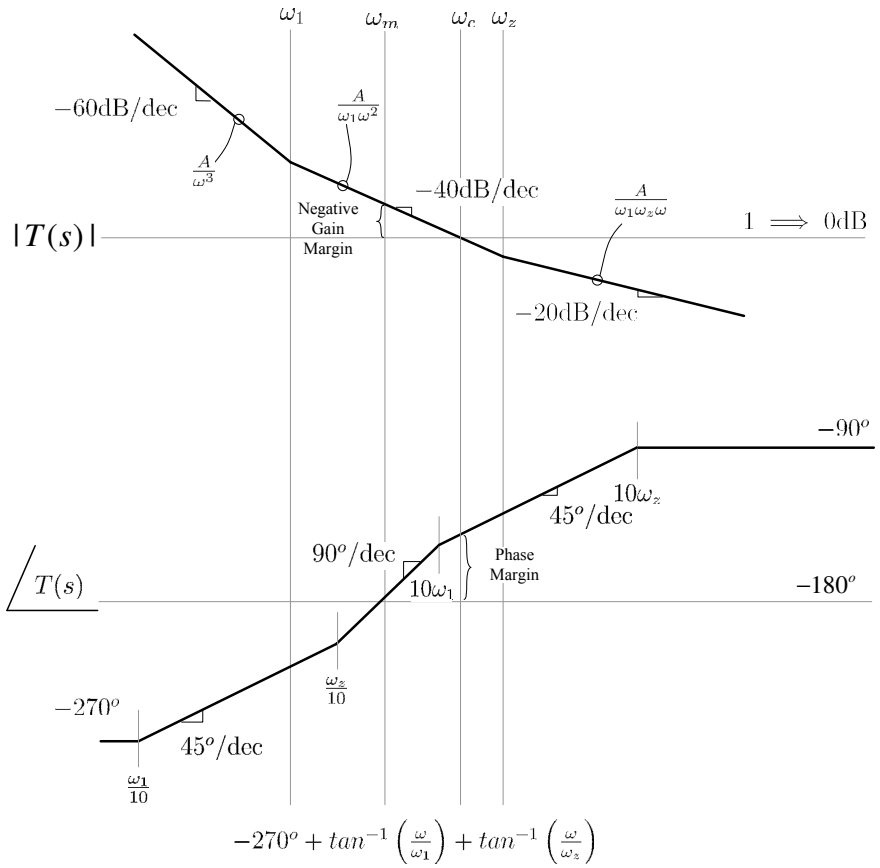


Figure 5.1: Bode Plot: System Loop Gain

With the crossover frequency defined, the margin is calculated by inserting the frequency value into the loop gain phase equation:

$$PM = 180^o - 270^o + tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) + tan^{-1}\left(\frac{\omega_c}{\omega_1}\right)$$

$$PM = 180^o - 270^o + tan^{-1}\left(\frac{17.3}{40}\right) + tan^{-1}\left(\frac{17.3}{1}\right) = 20^o$$

To determine the gain margin, the phase equation is used to determine the frequency in which the phase is -180^o.

$$-180^o = -270^o + tan^{-1}\left(\frac{\omega_m}{\omega_z}\right) + tan^{-1}\left(\frac{\omega_m}{\omega_1}\right)$$

Solving the phase equation for ω_m, $\omega_m = 6.32 rad/s$

Inserting the computed value of ω_m into the magnitude equation, the gain margin is calculated as follows:

$$|T(j\omega_m)| = \frac{A}{\omega_m^2} = \frac{300}{6.32^2} = 7.5$$

$$GM = -20log_{10}(7.5) = -17.5dB$$

Using MATLAB to verify the asymptotic bode plot, Figure 5.2 confirms the phase and gain margin analysis, with a gain margin and phase margin error of 1.1% and 6.1% respectively, due to the approximations of the asymptotic magnitude plot.

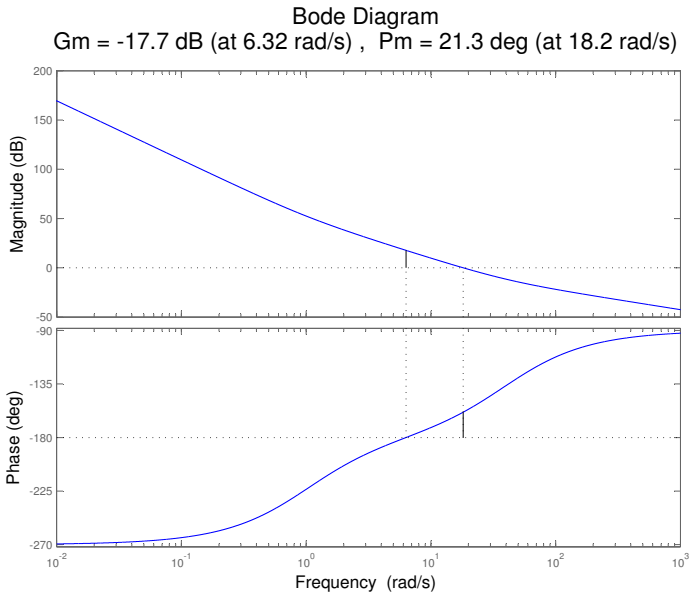


Figure 5.2: Matlab Analysis of phase and gain margin

With a positive phase margin, and a negative gain margin, additional criterion are necessary to determine if the system is stable. Another method used to determine the stability of a system is the Routh-Hurwitz stability criterion.

Before the Routh-Hurwitz criterion can be applied to the presented system, a closed loop transfer function must be derived for the system loop gain. One possible realization of the closed loop system is presented in Figure 5.3.

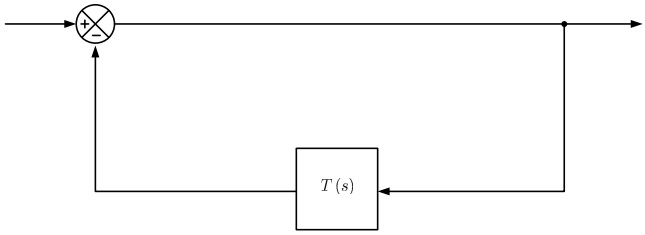


Figure 5.3: Closed-Loop realization of T_s

From Figure 5.3, the closed-loop transfer function is derived as follows:

$$T_{cl}(s) = \frac{1}{1 + T(s)}$$

$$T_{cl}(s) = \frac{1}{\frac{s^3 + A\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_1}\right)}{s^3}}$$

$$T_{cl}(s) = \frac{s^3}{s^3 + \frac{A}{\omega_z \omega_1} s^2 + A\left(\frac{1}{\omega_z} + \frac{1}{\omega_1}\right) s + A}$$

With the system defined in a closed-loop form, the denominator polynomial can be used to determine system stability as shown in Figure 5.4

s^3	1	$A\left(\frac{1}{\omega_z} + \frac{1}{\omega_1}\right)$
s^2	$\frac{A}{\omega_1 \omega_z}$	A
s^1	$\frac{A(\omega_1+\omega_z)}{\omega_z \omega_1} - \omega_z \omega_1$	
s^0	A	

Figure 5.4: Routh Hurwitz analysis of closed loop system

Applying the system parameters, Figure 5.5 confirms that no sign changes are present in the first column. This confirms that the system is stable, while having negative gain margin.

s^3	1	307.5
s^2	7.5	300
s^1	267.5	
s^0	300	

Figure 5.5: Routh Hurwitz Values

With the system confirmed as stable, the next item to explore is the possible parameter shifting in the system that could cause the system to become unstable. From the derivations shown in Figure 5.4, the only term that could cause a sign change in the first column is the s^1 term. Setting this term to zero and solving for A:

$$\frac{A\left(\omega_1+\omega_z\right)}{\omega_1\omega_z}-\omega_1\omega_z=0$$

$$A=\frac{1}{\omega_z+\omega_1}=39.024$$

Applying the shifted A parameter to the asymptotic bode plot of Figure 5.1, the updated bode plot is shown in Figure 5.6.

Applying the new value of A to the magnitude equation, $\frac{A}{\omega_c^2}=1$ or $\omega_c=\sqrt{A}=6.25 rad/s$. With this frequency, the phase margin is calculated to be -0.2^o.

As a confirmation of the above margin estimate due to parametric value shift, Figure 5.7 confirms the analysis, with a phase margin of $-8.82\cdot10^{-5}$.

5.1.3 Summary

This chapter has shown the reader how to apply asymptotic bode plots to determine the stability of a system. The reader has also learned that in some scenarios it may be necessary to use asymptotic bode plot analysis in conjunction with the Routh-Hurwitz stability criterion to determine the stability of a system.

5.1.4 MATLAB Code

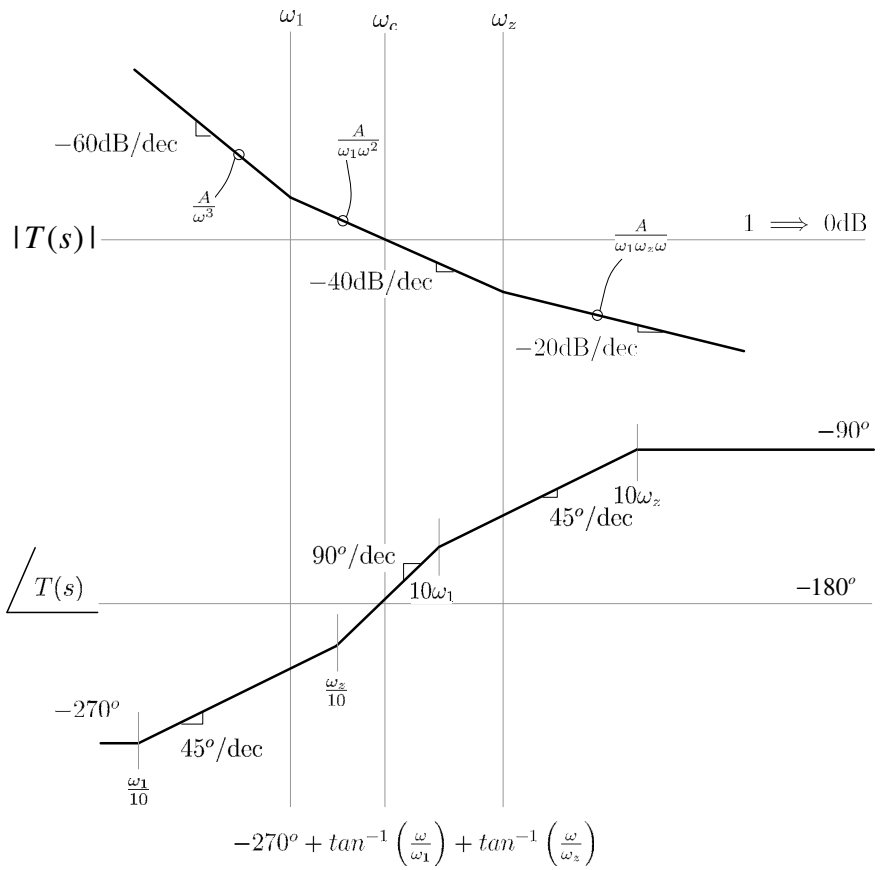


Figure 5.6: Bode Plot: System Loop Gain with parametric shift

```
clear all;
close all;

f = logspace(-3,3,10000);
w = 2*pi*f;
s = tf('s');

A = 300;
w1 = 1;
wz = 40;

%=========================================================================
%System Loop Gain
%=========================================================================
sys = A*(1+s/w1)*(1+s/wz)/(s^3);

figure(1)
```

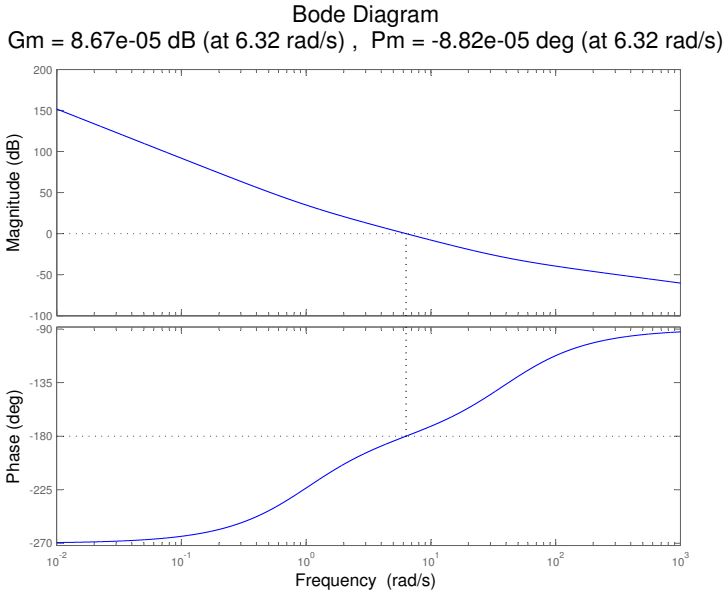


Figure 5.7: Matlab Analysis of phase and gain margin with parametric shift

```
18 [mag, phase] = bode(sys,w);
19 margin(mag, phase, w)
20
21 h = gcr;
22 xlim([10^-2 10^3]);
23 h.AxesGrid.TitleStyle.FontSize = 16;
24 h.AxesGrid.XLabelStyle.FontSize = 12;
25 h.AxesGrid.YLabelStyle.FontSize = 12;
26 %=========================================================================
27
28
29 %=========================================================================
30 %Plot Marginal Stability Per Routh Hurwitz
31 %=========================================================================
32 A=39.024;
33
34 sys = A*(1+s/w1)*(1+s/wz)/(s^3);
35
36 figure(2)
37 [mag, phase] = bode(sys,w);
38 margin(mag, phase, w)
39
40 h = gcr;
41 xlim([10^-2 10^3]);
42 h.AxesGrid.TitleStyle.FontSize = 16;
43 h.AxesGrid.XLabelStyle.FontSize = 12;
44 h.AxesGrid.YLabelStyle.FontSize = 12;
45 %=========================================================================
```

5.2 Design Example

5.2.1 Introduction

Consider the following feedback system:

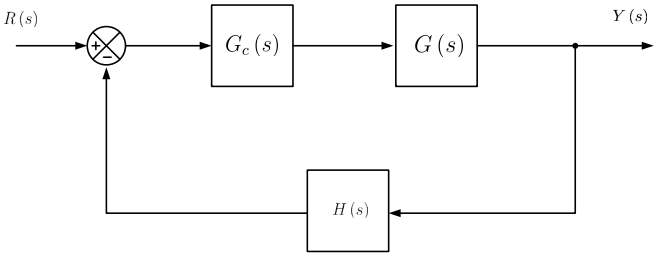


Figure 5.8: Feedback System Block Diagram

$$G(s) = \frac{G_o}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)} \tag{5.1}$$

$$H(s) = k \tag{5.2}$$

where $G_o = 500$, $\omega_1 = 2\pi(10)$, $\omega_2 = 2\pi(100)$, $\omega_3 = 2\pi(300)$, and $k = 0.5$.

$G_c(s)$ is a compensator that we need to design which is typically a lead, lag or lead-lag compensator or a variant of the PID compensators, (i.e. P, 1, PI, PD or PID).

5.2.2 Uncompensated System

We start our evaluation with an uncompensated open-loop system, one with a $G_c(s) = 1$. The loop gain is given as

$$T(s) = \frac{T_o}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)} \tag{5.3}$$

where

$$T_o = G_o H_o = 500 \cdot 0.5 = 250$$

$$\omega_1 = 2\pi(10), \omega_2 = 2\pi(100), \omega_3 = 2\pi(300)$$

We construct the Bode plot of the open-loop system

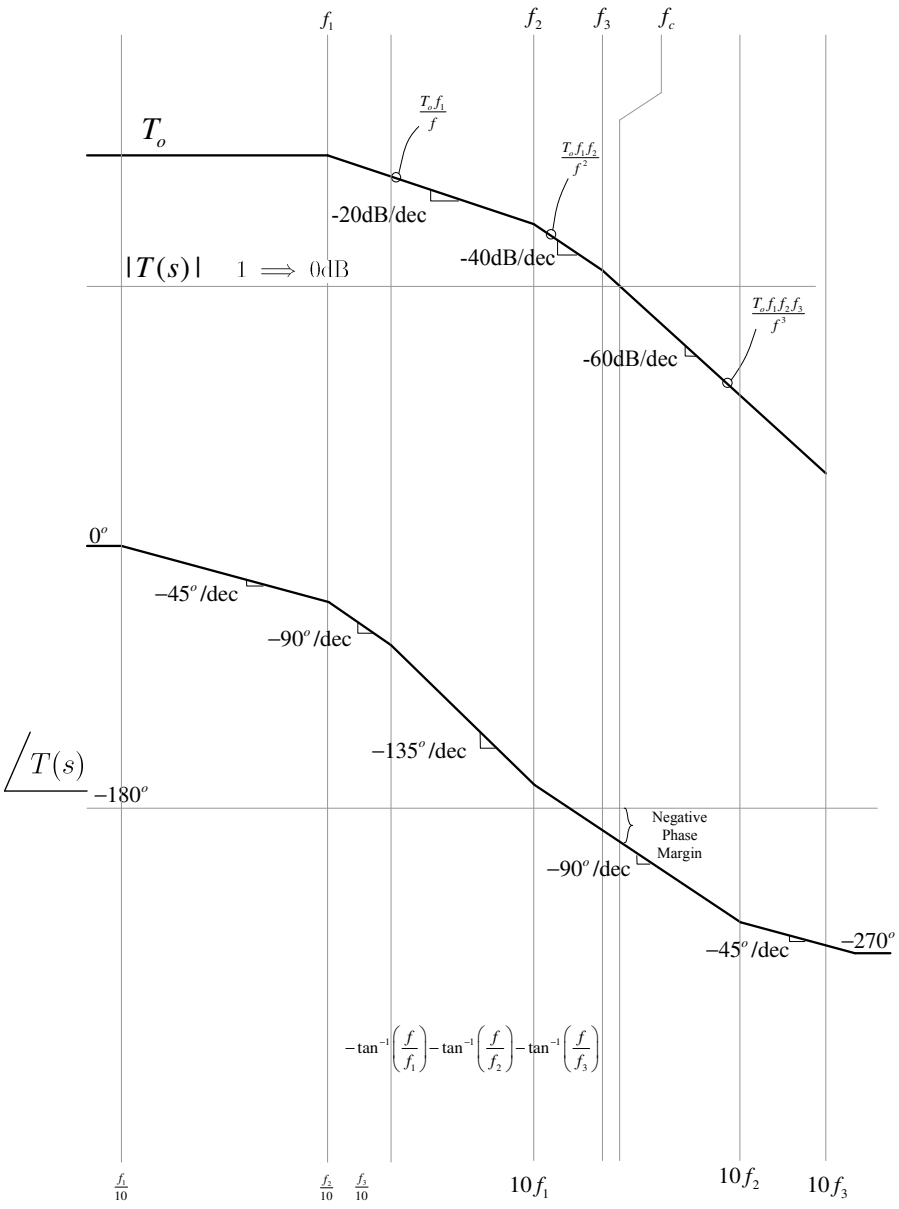


Figure 5.9: Bode Plot: Uncompensated System

Figure 5.10 is a Matlab margin plot indicating the actual unity gain frequency to be 385Hz with a phase margin of -36.1. Also, the Matlab analysis indicates a gain margin of -1 4.8dB.

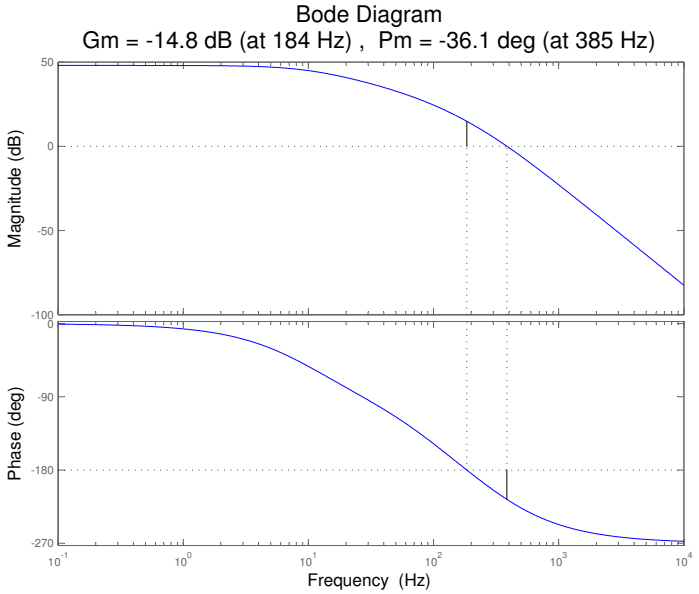


Figure 5.10: Matlab Analysis of Uncompensated System

These margins indicate that the open-loop system is unstable. So, the compensation is needed to make the system stable and improve the performance of the system.

5.2.3 Dominant Pole Compensated System

Dominant pole compensation is one of the simplest and most common forms of feedback compensation. The motivating idea behind this type of feedback control is to shape the open loop gain of the system such that two objectives are achieved:

1. High gain is achieved at DC and low frequencies. This condition ensures low steady state error.

2. The gain at the plant's lowest frequency pole is less than or equal to OdB. This condition ensures a positive phase margin and, consequently, stability.

In the case of dominant pole compensation, these objectives are achieved using a compensator consisting of a single pole at a frequency well below those of the plant's poles. In our design, an integrator, which is just a pole at DC, is employed

$$G_c(s) = \frac{\omega_I}{s}$$

where $\omega_I = 2\pi \cdot f_I$ is an appropriately chosen design constant. Figure 5.11 shows the Bode plot asymptotes for the magnitude and phase of this compensator.

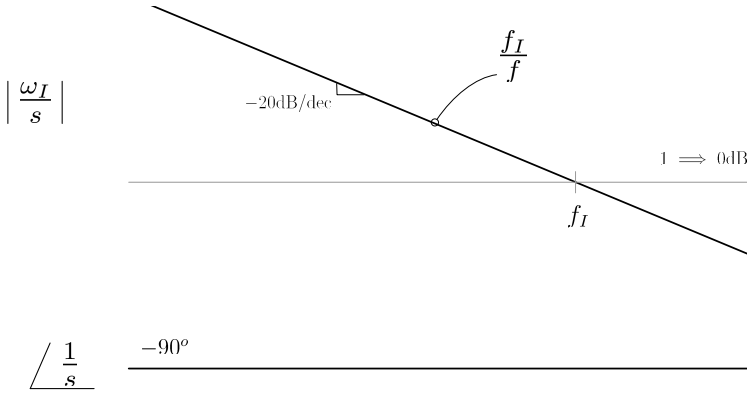


Figure 5.11: Bode Plot: Dominant Pole Compensator

Design of the compensator now consists of selecting an appropriate compensator parameter, f_I.

Figure 5.12 shows the graphical construction of the phase asymptotes for the loop gain with the compensator. Note that because the plant's transfer function is third order, it contributes a phase shift of $-270°$ at high frequencies and a shift of exactly $-45°$ at f_1. Furthennore, the compensator contributes its own $-90°$ phase shift and does so for all frequencies. Consequently, the total phase shift of the compensated open loop transfer function is $-135°$ at the dominant pole frequency (first pole), f_1. For this reason it is prudent to design this frequency f_1 to be the cut-off frequency of the overall system, so that we get a $+45°$ phase margin.

Figure 5.13 shows how the plant and compensator transfer functions combine to produce the gain of the compensated open loop. To achieve a phase margin that is $+45°$, we require the magnitude at f_1 to equal 1 (OdB).

$$\frac{f_I T_o}{f_1} = 1$$

$$f_I = \frac{f_1}{T_o} = \frac{10}{250} = 0.04$$

The dominant pole compensator in this case is:

$$G_c(s) = \frac{\omega_I}{s} = \frac{2\pi \cdot 0.04}{s}$$

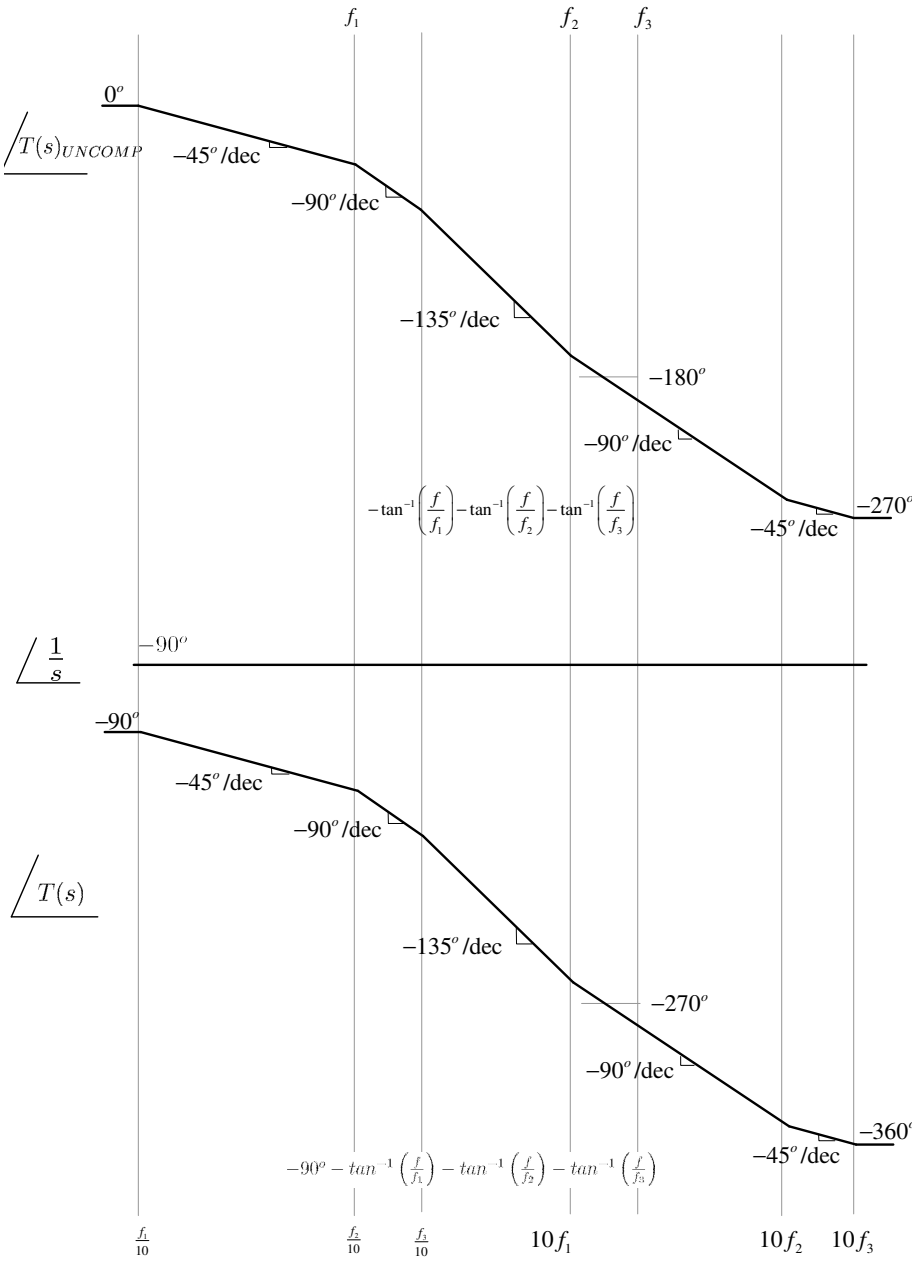


Figure 5.12: Dominant Pole: Phase Construction

Figure 5.14 shows the Bode plot of the resulting gain and phase asymptotes and Figure 5.15 shows a Matlab margin analysis which confirms the design.

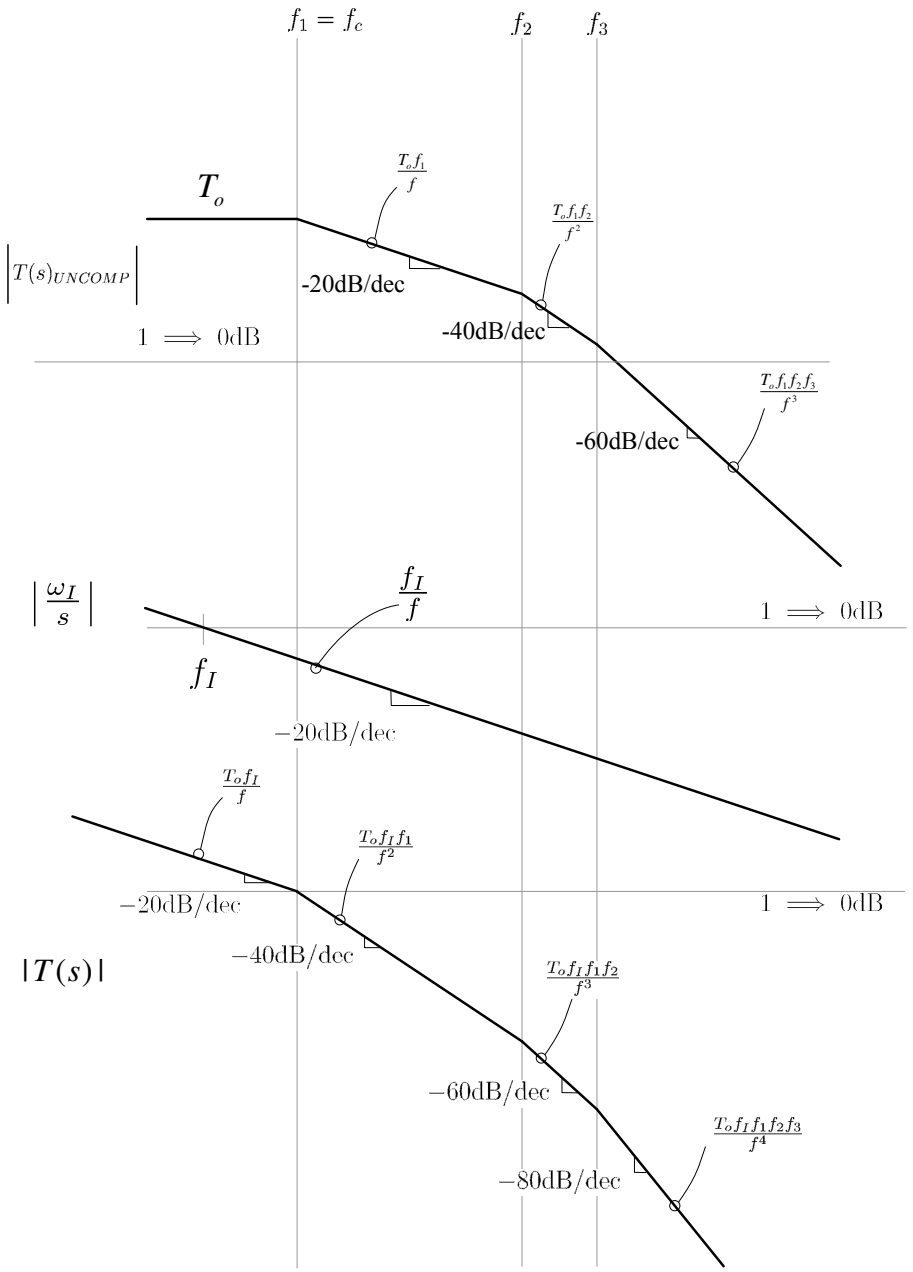


Figure 5.13: Dominant Pole: Magnitude Construction

$$\frac{numc\,(s)}{denc\,(s)} = G_c\,(s) = \frac{\omega_I}{s} = \frac{2\pi \cdot 0.04}{s}$$

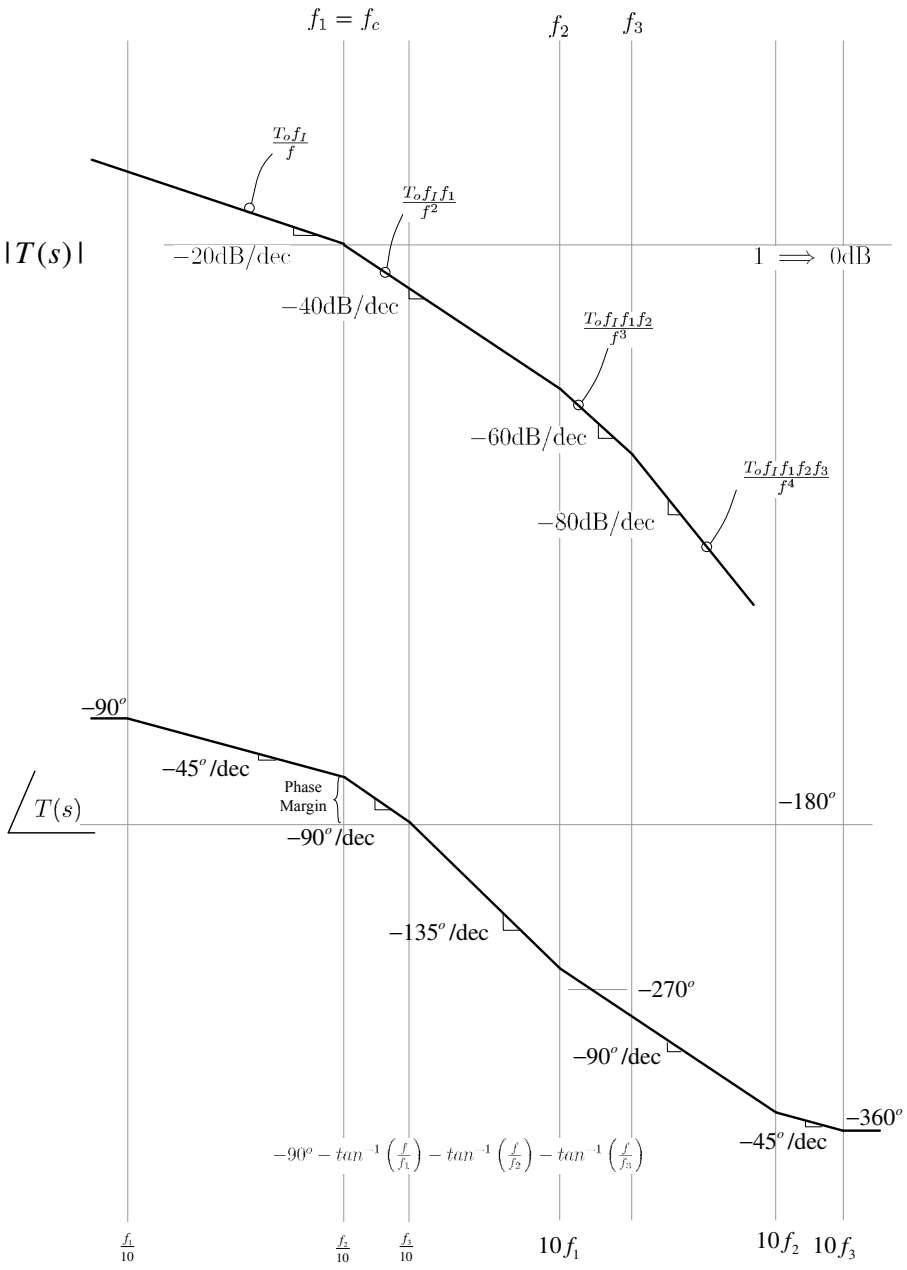


Figure 5.14: Dominant Pole Compensated System

$$\frac{numg\,(s)}{deng\,(s)} = G\,(s) = \frac{G_o}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)}$$

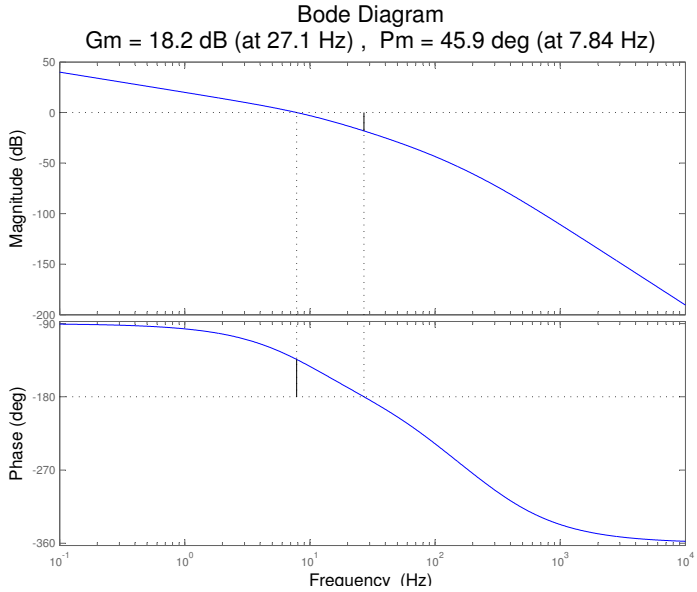


Figure 5.15: Matlab Analysis of Dominant Pole Compensated System

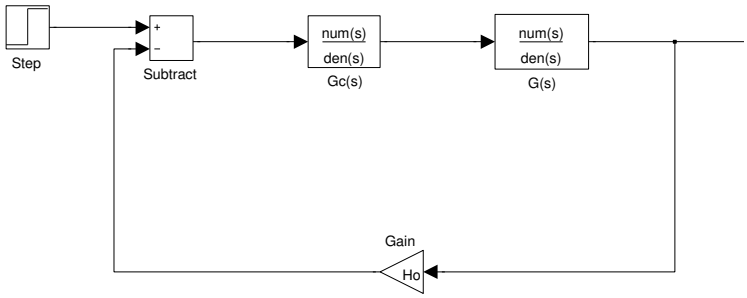


Figure 5.16: Simulink schematic of the Compensated System

Dominant Pole Compensation		
Characteristics	Value	Unit
Peak amplitude	2.44 (22.2% overshoot)	N/A
Rise time	24.7	ms
Settling time	134	ms
Steady-state error	0	N/A
Bandwidth	7.84	Hz
Phase margin	45.9	degree
Gain margin	18.2	dB

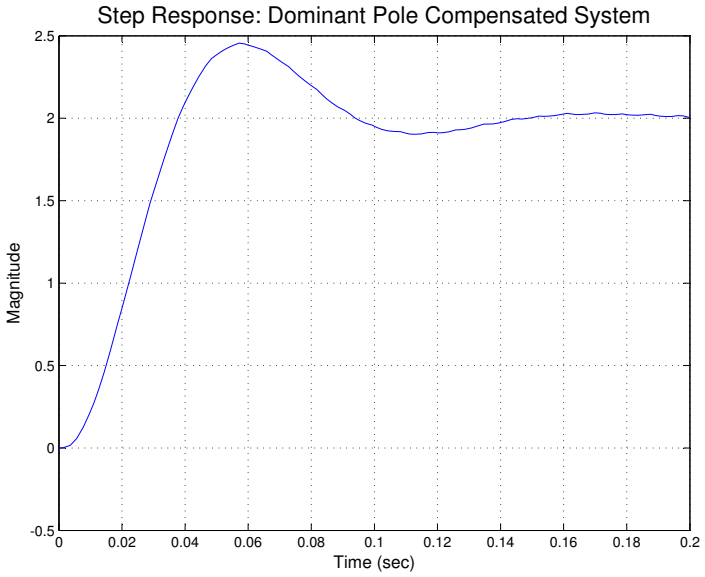


Figure 5.17: Step Response of the Dominant Pole Compensated System

It is clear from the simulation results that, although the design is stable and exhibits zero steady-state error, there is much room for improvement, particularly with respect to its transient response. A large overshoot still presents in the response.

The dominant pole compensator of the previous section, while stable and having zero steady state error, exhibits several undesirable characteristics including large overshoot and long settling time.

The reason is that when we compensate to make the system stable, we sacrifice all of the bandwidth of the system. The naJ.Tower the bandwidth is, the slower the response is. Thus, we need to make the bandwidth wider to speed up the response.

In order to do that, we add a zero to the compensator that will cancel the first pole of the system that is at, very low frequency. By doing that, the next pole at 100Hz now becomes the dominant pole that we will compensate for.

The transfer function for the compensator in this case is chosen to be

$$G_c(s) = \omega_I \frac{1 + \frac{s}{\omega_z}}{s} = \omega_I \frac{1 + \frac{s}{2\pi(10)}}{s}$$

The combine transfer function for the loop gain is:

$$T(s) = \frac{T_o}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)} \cdot \omega_I \frac{\left(1+\frac{s}{\omega_z}\right)}{s} = \frac{T_o \omega_I}{s\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)}$$

Using the same method as before, we choose W2 to be the cut-off frequency to get the phase margin of $+45°$.

$$\frac{f_I T_o}{f_2} = 1$$

$$f_I = \frac{f_2}{T_o}$$

The dominant pole compensator with zero in this case is:

$$G_c(s) = \omega_I \frac{1+\frac{s}{2\pi(10)}}{s} = 2\pi \cdot 0.4 \cdot \frac{1+\frac{s}{2\pi(10)}}{s}$$

The margin plot from MATLAB is

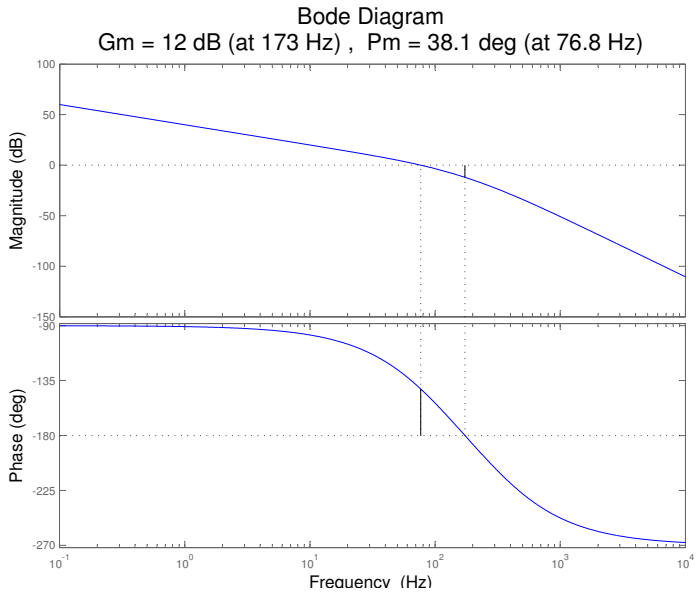


Figure 5.18: Matlab Analysis of Dominant Pole Compensated System with Zero

The bandwidth of the system indeed increases by a factor of 10.

However, the phase margin is not 45° as we expect. Because the next pole is at 300Hz, this pole actually contributes phase shift at the cut-off frequency.

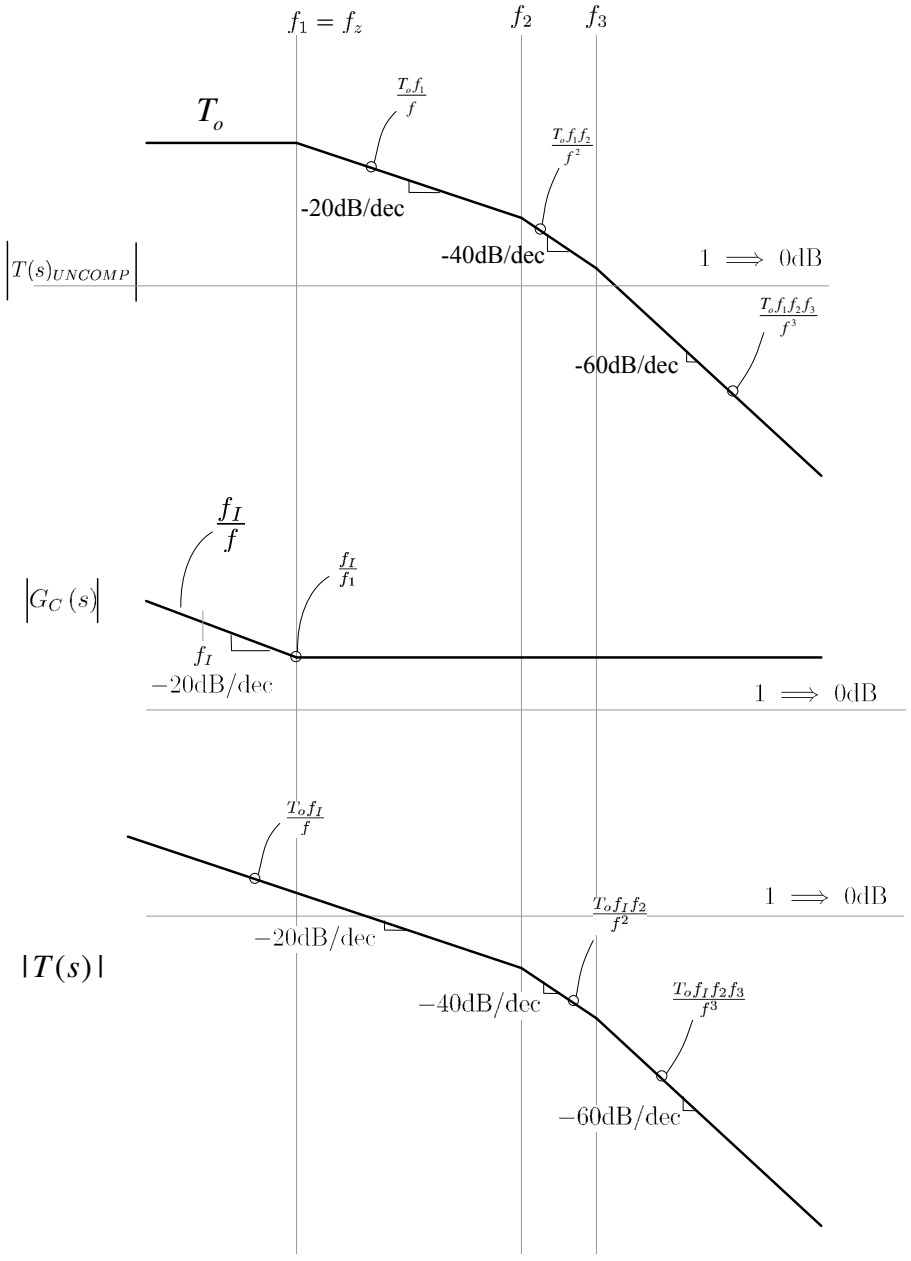


Figure 5.19: Dominant Pole with Zero Magnitude Construction

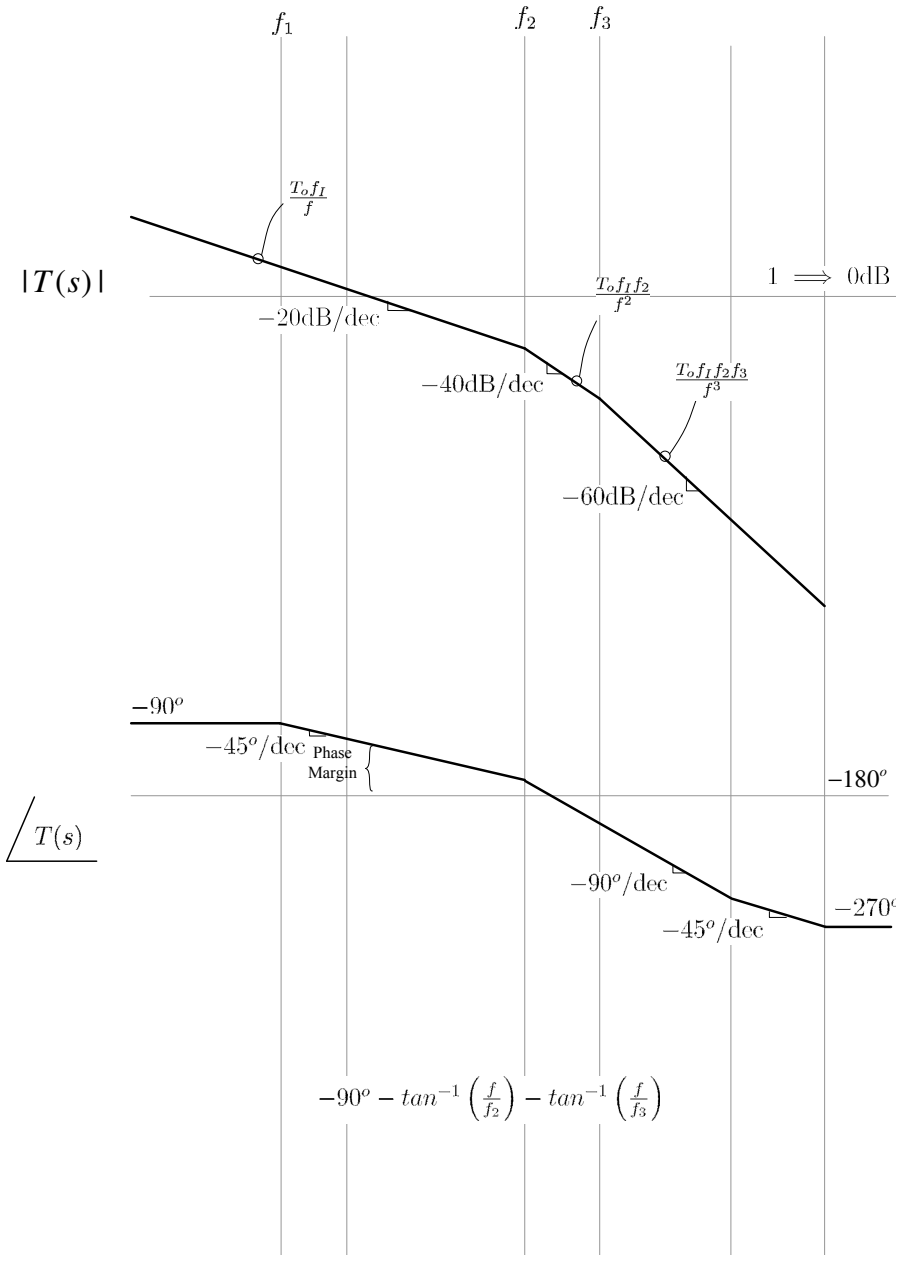


Figure 5.20: Dominant Pole with Zero Compensated System

To get the desired phase margin, we must lower the cut-off frequency

$$G_c(s) = \omega_I \frac{1 + \frac{s}{2\pi(10)}}{s} = 2\pi \cdot 0.3 \cdot \frac{1 + \frac{s}{2\pi(10)}}{s}$$

The margin plot from MATLAB is

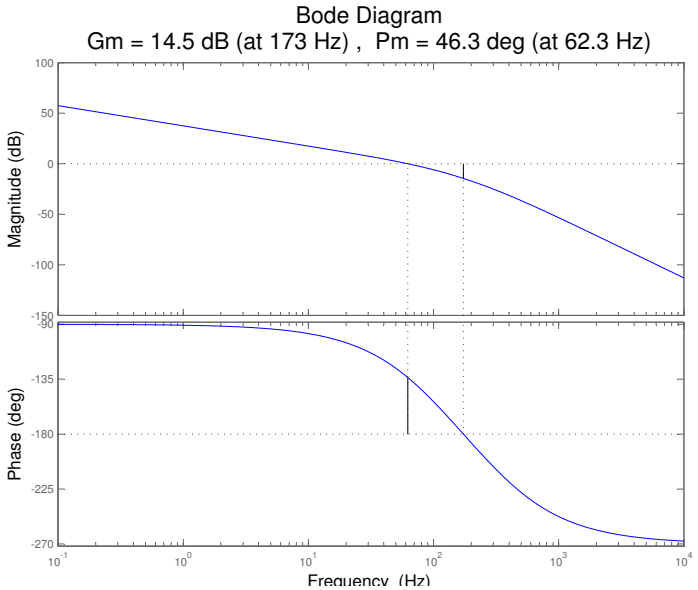


Figure 5.21: Matlab Analysis of Dominant Pole Compensated System with Zero

Dominant Pole with Zero Compensation		
Characteristics	Value	Unit
Peak amplitude	2.44 (22.2% overshoot)	N/A
Rise time	3.05	ms
Settling time	16.7	ms
Steady-state error	0	N/A
Bandwidth	62.3	Hz
Phase margin	46.3	degree
Gain margin	14.5	dB

The amount of overshoot is essentially the same due to the same phase margin. However, by extending the bandwidth of the system, the response is much faster.

To reduce the amount of overshoot, we increase the phase :margin to about 60°.

$$G_c(s) = \omega_I \frac{1 + \frac{s}{2\pi(10)}}{s} = 2\pi \cdot 0.15 \cdot \frac{1 + \frac{s}{2\pi(10)}}{s}$$

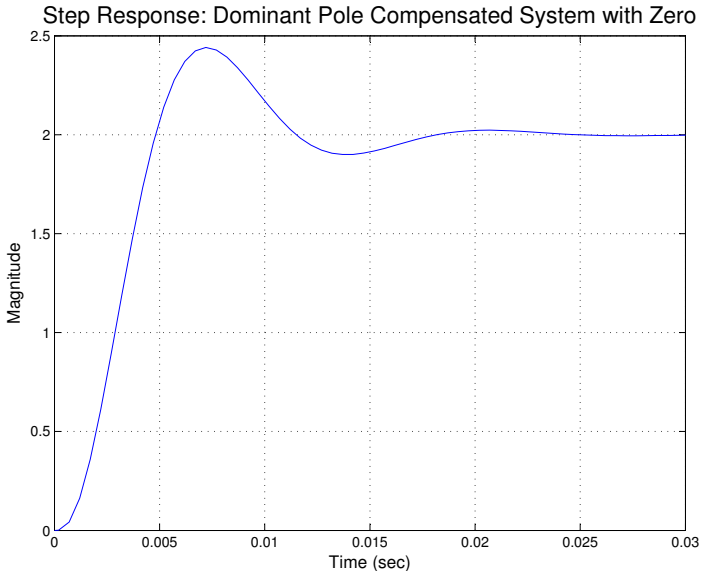


Figure 5.22: Step Response of the Dominant Pole with Zero Compensated System

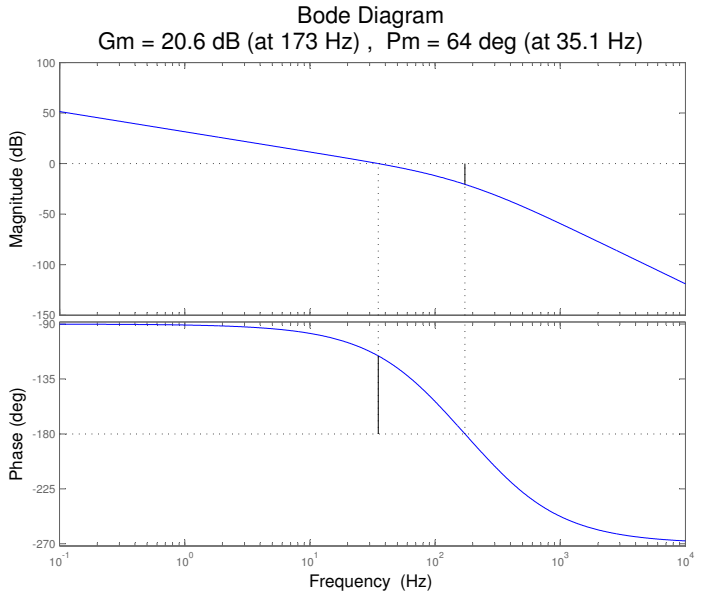


Figure 5.23: Matlab Analysis of Dominant Pole Compensated System with Zero (Improved Margin)

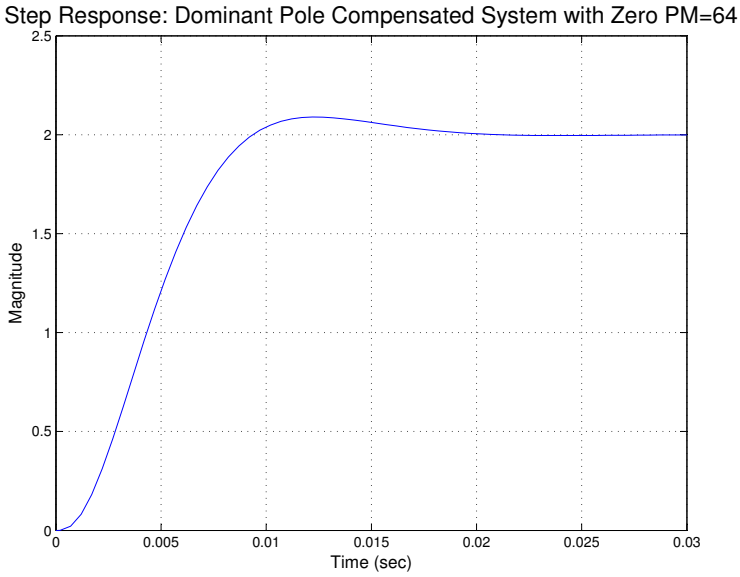


Figure 5.24: Step Response of the Dominant Pole with Zero Compensated System (Improved Margin)

Dominant Pole with Zero Compensation (Improved Margin)		
Characteristics	Value	Unit
Peak amplitude	2.09 (4.46% overshoot)	N/A
Rise time	5.81	ms
Settling time	16.5	ms
Steady-state error	0	N/A
Bandwidth	35.1	Hz
Phase margin	64	degree
Gain margin	20.6	dB

We can see that by increasing the phase margin, the amount of overshoot reduces significantly. On the other hand, the tradeoff is reducing the bandwidth, so the response is a little bit slower.

5.2.4 Lead Compensated System

A more sophisticated way to improve the performance of the system IS with a lead compensator. The transfer function of this compensator is

$$G_c(s) = G_{co}\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}}$$

where $\omega_z < \omega_p$. As can be seen from the plot of the transfer function shown in Figure 18, the lead compensator provides both a phase boost that is adjustable based on the pole and zero frequencies, and a gain boost at higher frequencies that can result· in a higher crossover frequency for a lead-compensated buck converter. Generally, a lead compensator is used to provide a phase boost, the level of which is chosen to improve the phase margin to a desired value. The new crossover frequency can be chosen arbitrarily. The design shown here will be to obtain a 60° phase margin for the loop gain with a lead compensator.

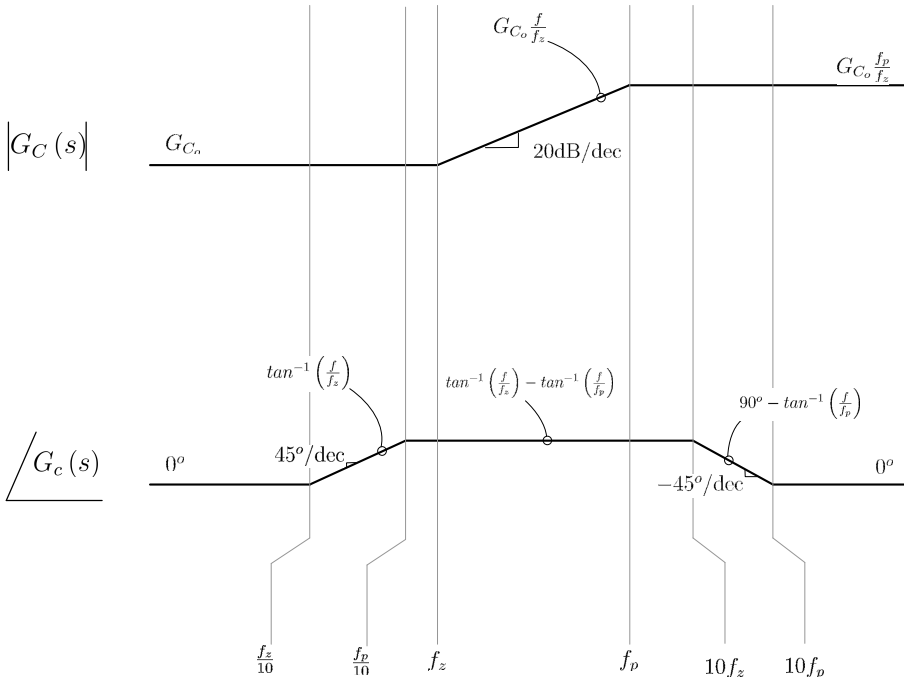


Figure 5.25: Bode Diagram: Lead Compensator

When the compensator is placed in the loop, the loop gain of the buck converter system becomes

$$T(s) = \frac{T_o G_{co}\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)}$$

The asymptotic Bode plot of this loop gain is shown in Figure 5.27. The expressions shown can be used to place the pole and zero frequencies of the compensator to obtain the desired phase margin and unity-gain crossover fre-

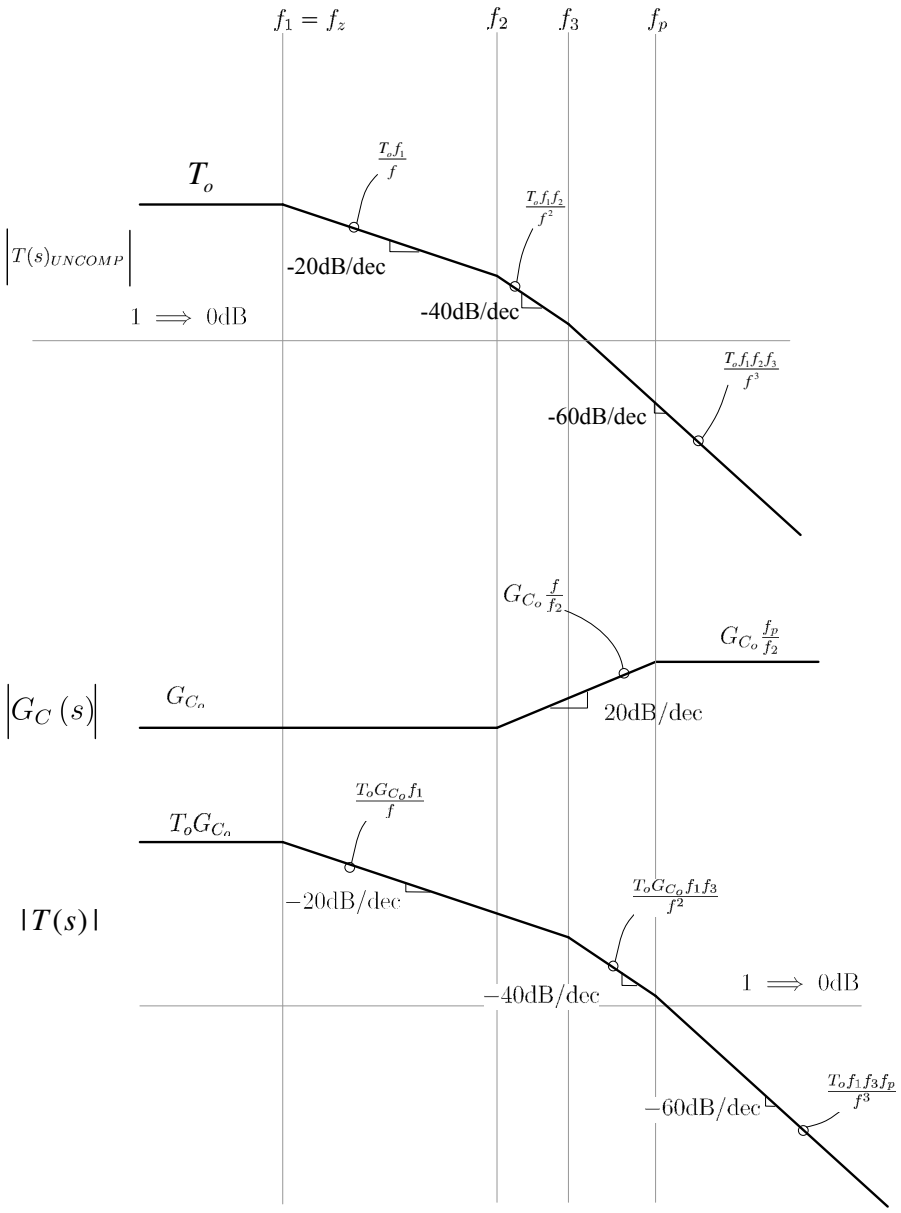


Figure 5.26: Lead Compensation Magnitude Construction

quency. As can be seen, the phase margin of the lead compensated system is given by

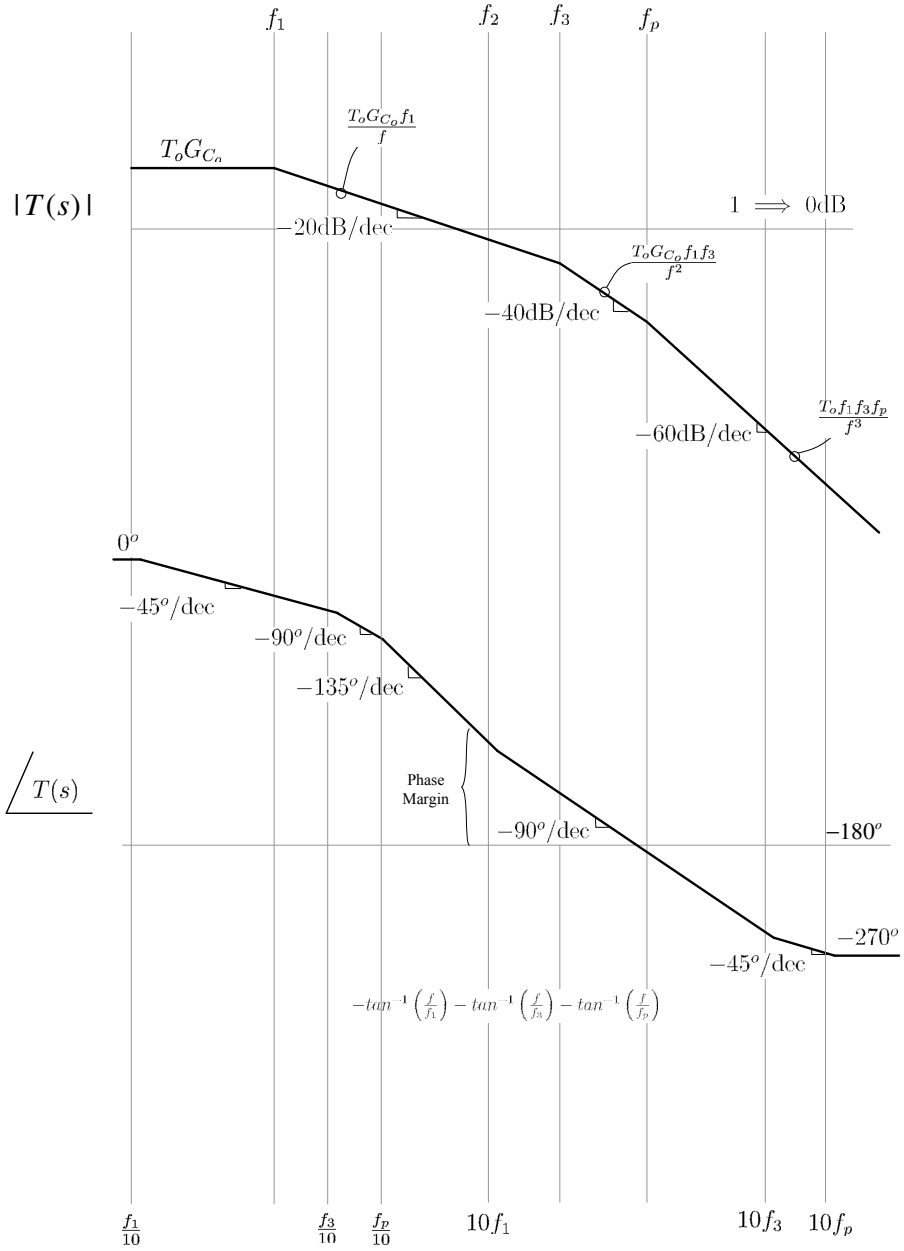


Figure 5.27: Lead Compensated System

$$\phi_M = 45° log\left(\frac{\omega_p}{\omega_z}\right)$$

We will add a phase boost of 30° to the system and move the cross-over frequency to get to desired phase margin (the more phase we want to get, the more separated the pole and zero are; we must put the zero at low frequency which will cause a slower response)

$$30^\circ = 45^\circ log\left(\frac{\omega_p}{\omega_z}\right)$$

$$\omega_p = 4.64\omega_z$$

Another thing is that we do not want to increase the order of the system so much, so that we will put the zero frequency at the pole frequency to cancel one of the poles. That means,

$$\omega_z = \omega_2 = 200\pi\frac{rad}{s}$$

$$\omega_p = 4.64\omega_z \approx 3000\frac{rad}{s}$$

The only parameter left is the gain of the compensator. We want to make the cross-over frequency at the frequency where the uncompensated system has the phase less than -180° (positive phase margin), so that when we add the phase boost of 30°, we get more than 60° phase margin.

From the bode plot of the uncompensated system, we choose the cross-over frequency of $f_c = 85Hz$, where the original system has the phase shift of -140°, so that with the phase boost of 30°, we get more than 60° phase margin.

$$\left|G_c(s)\,G(s)\,H(s)\right|_{s=j2\pi f_c} = 1$$

From this condition, we find $G_{co} = 0.0356$.

Therefore, the lead compensator transfer function is

$$G_c(s) = 0.0356\frac{1+\frac{s}{200\pi}}{1+\frac{s}{3000}}$$

The margin plot for the compensated system is

The gain margin is $71.2^\circ > 60^\circ$, the requirement that we set is met.

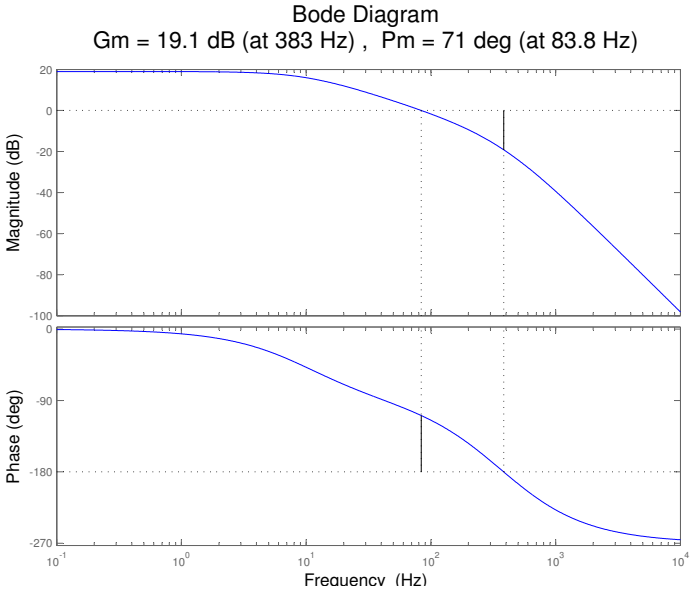


Figure 5.28: Matlab Analysis of Lead Compensated System

The unit step response of the system is

Lead Compensation		
Characteristics	Value	Unit
Peak amplitude	1.87 (4.23% overshoot)	N/A
Rise time	2.25	ms
Settling time	6.29	ms
Steady-state error	0.2(10%)	N/A
Bandwidth	83.8	Hz
Phase margin	71.2	degree
Gain margin	19.3	dB

We can see that the response is really fast due to the fact that the bandwidth is increased. However, there is steady-state en·or because no integrator is present in the loop.

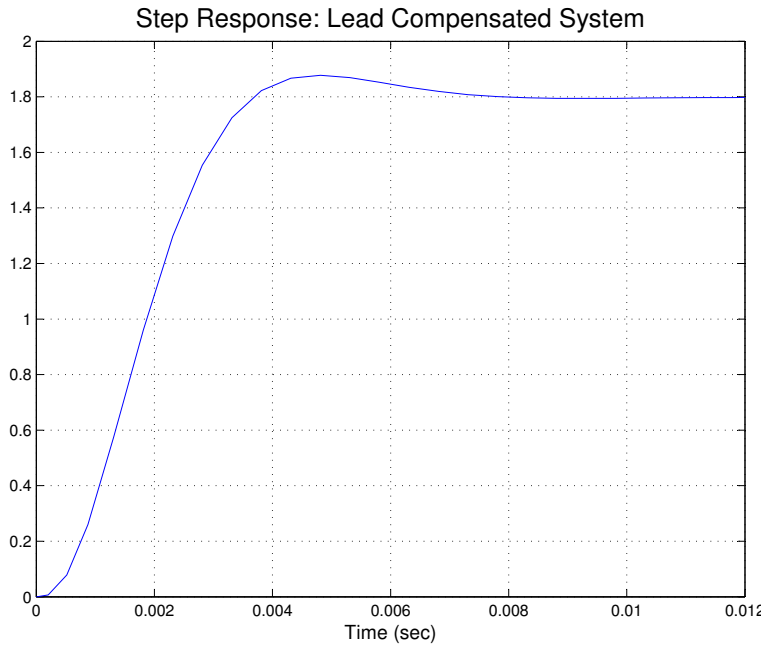


Figure 5.29: Step Response of the Lead Compensated System

5.2.5 Summary

Compensator Summary				
Compensator	Compensator transfer function	Phase margin (degree)	Bandwidth (Hz)	Steady-State
Dominant Pole	$\frac{2\pi \cdot 0.04}{s}$	45.9	7.84	2
Dominant Pole with zero (45° phase margin)	$2\pi \cdot 0.4\frac{1+\frac{s}{2\pi(10)}}{s}$	46.3	62.3	2
Dominant Pole with zero (60° phase margin)	$2\pi \cdot 0.15\frac{1+\frac{s}{2\pi(10)}}{s}$	64	35.1	2
Lead Compensator	$0.0356\frac{1+\frac{s}{200\pi}}{1+\frac{s}{3000}}$	71.2	83.8	1.8

5.2.6 MATLAB Code

```
1 clear all;
2 close all;
3
4 f = logspace(-1,4,1000);
```

```
5  w = 2*pi*f;
6  s = tf('s');
7
8  Go = 500;
9  w1 = 2*pi*10;
10 w2 = 2*pi*100;
11 w3 = 2*pi*300;
12 Ho = 0.5;
13 %=========================================================================
14 %UNCOMPENSATED
15 %=========================================================================
16 To=Go*Ho;
17 % z = [];
18 % p = [-w1 -w2 -w3];
19 % k = To*w1*w2*w3;
20 % sys = zpk(z,p,k)
21
22 sys = To/((1+s/w1)*(1+s/w2)*(1+s/w3));
23
24 figure(1)
25 [mag, phase] = bode(sys,w);
26 margin(mag, phase, w)
27
28 h = gcr;
29 h.AxesGrid.Xunits = 'Hz';
30 h.AxesGrid.TitleStyle.FontSize = 16;
31 h.AxesGrid.XLabelStyle.FontSize = 12;
32 h.AxesGrid.YLabelStyle.FontSize = 12;
33 %=========================================================================
34
35 %=========================================================================
36 %Dominant Pole Compensation
37 %=========================================================================
38 wI = w1/To;
39 sys2 = To*wI/(s*(1+s/w1)*(1+s/w2)*(1+s/w3));
40
41 figure(2)
42 [mag, phase] = bode(sys2,w);
43 margin(mag, phase, w)
44
45 h = gcr;
46 h.AxesGrid.Xunits = 'Hz';
47 h.AxesGrid.TitleStyle.FontSize = 16;
48 h.AxesGrid.XLabelStyle.FontSize = 12;
49 h.AxesGrid.YLabelStyle.FontSize = 12;
50
51 %=========================================================================
52
53
54
55
56
57 % Simulink Parameters
58 Gs = Go/((1+s/w1)*(1+s/w2)*(1+s/w3));
59 [num,den] = tfdata(Gs);
60 num = num{1};
61 den = den{1};
```

```
numc = [wI];
denc = [1 0];

% Plot of Simulink Step response results
plot(tout, yout);
grid on;
title('Step Response: Dominant Pole Compensated ...
    System','FontSize',16);
xlabel('Time (sec)','FontSize',12);
ylabel('Magnitude','FontSize',12);


%Time Domain Analysis Parameters
S = stepinfo(yout,tout,2)

%         RiseTime: 0.0247
%     SettlingTime: 0.1340
%      SettlingMin: 1.8911
%      SettlingMax: 2.4552
%        Overshoot: 22.7597
%       Undershoot: 1.5570e-57
%             Peak: 2.4552
%         PeakTime: 0.0572


%=========================================================================
%Dominant Pole With Zero Compensation
%=========================================================================
wI = w2/To;
wI = 2*pi*0.3
sys3 = To*wI/(s*(1+s/w2)*(1+s/w3));

figure(3)
[mag, phase] = bode(sys3,w);
margin(mag, phase, w)

h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;



% Simulink Parameters
Gs = Go/((1+s/w1)*(1+s/w2)*(1+s/w3));
[num,den] = tfdata(Gs);
num = num{1};
den = den{1};
Gc = wI*(1+s/w1)/s;
[numc,denc] = tfdata(Gc);
numc = numc{1};
denc = denc{1};



% Plot of Simulink Step response results
```

```
plot(tout, yout);
grid on;
title('Step Response: Dominant Pole Compensated System with ...
    Zero','FontSize',16);
xlabel('Time (sec)','FontSize',12);
ylabel('Magnitude','FontSize',12);
xlim([0 0.03]);


%Time Domain Analysis Parameters
S = stepinfo(yout,tout,2)

%         RiseTime: 0.0031
%     SettlingTime: 0.0167
%      SettlingMin: 1.8999
%      SettlingMax: 2.4408
%        Overshoot: 22.0402
%       Undershoot: 0
%             Peak: 2.4408
%         PeakTime: 0.0072

%=========================================================================


%=========================================================================
%Dominant Pole With Zero Compensation (Improved Phase Margin)
%=========================================================================
wI = 2*pi*0.15;
sys4 = To*wI/(s*(1+s/w2)*(1+s/w3));

figure(4)
[mag, phase] = bode(sys4,w);
margin(mag, phase, w)

h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;



% Simulink Parameters
Gs = Go/((1+s/w1)*(1+s/w2)*(1+s/w3));
[num,den] = tfdata(Gs);
num = num{1};
den = den{1};
Gc = wI*(1+s/w1)/s;
[numc,denc] = tfdata(Gc);
numc = numc{1};
denc = denc{1};



% Plot of Simulink Step response results
plot(tout, yout);
grid on;
```

```
174 title('Step Response: Dominant Pole Compensated System with Zero ...
        PM=64','FontSize',16);
175 xlabel('Time (sec)','FontSize',12);
176 ylabel('Magnitude','FontSize',12);
177 xlim([0 0.03]);
178
179
180 %Time Domain Analysis Parameters
181 S = stepinfo(yout,tout,2)
182
183 %          RiseTime: 0.0058
184 %      SettlingTime: 0.0165
185 %       SettlingMin: 1.8189
186 %       SettlingMax: 2.0893
187 %         Overshoot: 4.4660
188 %        Undershoot: 0
189 %              Peak: 2.0893
190 %          PeakTime: 0.0122
191
192 %=========================================================================
193
194
195
196
197 %=========================================================================
198 %Lead Compensation
199 %=========================================================================
200 Gco=0.0356;
201 wz = w2;
202 wp = 4.64*wz;
203
204 sys5 = To*Gco/((1+s/w1)*(1+s/w3)*(1+s/wp));
205
206 figure(5)
207 [mag, phase] = bode(sys5,w);
208 margin(mag, phase, w)
209
210 h = gcr;
211 h.AxesGrid.Xunits = 'Hz';
212 h.AxesGrid.TitleStyle.FontSize = 16;
213 h.AxesGrid.XLabelStyle.FontSize = 12;
214 h.AxesGrid.YLabelStyle.FontSize = 12;
215
216
217
218 % Simulink Parameters
219 Gs = Go/((1+s/w1)*(1+s/w2)*(1+s/w3));
220 [num,den] = tfdata(Gs);
221 num = num{1};
222 den = den{1};
223 Gc = Gco*(1+s/w2)/(1+s/wp);
224 [numc,denc] = tfdata(Gc);
225 numc = numc{1};
226 denc = denc{1};
227
228
229
```

```
% Plot of Simulink Step response results
plot(tout, yout);
grid on;
title('Step Response: Lead Compensated System','FontSize',16);
xlabel('Time (sec)','FontSize',12);
ylabel('Magnitude','FontSize',12);
xlim([0 0.012]);


%Time Domain Analysis Parameters
S = stepinfo(yout,tout,2)

%          RiseTime: 0.0029
%      SettlingTime: NaN
%       SettlingMin: 1.7943
%       SettlingMax: 1.8777
%         Overshoot: 0
%        Undershoot: 0
%              Peak: 1.8777
%          PeakTime: 0.0048
```

Chapter 6

Droop and Multi-Loop Control

()

Abstract

Constant output voltage is an important feature of a DC voltage regulator. This paper describes three compensation techniques including voltage droop, inductor current droop, and voltage compensation to minimize voltage deviation to changes in the output load of the system. Through simulation it is confirmed that droop compensation improves voltage deviation by a factor of two in comparison to traditional voltage compensation.

6.1 Introduction

In DC-DC voltage regulators, it is important to supply a constant voltage, regardless of the current load on the output. The goal of this paper is to describe three feedback compensation techniques for the Buck converter to limit the voltage deviation in response to a current step on the output. The designs to be implemented include a voltage droop compensator [1], an inductor current compensator [2], and a conventional voltage compensation circuit. For this design, resistive losses will be included for the inductor and the capacitor to provide a more complete and accurate analysis.

6.2 Design

6.2.1 Passive Droop Compensation

Concept of droop control

As discussed in [1], the basic concept behind droop control is to apply compensation to the Buck converter in a way that creates a constant, closed-loop output impedance. By creating a constant output impedance, any variation in load current will result in a change in output voltage to maintain a constant impedance. Knowing the maximum load current requirements, the maximum droop of the system is simply $\Delta V = \Delta IR$.

Reviewing the output section of the buck converter including losses, it can be seen that the open loop output impedance at high frequencies is equal to the parasitic resistance of the output capacitor. For this design, the parasitic resistance of the capacitor will be utilized as the value of the output impedance for the compensated Buck converter.

Derivation of the closed-loop output impedance

As shown in Figure 6.4, the output voltage variation of a Buck converter is determined based on the variation of the duty cycle, variations in the source

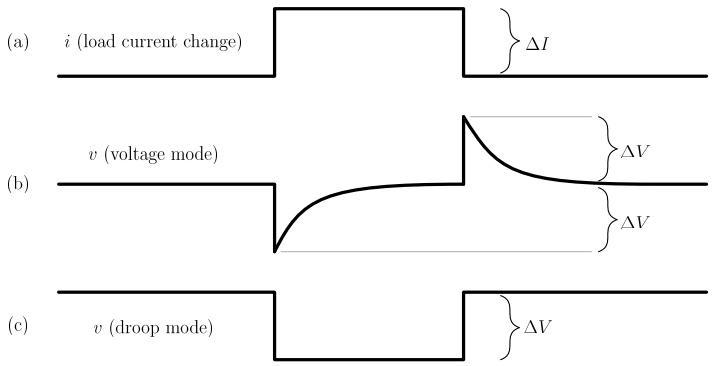


Figure 6.1: Transient Response of System with Droop Control

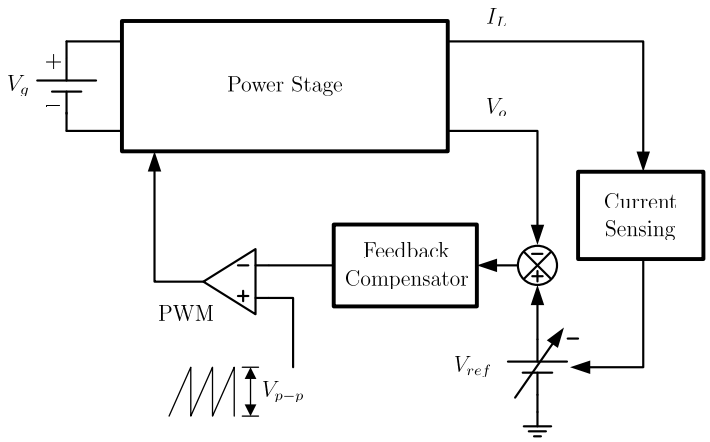


Figure 6.2: Active Droop Control System Block Diagram

voltage, and variations in the load current. For this example, input voltage variations will be neglected.

By definition,

$$Z_{oc}(s) = \frac{Z_o(s)}{1 + T(s)} \tag{6.1}$$

Following Figure 6.4, $T(s) = F_m H G_{vd}(s) G_{con}(s)$, where F_m is the PWM comparator effect, $G_{vd}(s)$ is the control to output transfer function, H is the feedback attentuation, and $G_{con}(s)$ is the compensation block to be designed.

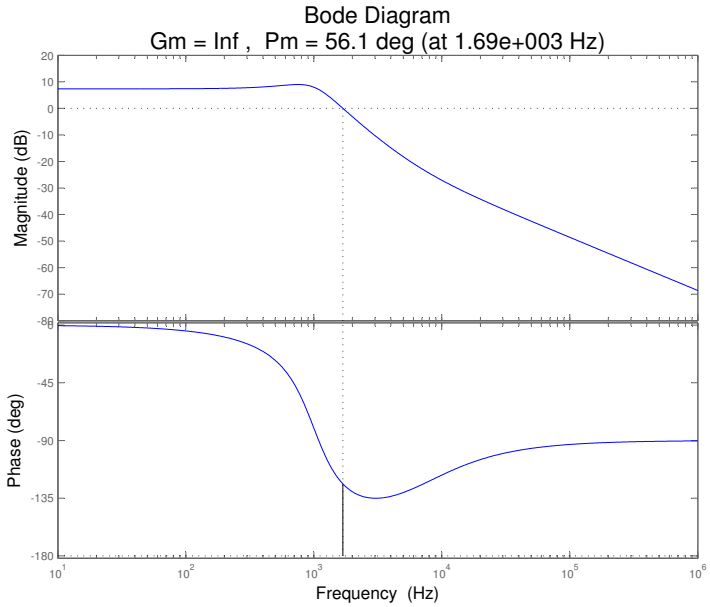


Figure 6.3: MATLAB Uncompensated Bode plot

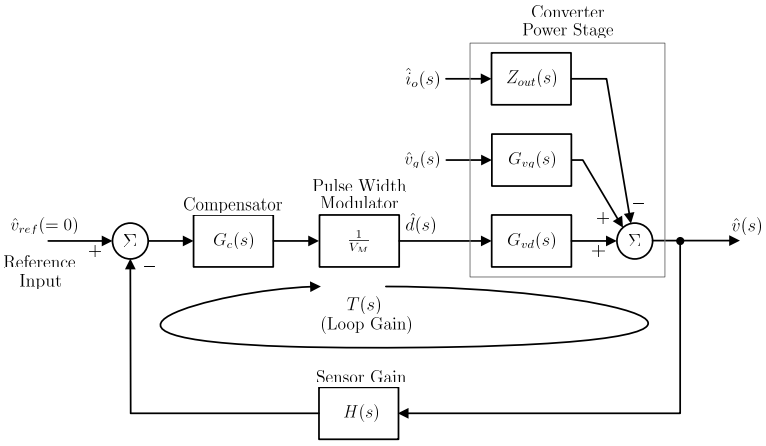


Figure 6.4: Buck converter control loop

To find $Z_{oc}(s)$ it is necessary to first calculate $Z_o(s)$ (the open loop output impedance) and $G_{vd}(s)$. Applying state space averaging methods to calculate the small signal model of $Z_o(s)$ and $G_{vd}(s)$, the functions are realized as shown below.

$$Z_o(s) = r_l \frac{(1+\frac{s}{\omega_c})(1+\frac{s}{\omega_l})}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \tag{6.2}$$

$$G_{vd}(s) = V_g \frac{1+\frac{s}{\omega_c}}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \tag{6.3}$$

Where $\omega_o \approx \frac{1}{\sqrt{CL}}$, $\omega_c = \frac{1}{r_c C}$, $\omega_l = \frac{r_l}{L}$, $\omega_R = \frac{1}{RC}$, and $Q \approx \frac{\sqrt{LC}}{r_l + r_c}$.

Recalling that our aim is to derive a compensator circuit that will implement a constant output impedance equal to the parasitic resistance of the capacitor, Z_{oc} is set equal to r_c.

$$Z_{oc}(s) = \frac{Z_o(s)}{1+T(s)} = \frac{Z_o(s)}{1+F_m G_{vd}(s) G_{con}(s)} = r_c$$

Expanding $Z_o(s)$ and $G_{vd}(s)$:

$$r_c = \frac{r_l \frac{(1+\frac{s}{\omega_l})(1+\frac{s}{\omega_c})}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}}}{1+\frac{F_m(1+\frac{s}{\omega_c})V_g}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} G_{con}(s)}$$

Rearranging the equation,

$$r_c F_m V_g (1+\frac{s}{\omega_c}) G_{con}(s) = r_l - r_c + [(\frac{1}{\omega_l}+\frac{1}{\omega_c})r_l - \frac{r_c}{Q\omega_o}]s + (\frac{r_l}{\omega_l \omega_c} - \frac{r_l}{\omega_o^2})s^2$$

Expanding the s^2 term,

$$\frac{r_l}{\omega_l \omega_c} - \frac{r_c}{\omega_o^2} = \frac{r_l}{\frac{r_l}{L}\frac{1}{r_c C}} - \frac{r_c}{\frac{1}{LC}} = r_c(LC - LC) = 0$$

$G_{con}(s)$ can then be simplified into the form:

$$G_{con}(s) = K_v \frac{1+\frac{s}{\omega_{zv}}}{1+\frac{s}{\omega_{pv}}} \tag{6.4}$$

Where $K_v = \frac{r_l - r_c}{r_c V_g F_m H}$,$\omega_{pv} = \omega_c$, and $\omega_{zv} = \frac{R_l - R_c}{L - R_c^2 C}$.

Using the circuit parameters defined in the introduction, $K_v = .1.71$, $\omega_{zv} = 4.1k\frac{\text{rad}}{s}$, and $\omega_{pv} = 40k\frac{rad}{s}$. For a Matlab calculation of these values, please refer to the MATLAB code provided at the end of the chapter.

Figure 6.5 show the frequency response of the loop gain of the system. Note that in this compensation design, a small gain at low frequencies is implemented, which is contrary to typical feedback designs where nearly infinite DC gain is desired.

In Figures 6.6 and 6.7, the open and closed loop output impedance and the system audio susceptibility are shown as a function of frequency. Note that as expected, the closed loop output impedance is approximately a constant $-26dB$ or $50m\Omega$ over the frequency range.

With the compensator circuit now completely defined, it can be realized using an operational amplifier circuit. As seen in Figure 6.8, the circuit can be implemented using a single op-amp.

Since the loop gain of this system is very low, it is not safe to assume that a reference of 5 V (V_oH) will work for this system. Looking at the block diagram, if the duty ratio is known, the output voltage of the amplifier is $\frac{D}{F_m}$. Using this value, the value of V_{ref} can found by applying nodal analysis at V_-. Using the DC value of D ($\frac{V}{V_g} = .53$), V_{ref} is found to be equal to approximately 3.9 V.

Through simulation of the droop circuit (Figure 6.8), it is found that the system performs exactly as expected for a step in current of 0.1 A to 5.0 A. With an output impedance of $50m\Omega$, the voltage change ideally would be equal to $\triangle V = (4.9A)(50m\Omega) = .245V$, which is approximately what is seen in Figure 6.8. In the next section, we will expand upon this design to incorporate additional compensation using the inductor current.

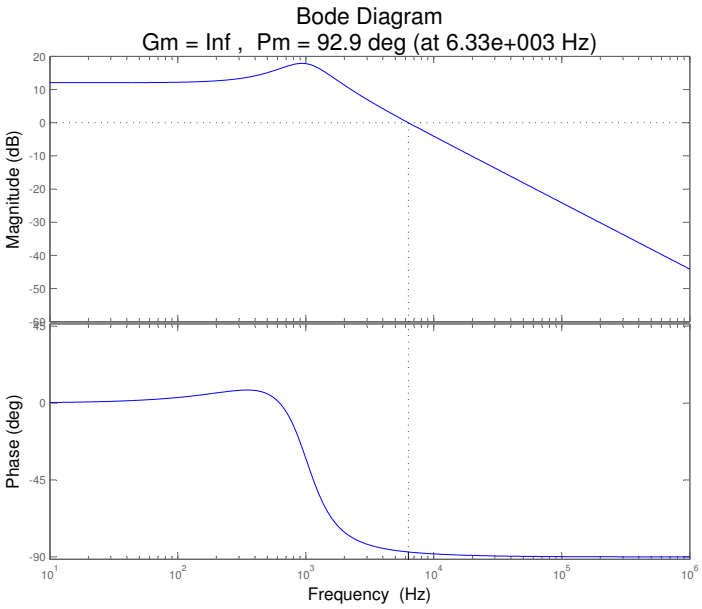


Figure 6.5: MATLAB Bode Plot of Loop Gain with Passive Droop Compensation

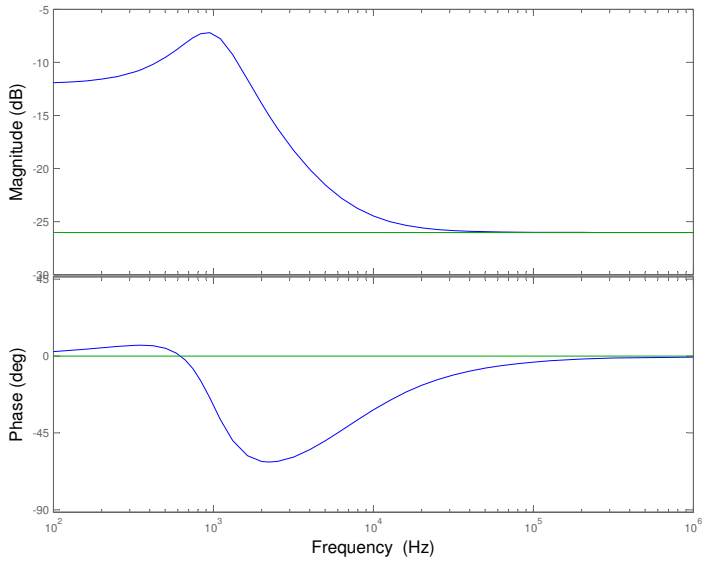


Figure 6.6: MATLAB Bode Plot of Z_o for Passive Droop Compensated System

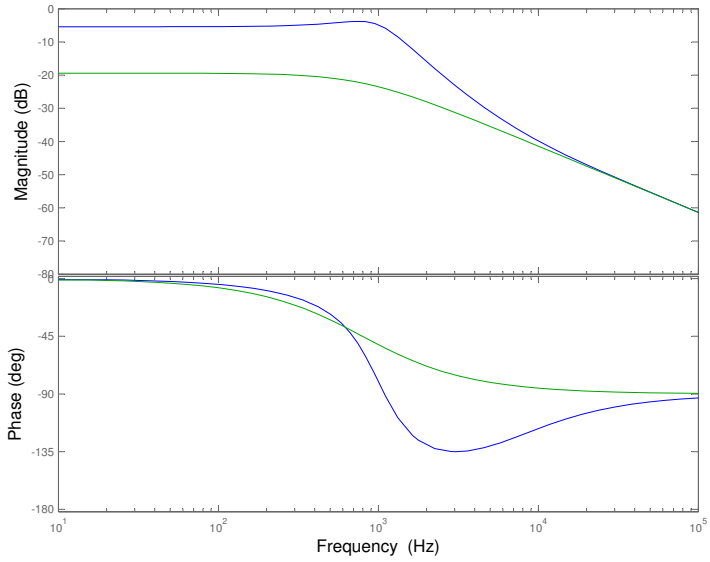


Figure 6.7: MATLAB Bode Plot of G_{vg} for Passive Droop Compensated System

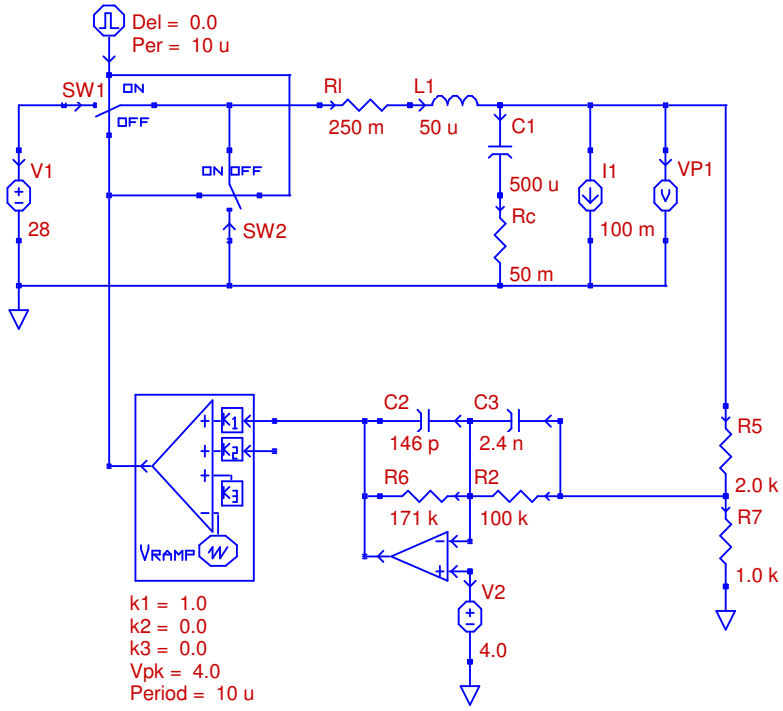


Figure 6.8: PECS Schematic of System with Passive Droop Compensation

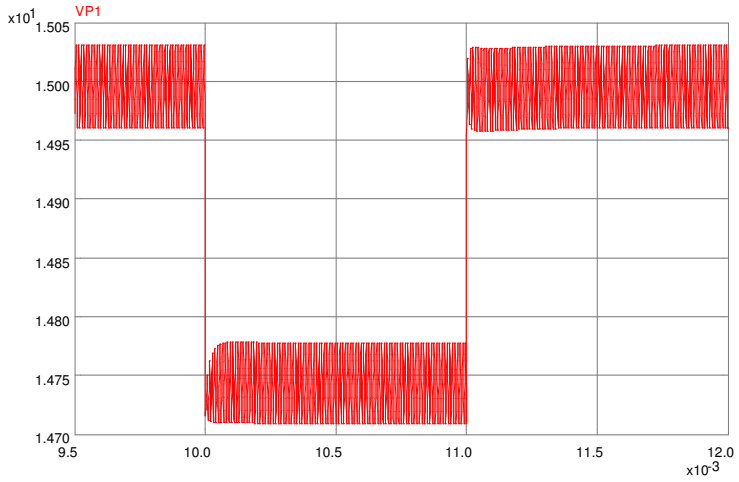


Figure 6.9: PECS Simulation of Passive Droop Compensation Response to a Load Current Step

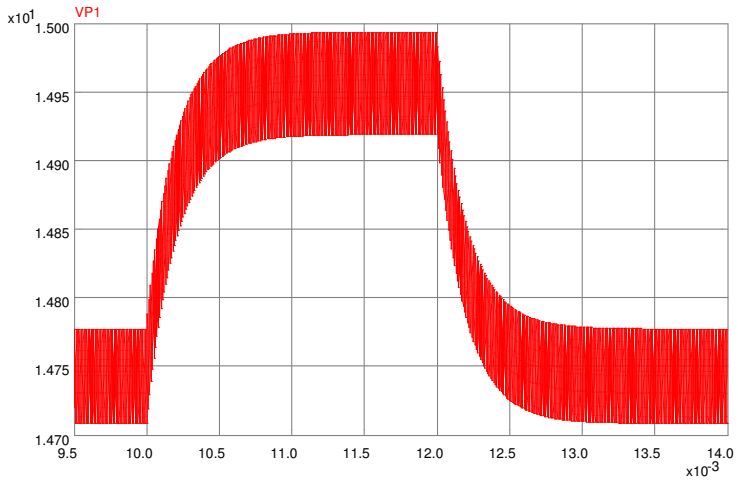


Figure 6.10: PECS Simulation of Passive Droop Compensation Response to a Supply Voltage Disturbance

6.2.2 Active Droop Compensation

Concept of Current Sensing Droop Control

This mode of control implements a constant output impedance equal to the parasitic resistance of the capacitor, similar to that of the previous section. However, this feedback system is composed of two loops. One loop is the voltage loop that was used in the Section 1 design. The second loop is a current sensing loop, which measures the inductor current and provides a feedback voltage proportional to this current. The goal of this design as presented in [2] is to combine these two loops into one compensator to control the deviation in the output voltage. This can be seen in Figure 6.11.

Figure 6.12 shows the current and voltage loops in terms of transfer functions via small-signal block diagram. $Z_o(s)$, $G_{vd}(s)$, and F_m are the same transfer functions used in the voltage droop mode. R_i is the inductor current sensing gain. $A_v(s)$ is the transfer function of the feedback compensator, and is synomynous to $G_{con}(s)$ in the voltage droop mode. $G_{ii}(s)$ is the transfer function of inductor current to load current. $G_{id}(s)$ is the transfer function of inductor current to duty cycle. Applying state space averaging methods to calculate the small signal model of $G_{ii}(s)$ and $G_{id}(s)$(see Appendix 1), the functions are realized as shown below.

$$G_{ii}(s) = \frac{1 + \frac{s}{\omega_c}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{6.5}$$

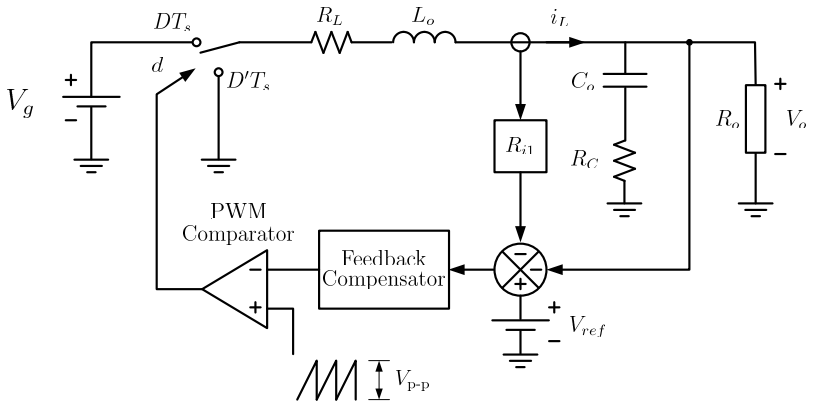


Figure 6.11: Buck converter with the current sensing mode [2]

$$G_{id}(s) = \frac{V_{in}}{R_o} \frac{1 + \frac{s}{\omega_R}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{6.6}$$

where $\omega_o \approx \frac{1}{\sqrt{CL}}$, $\omega_c = \frac{1}{R_c C}$, $\omega_l = \frac{R_l}{L}$, $\omega_R = \frac{1}{RC}$, and $Q \approx \frac{\sqrt{LC}}{R_l + R_c}$.

Design of Current Sensing Droop Control

To create a feedback compensator $A_v(s)$ for the current sensing droop control, the first step is realizing the functions for the current loop $T_i(s)$ and the voltage loop $T_v(s)$. This can be achieved by following each loop in Figure 6.12. For a complete diagram including input voltage disturbances, refer to Figure 6.20.

$$T_i(s) = A_v(s) F_m G_{id}(s) R_i \tag{6.7}$$

$$T_v(s) = A_v(s) F_m G_{vd}(s) \tag{6.8}$$

In order to determine a single compensator $A_v(s)$ for both loops, $T_i(s)$ and $T_v(s)$ need to be related. Because the compensator effects both loops, it is important to design the loops with the same characteristics. This allows both loops to be in unison and not work against each other. This can be achieved by designing both loops to have the same crossover frequency. This happens when the ratio of the two loops is set equal to 1.

$$\frac{T_v(s)}{T_i(s)} = \frac{G_{vd}(s)}{R_i G_{id}(s)} = \frac{R(1 + \frac{s}{\omega_c})}{R_i(1 + \frac{s}{\omega_R})} \tag{6.9}$$

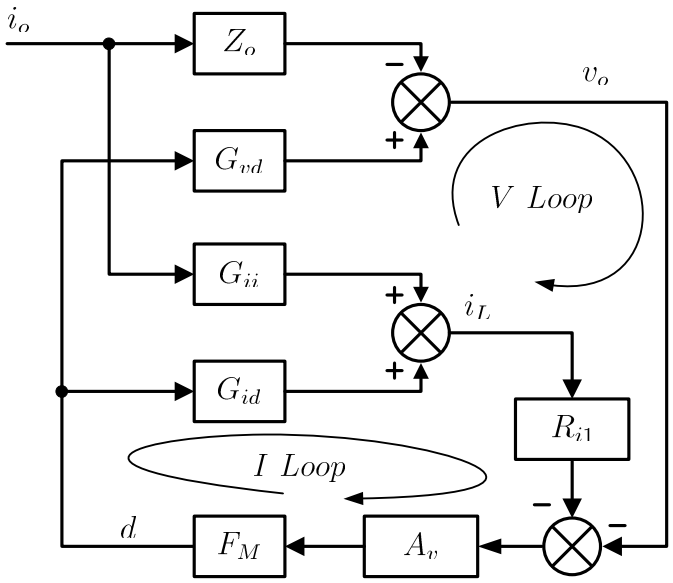


Figure 6.12: Small-signal block diagram of the current sensing mode

It can be seen that this ratio equals 1 when $R_i = R_c$ and when $\omega > \omega_c$, since the zero from the output capacitor is normally much larger than ω_R.

The design should be similar to the voltage droop control in terms of having a constant impedance gain equal to the parasitic losses of the output capacitor. The closed-loop output impedance function, $Z_{oc}(s)$, is shown below.

$$Z_{oc}(s) = \frac{Z_o(s)(1 + T_i(s)) + T_i(s)\frac{G_{vd}(s)G_{ii}(s)}{G_{id}(s)}}{1 + T_i(s) + T_v(s)} \tag{6.10}$$

Setting the above equation equal to the value of R_c the transfer function of $A_v(s)$ can be derived. From [2], the current loop should be stable with a phase margin of around 90°. In order to achieve this, a zero, ω_z, is needed to compensate for the power stage double pole. The high frequency switching noise should also be filtered. This requires a pole, ω_p, placed well before the switching frequency. The current loop should have a crossover frequency that is higher than the parasitic zero of the output capacitor. This can be done by making the gain, ω_i, of the compensator sufficiently large. Since infinite DC gain is required, an integrator is used by placing a pole at zero, $\frac{1}{s}$. The compensator transfer function can now be realized.

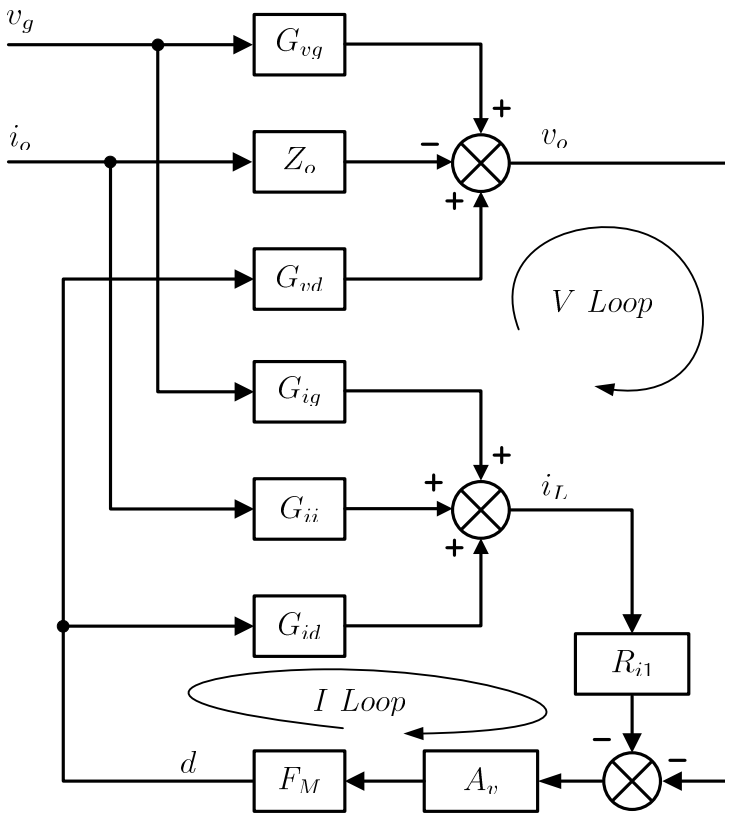


Figure 6.13: Small-signal block diagram of the current sensing mode -General

$$A_v(s) = \omega_i \frac{1 + \frac{s}{\omega_z}}{s(1 + \frac{s}{\omega_p})} \tag{6.11}$$

where $\omega_z = \omega_o$, $\omega_p = (2\pi)50,000$, and $\omega_i = 100,000$

The compensator can now be implemented using an operational amplifier circuit. As seen if Figure 6.17, this circuit can be implemented using a single op-amp. The summing of the two loops is incorporated into the op-amp used by the compensator. Please note the use of a voltage divider in the voltage feedback loop is similar to that in the previous section, only it has been scaled to a ratio of $\frac{1}{2}$ for component value selection.

The loop gain of this system is a ratio of the current and voltage loops, and once again it's not safe to assume a reference of 5 V will work for this system. V_{ref} is found to be approximately 3.8 V in this design.

Loop Gain Analysis

With the design stage complete, the system can be analyzed for stability and crossover frequency verification. The outer loop, T_2, shown below, determines the system stability.

$$T_2(s) = \frac{T_v(s)}{1 + T_i(s)} \tag{6.12}$$

It can be seen in Figure 6.14 that all three loops have the same crossover frequency. Stability is verified with T_2 having a phase margin of about 105°. This is really close to the design of 90°, with other poles and zeros from T_v and T_i accounting for the slight difference.

It can be observed in Figure 6.15 that the impedance gain is nearly constant. The impedance phase is also nearly constant as it changes only slightly over the entire range of frequencies.

In Figure 6.18, the current sensing droop control was simulated with a step in the load current, the same as was performed Section 1. The results are nearly the same as with the voltage droop control. There are slight transient spikes, but they are small and are on the order of the ripple. These spikes are caused from the slight deviation in the constant output impedance. With the output impedance at $50m\Omega$, the ideal voltage change would again be .245 V. Aside from the slight transient spikes, this is what is approximately seen in Figure 6.18. This two loop compensation control can achieve the same results as the simple voltage droop control, yet have the versatility to compensate for both voltage and current. In the next section, a voltage compensation scheme will be presented and compared to the droop control methods.

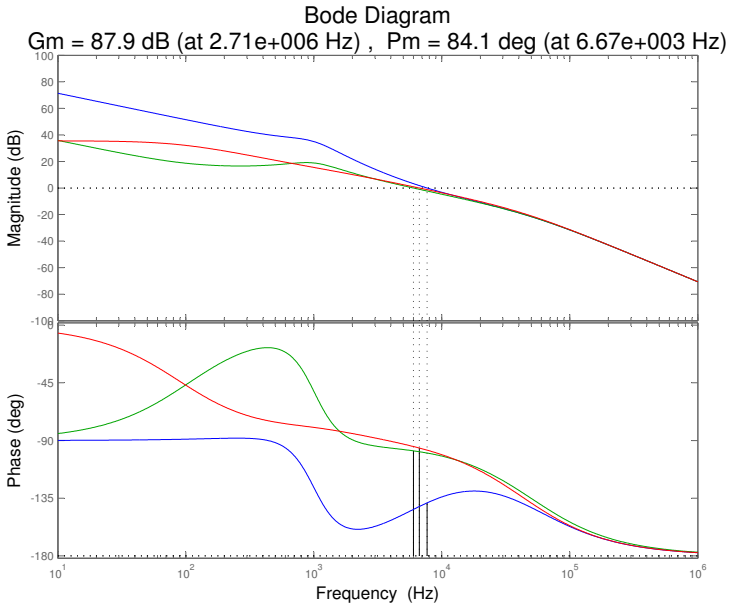


Figure 6.14: MATLAB Bode Plot of Loop Gains with Active Droop Compensation

6.2.3 Voltage Mode Compensation

Concept of voltage compensation

The final design that will be discussed in this report is a traditional voltage compensation design. Back in Figure 6.4, we found for the purposes of droop control that we would design for changes in output current and neglect any disturbances in the input voltage. For this design, the compensation circuit will be designed to reduce the audio susceptibility of the circuit ($G_{cl}(s) = \frac{\hat{v}}{\hat{v_g}}$). This design will then be tested by applying a step disturbance to the load current, and determining the maximum deviation of the output voltage in response to the disturbance.

By following the loop in Figure 6.4, it can be seen by inspection that $G_{cl}(s) = \frac{G_{vg}(s)}{1+T(s)}$, where $T(s) = G_{vd}(s)(Fm)G_{con}(s)$ and $G_{vd}(s)$ is the same as in Section 1 and Section 2. $G_{vg}(s)$ can be found to equal the following expression:

$$G_{vg}(s) = D\frac{1 + \frac{s}{\omega_c}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{6.13}$$

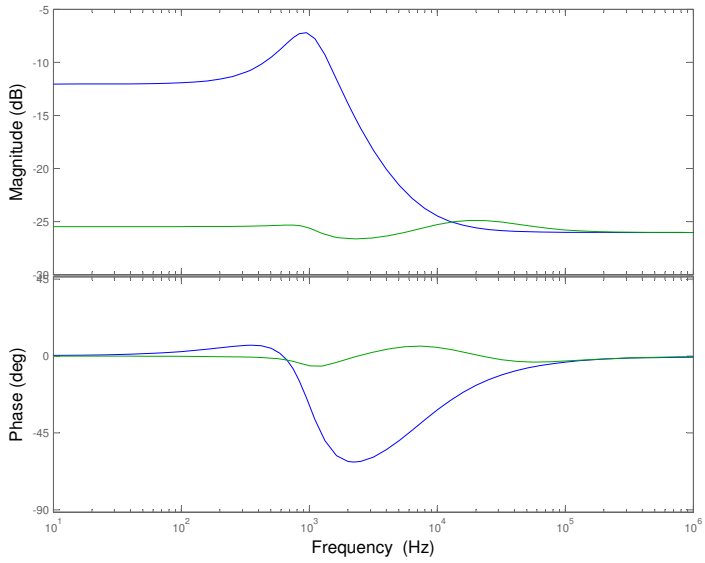


Figure 6.15: MATLAB Bode Plot of Z_o for Active Droop Compensated System

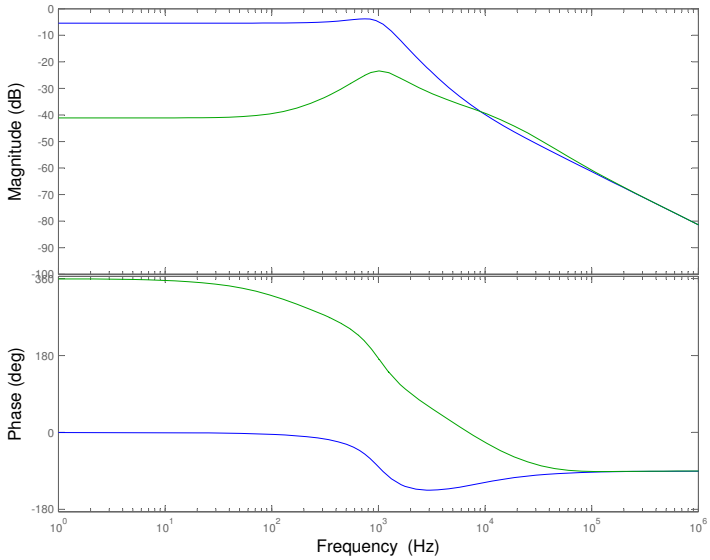


Figure 6.16: MATLAB Bode Plot of G_{vg} for Active Droop Compensated System

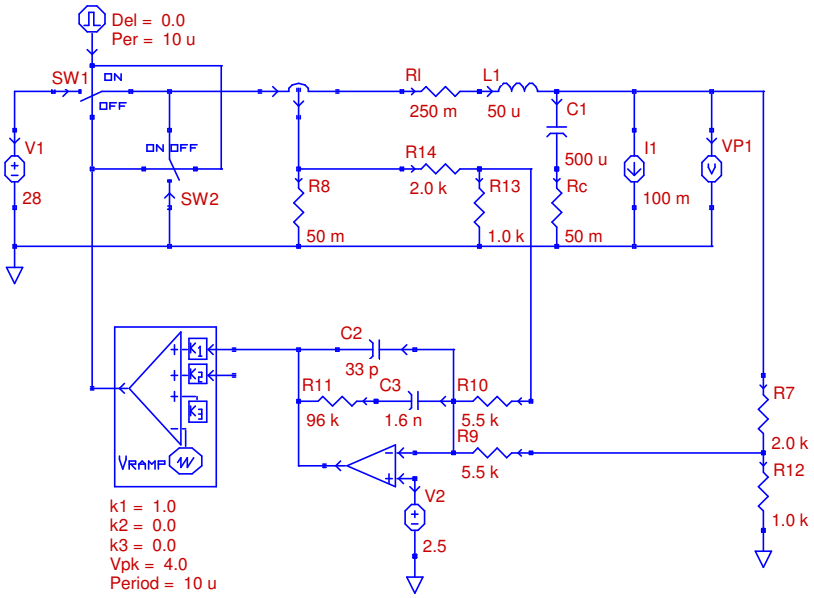


Figure 6.17: PECS Schematic of System with Active Droop Compensation

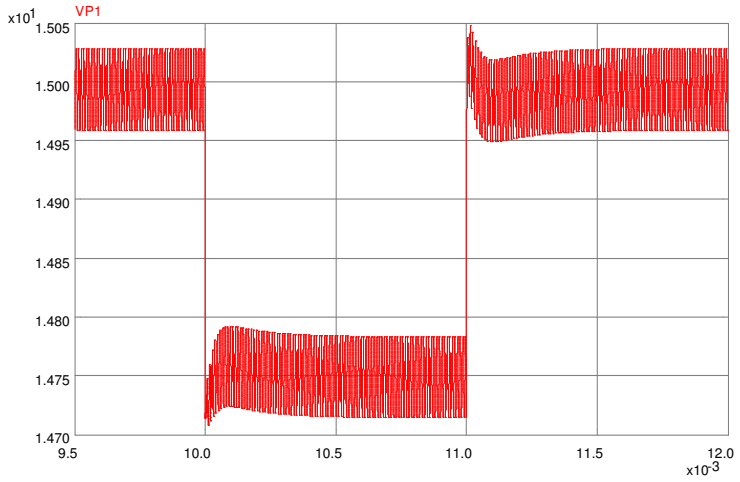


Figure 6.18: PECS Simulation of Active Droop Compensated Response to a Load Current Step

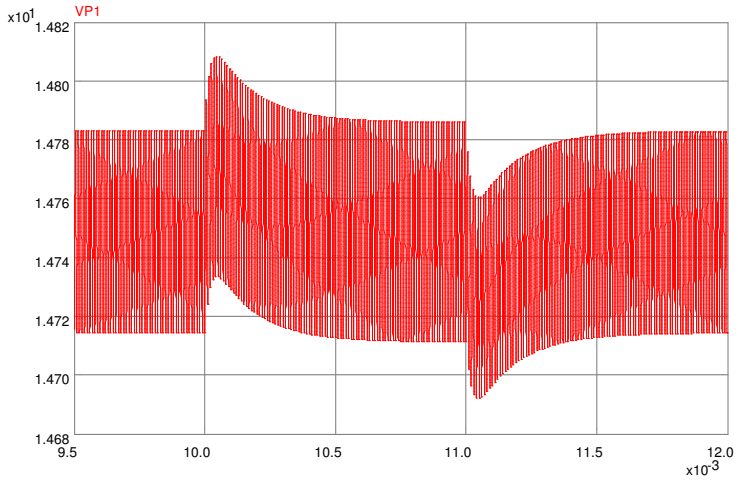


Figure 6.19: PECS Simulation of Active Droop Compensated Response to a Supply Voltage Disturbance

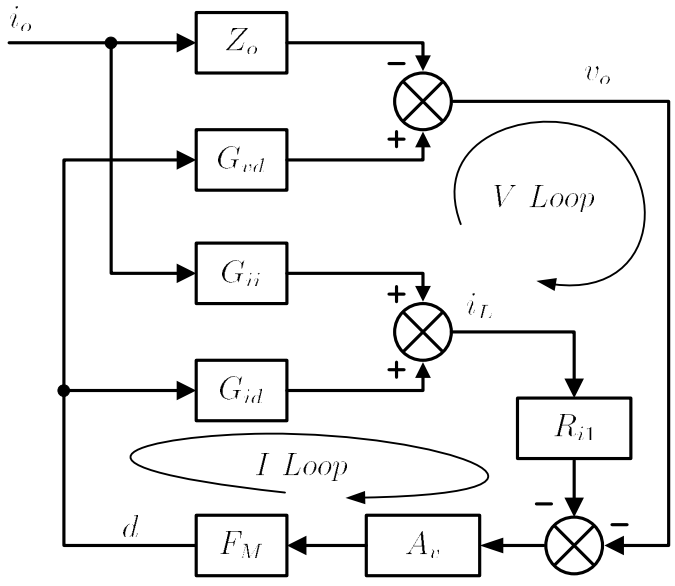


Figure 6.20: Complete Small-signal block diagram of the current sensing mode

Where all parameters of the equation are the same as described in the previous sections.

Designing loop compensation

The goal of this design is to create a compensation block that will maximally reduce the effect of input voltage disturbances on the output. To improve on the basic integrator compensator design, two zeros are added around the crossover frequency to combat the extra $-90°$ of phase shift introduced by the integrator. Two poles are also introduced to ensure that the switching frequency noise will be canceled with the introduction of the zero. The equation for this compensation block is shown below:

$$G_{con}(s) = \frac{\omega_I}{s} \frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \tag{6.14}$$

where ω_I is the constant gain and ω_{z1}, ω_{z2}, ω_{p1}, and ω_{p2} are the new parameters to be designed.

To gain a better understanding of the system, the system transfer functions are plotted for three different cases of zero placement:

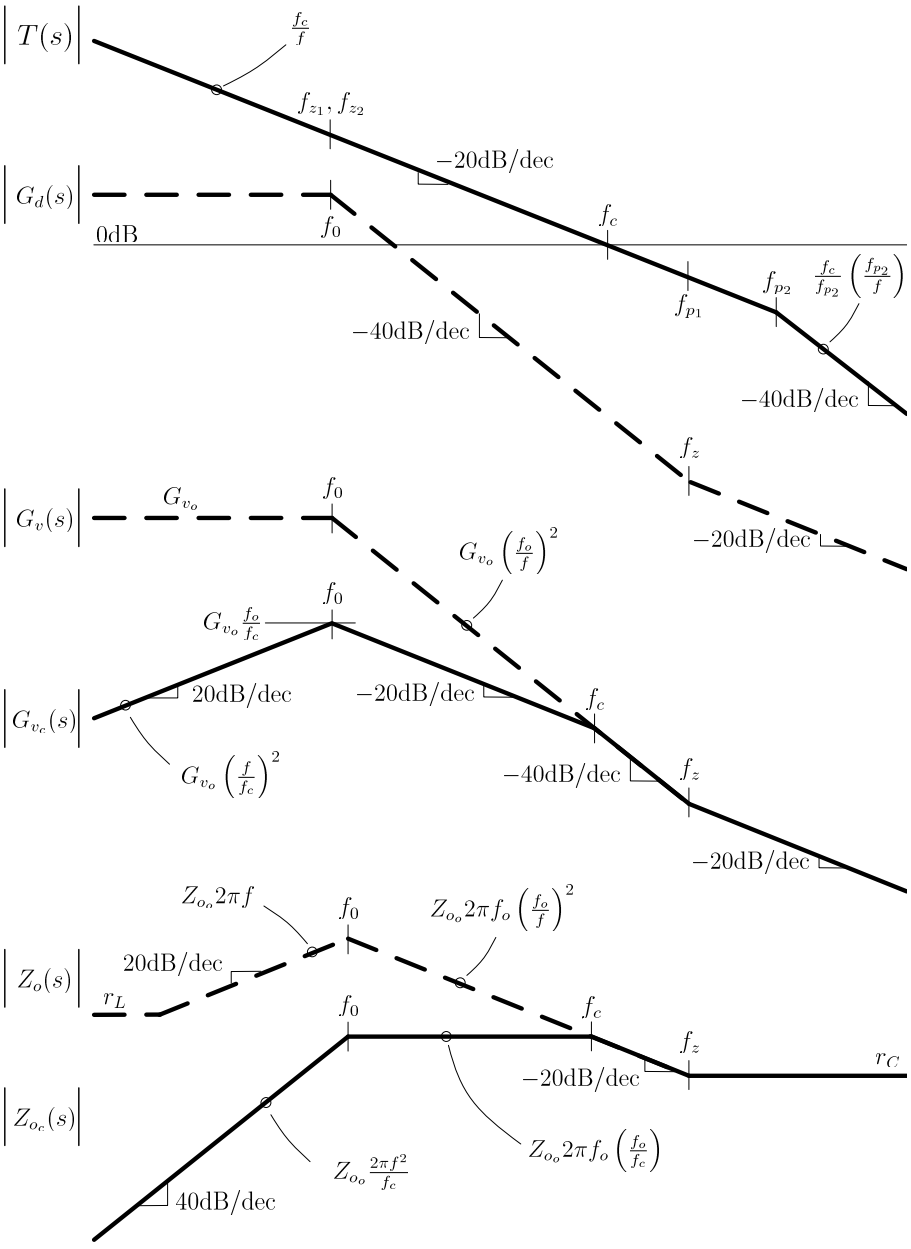


Figure 6.21: Bode Plot Asymptotes for Case 1

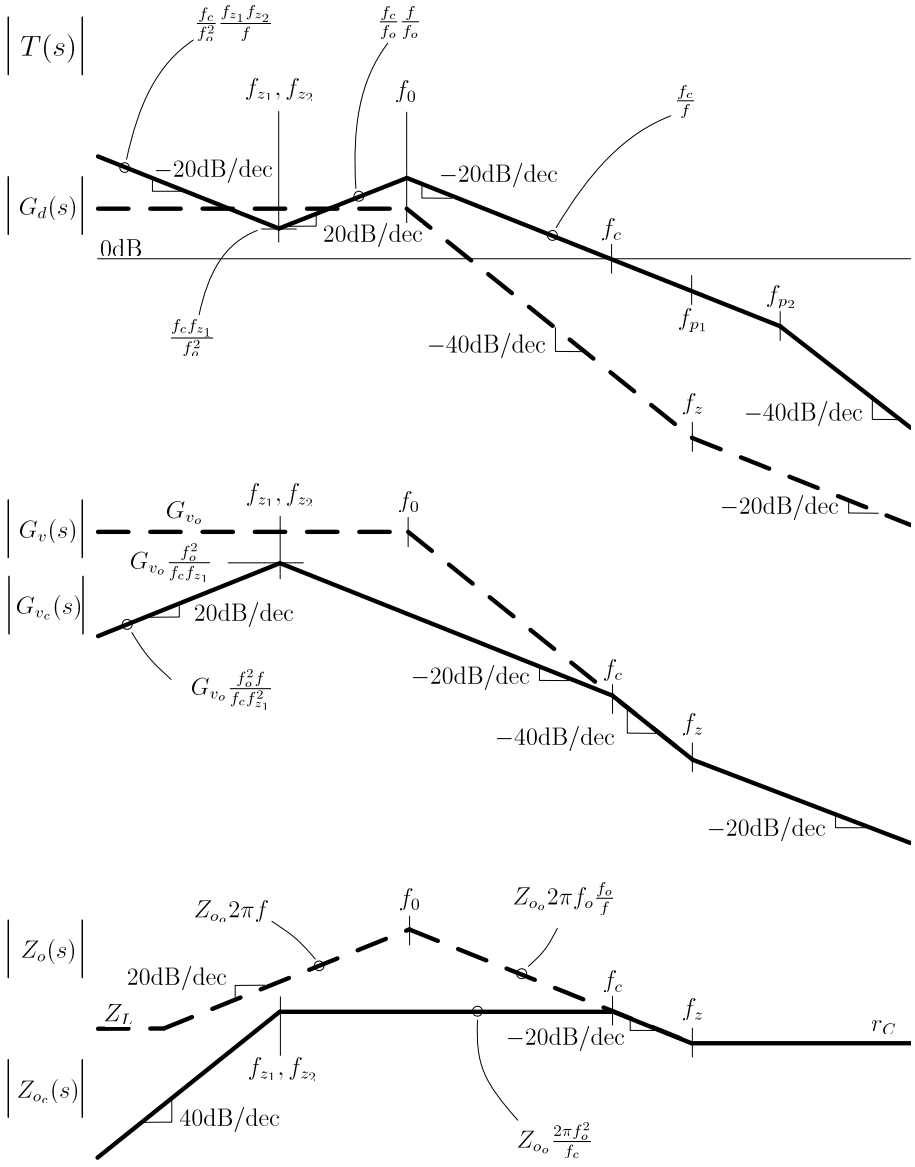


Figure 6.22: Bode Plot Asymptotes for Case 2

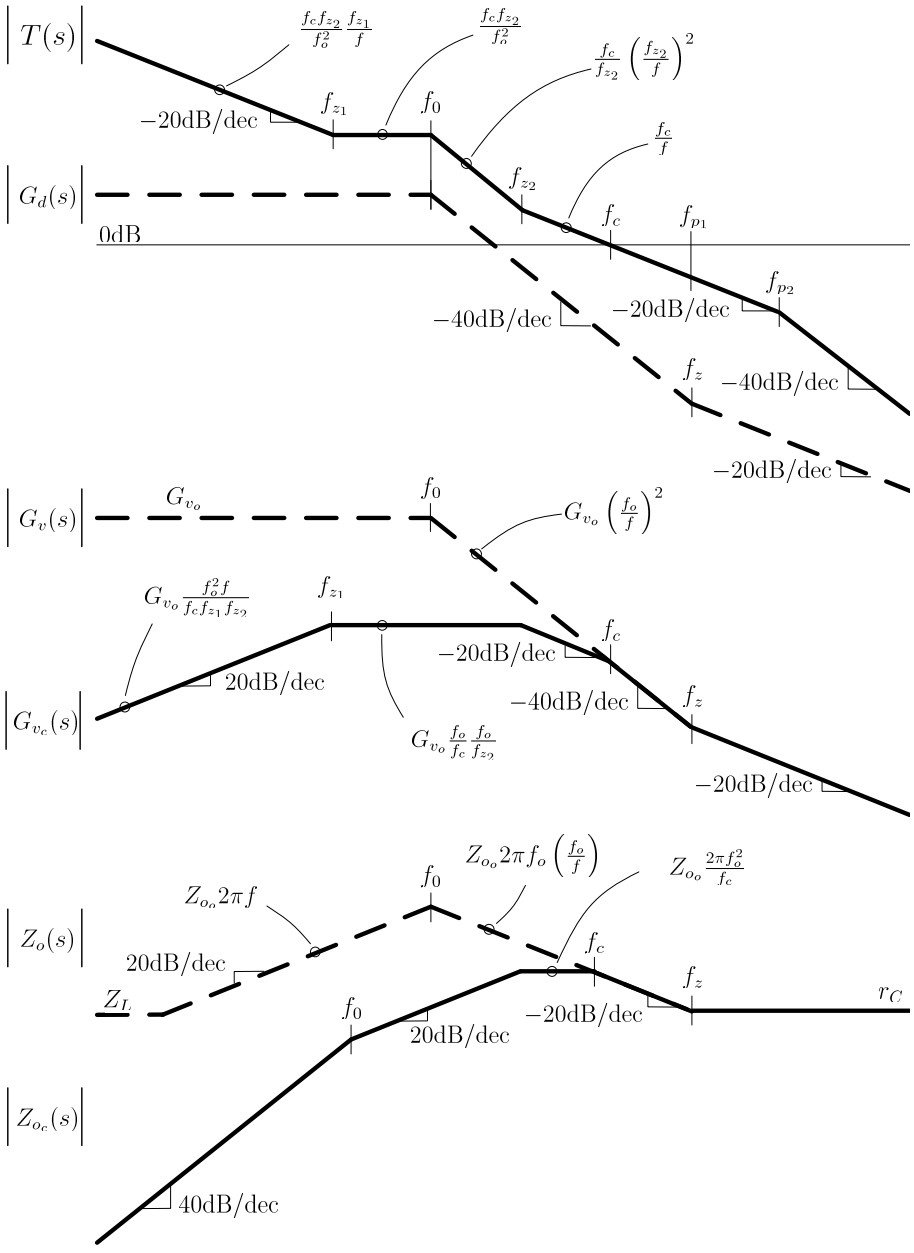


Figure 6.23: Bode Plot Asymptotes for Case 3

To determine a proper location for the introduced components, it is important to first start by improving the phase margin. This is accomplished by having at least one zero below the natural frequency of the system. By introducing one zero rather than both at this point, it will work to exactly cancel the phase shift introduced by the integrator without dropping the loop gain more than necessary. Introducing the second zero after the natural frequency will help extend the loop gain bandwidth, pushing the crossover frequency further toward higher frequency.

Through careful adjustment of parameter location and system response simulation, the system parameters were calculated as shown below. An optimum crossover frequency is found in terms of improving the phase margin, yet also maximizing loop gain bandwidth at $f_c = 6.31kHz$. This will be shown in the system response later in this section.

$$\omega_{z1} = (2\pi)5.06\frac{krad}{s}$$

$$\omega_{z2} = (2\pi)8.22\frac{krad}{s}$$

$$\omega_{p1} = \omega_(z) = (2\pi)6.37\frac{krad}{s}$$

$$\omega_{p2} = (2\pi)63.6\frac{krad}{s}$$

$$\omega_I = 17k\frac{rad}{s}$$

Figure 6.24 describe the loop gain of the system as a function of frequency. Note that with the previously discussed changes, high DC gain, switching frequency attenuation, and system stability are all accomplished.

Figure 6.27 is the circuit realization of the compensation scheme designed above. Figure 6.28 shows the simulation results of the circuit in response to the change in output current described in the introduction. Note that the maximum deviation from peak to peak using this voltage compensation scheme is 300 mV. The system shows a spike in voltage when the current is changed, and then quickly reduces to the expected voltage. This clearly shows the difference between this method of design and the constant impedance method, where a constant impedance will have half of the peak to peak voltage deviation; yet, there is a difference in the average output voltage level depending on the load applied. However, since power supply requirements are typically quantified in terms of an output voltage tolerance range, the voltage droop compensation and current droop compensation allow for tighter restrictions on levels, thus making them a better design compared to traditional voltage compensation.

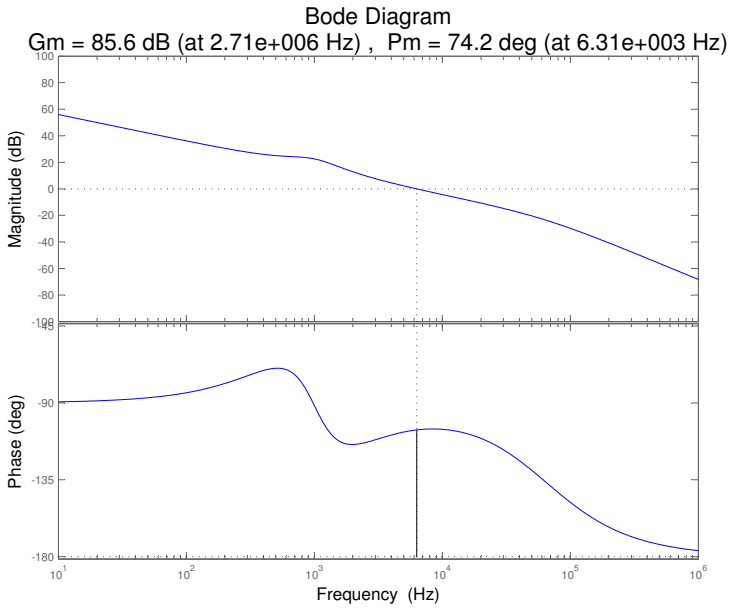


Figure 6.24: MATLAB Bode Plot of Loop Gains with Voltage Mode Compensation

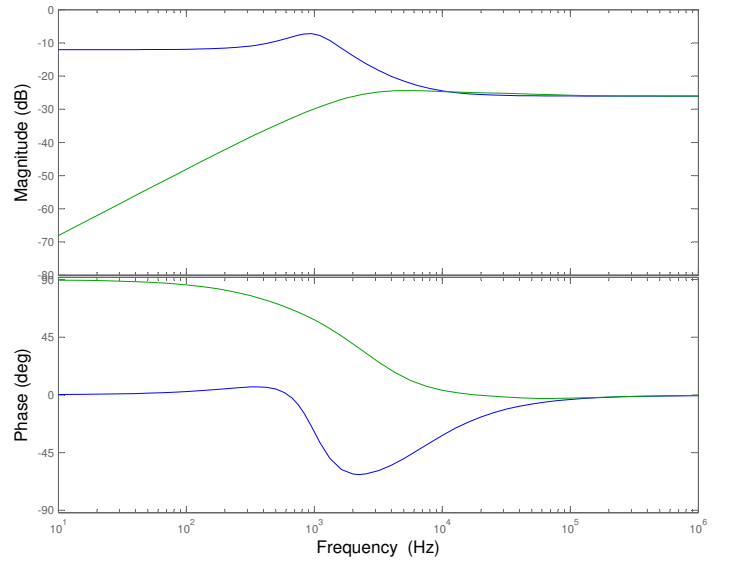


Figure 6.25: MATLAB Bode Plot of Z_o for Voltage Mode Compensated System

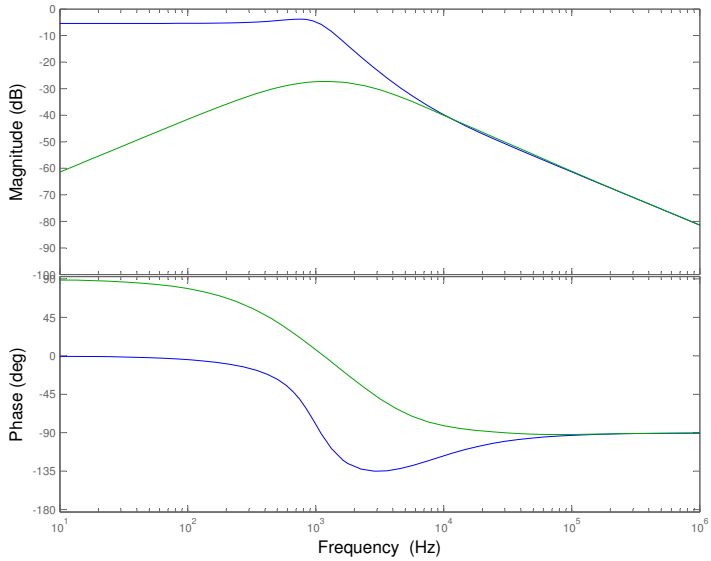


Figure 6.26: MATLAB Bode Plot of G_{vg} for Voltage Mode Compensated System

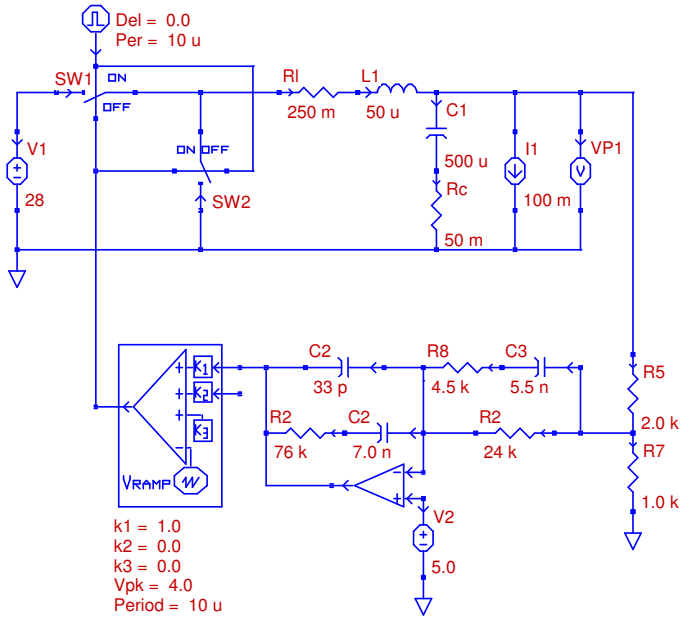


Figure 6.27: PECS Schematic of System with Voltage Mode Compensation

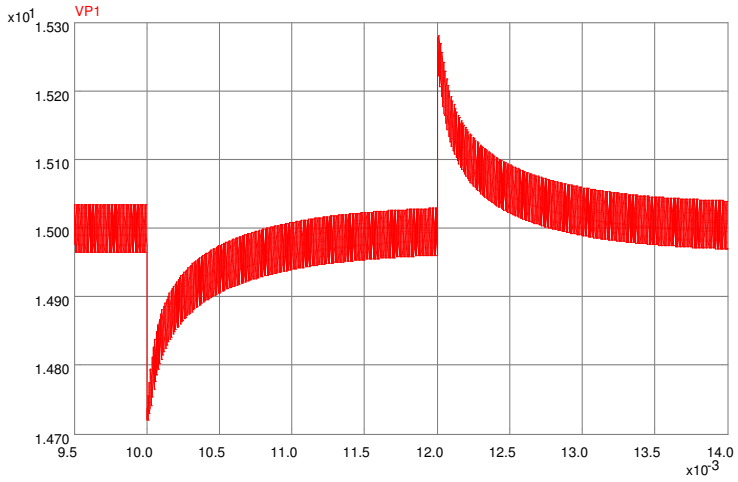


Figure 6.28: PECS Simulation of Voltage Mode Compensated Response to a Load Current Step

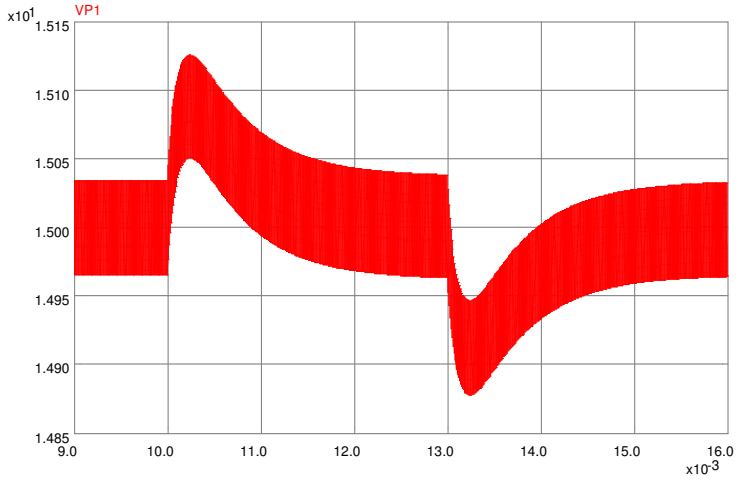


Figure 6.29: PECS Simulation of Voltage Mode Compensated Response to a Supply Voltage Disturbance

6.3 Summary

Through implementation of a voltage droop, inductor current droop, and a voltage compensation circuit, it was found that the voltage and current droop compensation techniques were able to have an output voltage deviation of half the size of the voltage compensation method. This reduction in output voltage deviation is an effect of creating a constant closed loop output impedance on the output of the converter. The only downside to the droop compensation methods is that the output voltage changes to the deviation value, rather than introducing a small transient and returning, as is the case with the voltage compensation.

Overall, due to the fact that regulated voltages are defined over an acceptable output range, the droop control methods both allow the smallest deviation that can fit in a given tolerance window. Ideally the current sensing droop control is the most complete method of compensation due to the two loop compensation. Practically, however, the voltage droop method accurately reduces the output voltage deviation and is the simplest to implement in terms of components.

6.4 MATLAB Code

```
clear
close all
format compact

s = tf('s');

Vg = 28;
R = 3;
L = 50e-6;
C = 500e-6;
rl = 0.25;
rc = 0.05;
Vm = 4;
Vo = 15;
D = Vo/Vg;


H = 1/3;
w0 = 1/sqrt(L*C);
f0 = w0/(2*pi);
wc = 1/(rc*C);
wr = 1/(R*C);
wl = rl/L;
Q = sqrt(L/C)/(rl+rc);
PWM = 1/Vm;
T0 = Vg*H*PWM;


```

```
29 f = logspace(1,6,1000);
30 w = 2*pi*f;
31
32 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
33 %%%   Plant Open-loop
34
35 Gvg = D*(1+s/wc)/(1+s/(Q*w0)+(s/w0)^2);
36 Gvd = Vg*(1+s/wc)/(1+s/(Q*w0)+(s/w0)^2);
37 Zo = rl*(1+s/wc)*(1+s/wl)/(1+s/(Q*w0)+s^2/w0^2);
38
39 %%%  Loop gain
40 T = tf(T0*[1/wc 1], [1/w0^2 1/(Q*w0) 1]);
41
42 figure(1)
43 [mag, phase] = bode(T,w);
44 margin(mag, phase, w)
45
46 h = gcr;
47 h.AxesGrid.Xunits = 'Hz';
48 h.AxesGrid.TitleStyle.FontSize = 16;
49 h.AxesGrid.XLabelStyle.FontSize = 12;
50 h.AxesGrid.YLabelStyle.FontSize = 12;
51
52 % Zoc = Zo/(1+T);
53 % Gvgc = Gvg/(1+T);
54 %
55 % figure(2)
56 % bode(Zo);
57 % hold
58 % bode(Zoc)
59 % title('');
60 % h = gcr;
61 % h.AxesGrid.Xunits = 'Hz';
62 % h.AxesGrid.TitleStyle.FontSize = 16;
63 % h.AxesGrid.XLabelStyle.FontSize = 12;
64 % h.AxesGrid.YLabelStyle.FontSize = 12;
65 %
66 %
67 % figure(3)
68 % bode(Gvg);
69 % hold
70 % bode(Gvgc)
71 % title('');
72 % h = gcr;
73 % h.AxesGrid.Xunits = 'Hz';
74 % h.AxesGrid.TitleStyle.FontSize = 16;
75 % h.AxesGrid.XLabelStyle.FontSize = 12;
76 % h.AxesGrid.YLabelStyle.FontSize = 12;
77
78
79
80
81 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
82 %%% Droop passive
83
84 Kv = (rl-rc)/(rc*Vg*(1/Vm)*H);
85 wzc = (rl-rc)/(L-rc*rc*C);
```

```
wpv = wc;

Gcdroop_p = tf(Kv*[1/wzc 1], [1/wpv 1]);

Tdroop_p = Gcdroop_p * T;

figure(4)
[mag, phase] = bode(Tdroop_p,w);
margin(mag, phase, w)
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;


Zoc = Zo/(1+Tdroop_p);
Gvgc = Gvg/(1+Tdroop_p);

figure(2)
bode(Zo);
hold
bode(Zoc)
title('');
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;


figure(3)
bode(Gvg);
hold
bode(Gvgc)
title('');
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%% Droop active

wi_da = 100000;
wz_da = w0;
wp_da = 2*pi*50000;

% wi_da = 7.3529e+004;
% wz_da = w0;
% wp_da = 2*pi*5.4683e+004;

Gcvdroop_a = tf(wi_da*[1/wz_da 1], conv([1 0], [1/wp_da 1]));

Tvdroop_a = Gcvdroop_a * T;
```

```
143
144 figure(5)
145 [mag, phase] = bode(Tvdroop_a,w);
146 margin(mag, phase, w)
147
148 hold
149
150 Ti = tf(Vg/R*[1/wr 1], [1/w0^2 1/(Q*w0) 1]);
151 Tidroop_a = PWM * H *Gcvdroop_a * Ti * rc;
152
153 [mag, phase] = bode(Tidroop_a,w);
154 margin(mag, phase, w)
155
156 T2 = Tvdroop_a/(1+Tidroop_a);
157 [mag, phase] = bode(T2,w);
158 margin(mag, phase, w)
159
160 h = gcr;
161 h.AxesGrid.Xunits = 'Hz';
162 h.AxesGrid.TitleStyle.FontSize = 16;
163 h.AxesGrid.XLabelStyle.FontSize = 12;
164 h.AxesGrid.YLabelStyle.FontSize = 12;
165
166 hold off
167
168
169
170
171 Gii=(1+s/wc)/(1+s/(Q*w0)+s^2/w0^2);
172 Gid=(Vg/R)*(1+s/wr)/(1+s/(Q*w0)+s^2/w0^2);
173 Gig=s*C/(1+s/(Q*w0)+s^2/w0^2);
174
175 % Av=wi*(1+s/w1)/(s*(1+s/w2));
176 % Ti= Av*Fm*Gid*H*Ri1;
177 % Tv=Av*Fm*H*Gvd;
178 % T2=Tv/(1+Ti);
179 %Gvgc=Gvg/(1+T2);
180
181 Ti = Tidroop_a;
182 Tv = Tvdroop_a;
183
184 Zoc = (Zo*(1+Ti)+Ti*(Gvd*Gii)/Gid)/(1+Ti+Tv);
185 Gvgc = (Gvg*(1+Ti)—Ti*(Gvd*Gig)/Gid)/(1+Ti+Tv);
186
187 figure(9)
188 bode(Zo);
189 hold
190 bode(Zoc)
191 title('');
192 h = gcr;
193 h.AxesGrid.Xunits = 'Hz';
194 h.AxesGrid.TitleStyle.FontSize = 16;
195 h.AxesGrid.XLabelStyle.FontSize = 12;
196 h.AxesGrid.YLabelStyle.FontSize = 12;
197
198
199 figure(10)
```

```
bode(Gvg);
hold
bode(Gvgc)
title('');
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%% Voltage mode

wi = 17000;
wz1 = 0.8*w0;
wz2 = 1.3*w0;
wp1 = wc;
wp2 = 10*wp1;

Gcvmode = tf(wi*conv([1/wz1 1], [1/wz2 1]), conv([1 0], ...
    conv([1/wp1 1], [1/wp2 1])));

Tvmode = Gcvmode * T;

figure(6)
[mag, phase] = bode(Tvmode,w);
margin(mag, phase, w)
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;

Zoc = Zo/(1+Tvmode);
Gvgc = Gvg/(1+Tvmode);

figure(7)
bode(Zo);
hold
bode(Zoc)
title('');
h = gcr;
h.AxesGrid.Xunits = 'Hz';
h.AxesGrid.TitleStyle.FontSize = 16;
h.AxesGrid.XLabelStyle.FontSize = 12;
h.AxesGrid.YLabelStyle.FontSize = 12;


figure(8)
bode(Gvg);
hold
bode(Gvgc)
title('');
h = gcr;
```

```
256 h.AxesGrid.Xunits = 'Hz';
257 h.AxesGrid.TitleStyle.FontSize = 16;
258 h.AxesGrid.XLabelStyle.FontSize = 12;
259 h.AxesGrid.YLabelStyle.FontSize = 12;
260
261
262
263 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
264 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
265 %%%  Components
266
267 %%% Droop passive
268 display(' Droop passive ')
269 R1 = 100000;
270 C1 = 1/(R1*wzc);
271 R2 = Kv*R1;
272 C2 = 1/(R2*wpv);
273
274 R1
275 R2
276 C1
277 C2
278 display(' ')
279
280 %%% Droop active
281
282 display('Droop active ')
283 C1 = 33e-12;
284 R2 = 1/(wp_da*C1);
285 C2 = 1/(R2*wz_da);
286 R1 = 1/(C2*wi_da);
287
288
289 R1
290 R2
291 C1
292 C2
293 display(' ')
294
295 %%% Voltage mode,   R1 >> R3, C1 >> C3
296
297 display('Voltage mode ')
298 C3 = 33e-12;
299 R2 = 1/(C3*wp2);
300 C1 = 1/(R2*wz1);
301 R1 = 1/(C1*wi);
302 C2 = 1/(R1*wz2);
303 R3 = 1/(C2*wp1);
304
305 C1
306 C2
307 C3
308 R1
309 R2
310 R3
311
312 %%% Droop passive
```

```
% R1 =
%       100000
% R2 =
%   1.7143e+005
% C1 =
%   2.4375e-009
% C2 =
%   1.4583e-010


% Droop active
% wi_da = 70000;
% wz_da = w0;
% wp_da = 70000;
%
% R1 =
%   3.9113e+004
% R2 =
%   4.3290e+005
% C1 =
%   3.3000e-011
% C2 =
%   3.6524e-010


% %%% Droop active
% wi_da = 150000;
% wz_da = w0;
% wp_da = 50000;
% R1 =
%   2.5554e+004
% R2 =
%   6.0606e+005
% C1 =
%   3.3000e-011
% C2 =
%   2.6089e-010


%%% Voltage mode
% wi = 7000;
% wz1 = 0.3*w0;
% wz2 = 1.4*w0;
% wp1 = wc;
% wp2 = 10*wp1;
%
% C1 =
%   6.9570e-009
% C2 =
%   5.5000e-009
% C3 =
%   3.3000e-011
% R1 =
%   2.3957e+004
% R2 =
%   7.5758e+004
% R3 =
```

```
370 %   4.5455e+003
371
372
373 % %%% Voltage mode
374 % wi = 17000;
375 % wz1 = 0.8*w0;
376 % wz2 = 1.3*w0;
377 % wp1 = wc;
378 % wp2 = 10*wp1;
379 %
380 % C1 =
381 %   2.6089e-009
382 % C2 =
383 %   5.3942e-009
384 % C3 =
385 %   3.3000e-011
386 % R1 =
387 %   2.2547e+004
388 % R2 =
389 %   7.5758e+004
390 % R3 =
391 %   4.6346e+003
392
393
394 %%%%  Droop active
395 R1 = 50e3;
396 R2 = 593e3;
397 C1 = 5e-12;
398 C2 = 267e-12;
399 wi = 1/(R1*(C1+C2));
400 fz = 1/(2*pi*R2*C2);
401 fp = 1/(2*pi*R2*C1*C2/(C1+C2));
402 display('Droop active - good')
403 wi
404 fz
405 fp
```

Bibliography

[1] M. Xu K. Yao and F. Lee. Design considerations for vrm transient response based on the output impedance. *IEEE*, 18(6):1270–1277, November 2003.

[2] M. Xu K. Yao, K. Lee and F. Lee. Optimal design of the active droop control method for the transient response. *IEEE*, pages 718–723, 2003.

[3] RD Middlebrook. Predicting modulator phase lag in pwm converter feedback loops. *Powercon*, 1981.

Part II

Modern Control

Chapter 7

Introduction

There are three main problems that can be examined in the study of systems in the controls context: system dynamics, system identification or modeling, and system control. They develop from the three aspects that are present in the block diagram of a basic system: input, system, and output [?]. Typically, two of the three aspects are known, and the third must be determined from the other two.

In system control, the system is known, and the input to the system that produces a desired output must be determined. Part II focuses on the fundamental control problem of regulation for disturbance rejection as it pertains to DC-DC converters, and uses the Ćuk DC-DC converter as the platform for applying the various design steps, leading up to a mimimal-order compensator design, demonstrated in Chapter 13. It is assumed that the reader of this part of the book is familiar with the classical control system design techniques presented earlier as the modern control design methods build on a classical foundation. Note that for the regulation problem, the desired output value is fixed, whereas in the servo problem, the desired output is to track a changing setpoint.

The Ćuk DC-DC converter was chosen as an example system for two main purposes. This nonlinear switching circuit can act to raise (boost) or lower (buck) the voltage from input to output, making it a generic DC-DC converter (compared to converters that can only boost or buck the input voltage, but not do both). Also, the circuit contains four energy storage devices leading to a fourth-order system, which creates sufficient complexity in an output feedback compensator to require compensator order reduction. This allows an original idea regarding order reduction to be presented. Boost or buck converters are typically implemented with only two energy storage components, and the resulting simplicity in compensators designed using modern control techniques either does not require model reduction or renders one of the techniques presented practically useless.

Analysis of the Ćuk converter circuit begins in Chapter 8. The control system design procedures use MATLAB from The Mathworks, Inc. (See Appendix ?? for code.) The nonlinear Ćuk switching circuit is modeled as a small-signal

continuous linear time invariant (LTI) system using state space averaging. The LTI model to be used during the design process is validated by transient comparison with a nonlinear circuit simulation to justify the assumption that the small-signal model would be adequate. The open-loop performance characteristics are tested, and a set of performance criteria for the closed-loop controlled system are specified.

Chapter 9 covers pole placement using state feedback. This chapter uses desired poles given by a filter prototype that is optimal with respect to an integral performance index and discusses how to select a weighting parameter that determines the closed-loop pole locations.

Integral augmentation of the state feedback architecture is described in Chapter 10. This allows the closed-loop system to completely eliminate steady state error, which could not be accomplished by state feedback alone.

Chapter 11 discusses state estimation using full- and reduced-order observers to allow for the use of output feedback, as state information is not always available to the designer.

Chapter 12 shows the application of optimal control and estimation using linear quadratic methods. These techniques allow the designer to determine optimal controller and optimal estimator gains. Loop transfer recovery is discussed as a means to recover desirable frequency-domain stability margins that are lost when designing an optimal output feedback compensator.

In order to design compensators that can be constructed from a minimum number of components, Chapter 13 covers order reduction methods. First, a reduced-order optimal compensator with recovered loop gain is designed. This step is followed by applying balanced realization and truncation techniques to eliminate states with little effect on performance, resulting in additional compensator order reduction.

Chapter 14 describes how to implement two of the final compensator designs that were created and shows the difference in analog controller circuit complexity that can arise from only one additional order in the compensator.

Finally, Chapter 15 presents the minimal compensator circuit test results from a power electronics simulator that prove the performance of the final controller design exceeded the original design specifications.

Chapter 8

System Analysis

Prior to designing a controller for a system, the control system designer must understand the system's characteristics. For example, is the system open-loop stable? Are there dominant poles? Are there poles that may be neglected during design? Is the system controllable using the selected inputs? Can an estimator be constructed based on the measured outputs? These types of questions should be answered both intuitively and mathematically prior to embarking on an attempt to design a controller for the system.

As stated in Chapter 7, the Ćuk DC-DC converter is used here as the example system for demonstrating the compensator design processes described in Part II. The starting point is the construction of a mathematical model of the system in MATLAB. The model is a mathematical description of some or all of the behavior of the real-world system that is adequate for performing controller design. State space averaging yields a linear small-signal model for the nonlinear switching system (derivations may be found in the Appendix) [**?**]. Additionally, a nonlinear circuit model was created in the Power Electronics Circuit Simulator (PECS) software package in order to validate the performance of the assumed linear model. PECS uses a schematic-based circuit editor and features its own plotting tool, PECSPLOT.

A note on notation: the zeros, poles, and gains of systems discussed in Part II are in the Evans form, i.e., the coefficient of the highest power of s in each factored term is unity and the stated gain is not the DC gain of the system. This is in contrast to Bode form, where the constant in each factored term is unity and the DC gain is explicitly stated. Evans form was chosen for convenience, as it is the form used by *zpk* systems in MATLAB.

8.1 The Ćuk Converter

The Ćuk converter is a step-down/step-up converter based on a switching boost-buck topology. Essentially, the converter is composed of two sections, an input stage and an output stage. The schematic of the Ćuk converter is presented

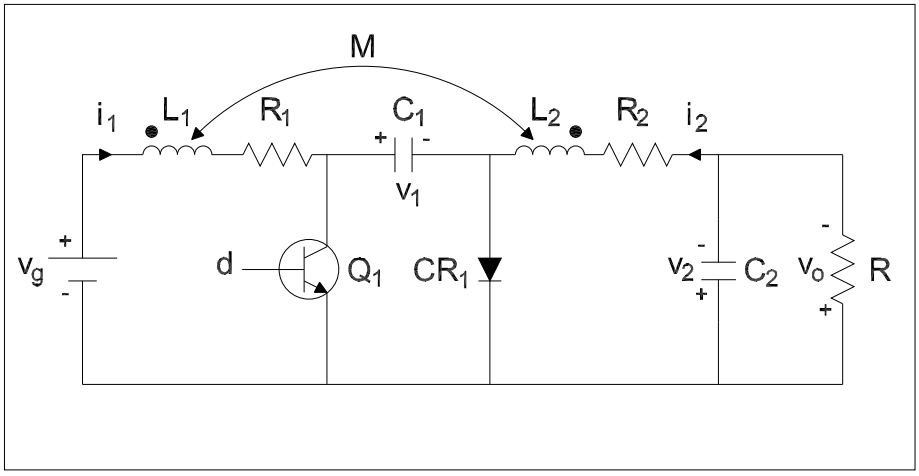


Figure 8.1: Ćuk converter with inductor equivalent series resistances.

in Figure 8.1, with component values given in the Appendix. (The lowercase variables indicate small-signal deviations from nominal operating point variables as obtained by linearization.) The input voltage v_g is fed into the circuit via inductor L_1. When transistor Q_1 is on, current i_1 builds the magnetic field of the inductor in the input stage. The diode CR_1 is reverse biased, and energy dissipates from the storage elements in the output stage. When Q_1 turns off, inductor L_1 tries to maintain the current flowing through it by reversing polarity and sourcing current as its magnetic field collapses. It thus provides energy to the output stage of the circuit via capacitor C_1. Both currents i_1 and i_2 must sum to zero in the steady state, since the assumption is that voltage v_1 is essentially constant (given that the voltage across a capacitor cannot change instantaneously and the switching speed of the circuit is high). This provides for the following charge conservation relation:

$$i_1 t_{on} + i_2 t_{off} = 0 \tag{8.1}$$

The inductor currents are the input and output currents, therefore, if the principle of conservation of energy is applied:

$$\frac{v_o}{v_g} = \frac{D_s}{1 - D_s} \tag{8.2}$$

where D_s is the duty cycle of the switch, $D_s \triangleq \frac{t_{on}}{t_{on}+t_{off}}$. Equation 8.2 shows that by controlling the duty cycle of the switch (by small-signal deviation d), the output voltage v_o can be controlled and can be higher or lower than the input voltage v_g. By using a controller to vary the duty cycle during operation, the circuit can also be made to reject disturbances, as will be shown.

8.2 Open Loop Performance of the Ćuk Converter

Before a controller was designed, the performance of the open-loop Ćuk model was examined. A state space block diagram for the open-loop model is shown in Figure 8.2. The state space equations were determined to be:

$$\begin{aligned} \dot{x} &= Ax + Bv_g + B_d d \\ v_o &= Cx \\ x &= \begin{bmatrix} v_2 & v_1 & i_2 & i_1 \end{bmatrix}' \end{aligned} \tag{8.3}$$

The state space matrices for the open-loop model from the disturbance input

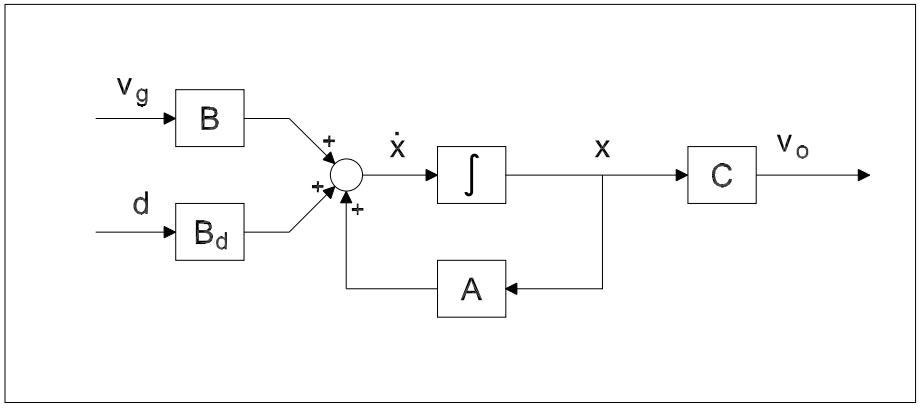


Figure 8.2: State space model of the Ćuk converter.

v_g to the output v_o are the state space averaged matrices $\{A, B, C, D\}$. The state space matrices for the open-loop system from the control input d to the output v_o are the state space averaged matrices $\{A, B_d, C, D\}$. Thus, the model of the Ćuk converter has two inputs (a control input d and a disturbance input v_g) and one output (v_o). (See Appendix for model derivations.)

The MATLAB model open-loop response to a unit step disturbance in v_g is shown in Figure 8.3. By inspection of the plotted response, it was determined that the system reached lightly damped oscillations around a steady state DC value in approximately 20 ms. The steady state value was 26 V, a value predicted from the gain equation for the Ćuk converter:

$$v_o = \frac{D_s}{1 - D_s} v_g \tag{8.4}$$

With nominal duty cycle $D_s = 0.667$, a 1 V step input in v_g produces a 2 V step in the output voltage v_o. This shows that the open-loop system does not

reject disturbances on the input voltage v_g. Also, note that the output of the circuit is a lightly damped sinusoid, with an approximate frequency of 1.83 kHz (11.5 krad/s).

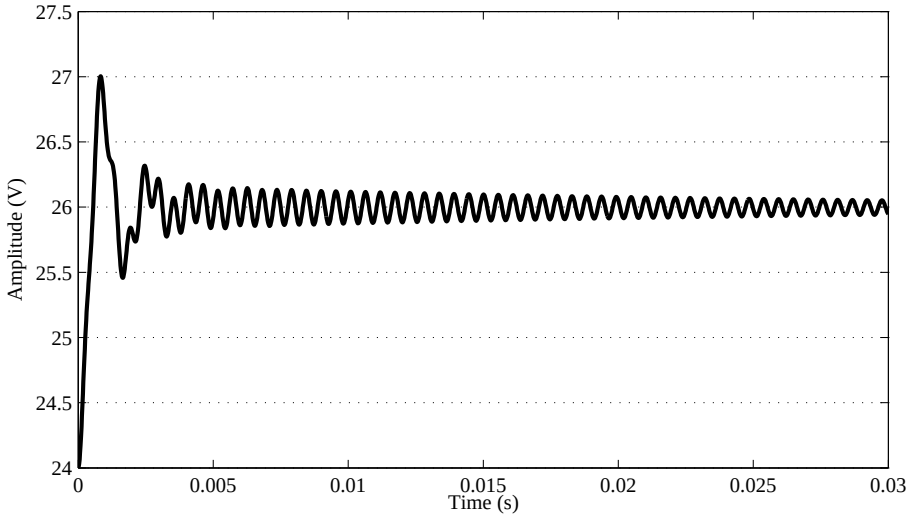


Figure 8.3: Ćuk converter output voltage response to a unit step disturbance in v_g.

The PECS circuit is shown in Figure 8.4. The simulator was set up to check the performance of the nonlinear converter in response to a unit step up in v_g. The PECS plot of these transients is shown in Figure 8.5. Comparison of the MATLAB and PECS plots reveals that the linear model used in MATLAB is an acceptable model of the plant to use for control system design.

The pole-zero plot of $T_{v_o d}$ is shown in Figure 8.6. All poles and zeros are in the LHP, therefore the Ćuk converter is a stable minimum-phase system. The locations for the zeros and poles are:

$$\begin{aligned} z &= \left[\; -1490 \pm j9000 \; \right] \\ p &= \left[\; -879 \pm j3641, \quad -40 \pm j11500 \; \right] \end{aligned}$$

The 1.83 kHz ringing in the output transient caused by the unit step disturbance is due to the frequency associated with the dominant pole pair at $-40 \pm j11500$.

8.3 Controllability and Stabilizability

The idea of controllability refers to the ability of the input control u to affect the system dynamics. Controllability is defined as the ability to move the state of a system from an initial value x_0 to any arbitrary state x_f within a finite

time period t using the input signal u. (Note that controllability says nothing about the magnitude of the input signal u, i.e., the control effort, nor the time t required to accomplish this transition.) Essentially, it is a test to determine if the closed-loop system poles may be arbitrarily placed in the complex plane.

The controllability matrix M_c is constructed from (A, B) in the following manner:

$$M_c = \begin{bmatrix} B & AB & A^2B & \dots & A^{n-1}B \end{bmatrix} \tag{8.5}$$

where n is the order of the system. If M_c is a full rank matrix, the system is fully controllable. The rank deficiency of M_c tells the designer how many modes are uncontrollable. There is no rank deficiency in M_c for the Ćuk converter model, therefore the system is fully controllable.

8.4 Observability and Detectability

Observability refers to the ability to determine any initial state x_0 using only a finite record of the output y between an initial time and a final time. The observability matrix M_o is constructed from (A, C) in the following manner:

$$M_o = \begin{bmatrix} C \\ CA \\ CA^2 \\ \vdots \\ CA^{n-1} \end{bmatrix} \tag{8.6}$$

where n is the order of the system. If M_o is a full rank matrix, the system is fully observable. The rank deficiency of M_o tells the designer how many modes are unobservable. The Ćuk converter model is fully observable.

8.5 Controlling the Ćuk Converter

The model used in controller design is a small-signal model, since, like many other methods of linearization, the state-space averaging method only holds for small deviations from the nominal operating point. Most of the equations and figures that follow refer to deviations from the nominal operating point of the system unless otherwise stated or identifiable from context.

The control system designer must always begin with a set of design specifications when starting a project. The specifications are a set of goals for the behavior of the controlled system, and may need to change during the design process if not achievable or as new information becomes available. Specifications generally consider both transient behavior (e.g., rise time, settling time, percent overshoot) and stability margins (e.g., relative stability, gain margin, phase margin).

8.5.1 Time Domain Specifications

Time domain constraints are given by the system performance specifications. The transient response of a regulated system is typically limited in terms of both maximum amplitude deviation from the nominal output and settling time in response to a transient. The goal for the Ćuk converter controller design example is to control the output voltage to within 1% of nominal (i.e., 23.76 to 24.24 V) in response to unit step voltage disturbances in the input. This matches the 1% regulation of standard industrial power supplies sold by a major control system equipment manufacturer. Also, the controller should be able to maintain the nominal output voltage within tolerances as the input varies over a range of 9 to 14 V, though this shall be considered a steady-state, not transient, operating requirement. As a final specification, steady-state error in the output voltage shall be eliminated within 20 milliseconds of the start of a transient.

8.5.2 Frequency Domain Specifications

The frequency response of the transfer function $T_{v_o d}$ should be high at low frequencies for proper regulation and low at high frequencies for adequate noise rejection. The example system base switching frequency is 100 kHz (6.28×10^5 rad/s). As the small signal model breaks down above half of the switching frequency, the loop gain at any frequency above 50 kHz (3.14×10^5 rad/s) should be less than 0 dB. Indeed, there should be a design margin left between this frequency and the gain crossover frequency. A gain margin of at least 20 dB and a phase margin of at least 50° will be sought to ensure stability.

8.5.3 Control Effort Constraints

The Ćuk converter nominal duty cycle is related to the steady-state gain of the converter G by Equation 8.4. Neglecting circuit losses, Equation 8.4 may be rearranged to calculate the duty cycle as a function of the output operating point and input voltages, v_o and v_g:

$$D_s = \frac{v_o}{v_o + v_g} \tag{8.7}$$

Therefore, the nominal duty cycle at the operating point of 24 V for an input of 12 V is determined to be 0.667. However, the purpose of controller design is to ensure the output voltage remains within 1% of 24 V despite disturbances in the input voltage. Since a deviation model is used, the difference between the nominal operating duty cycle and the duty cycle required to keep the output at exactly 24 V may be approximated, and this is shown in Figure 8.7. It is this change in duty cycle that the controller must provide, as the deviation in duty cycle is the small-signal control input of the Ćuk converter. Thus, it can be predicted from Equation 8.7 or Figure 8.7 that the the controller must change the duty cycle by -0.018 to maintain the output at 24 V for a step disturbance input on v_g from the nominal 12 V to 13 V. This value of -0.018 will be used

to verify the correct steady-state control effort in controller design. (Note that Equation 8.7 does not account for any voltage losses within the circuit, so the duty cycle will actually be slightly higher from the calculated value when any resistances are included in the circuit.) The duty cycle is limited to $0 \leq D_s \leq 1$, therefore if the control effort plus the nominal value of 0.667 exceeds these limiting values, the compensator design is not acceptable. This leads to hard limits on the small-signal control effort of $[-0.667, 0.333]$, though the inclusion of a design margin to these limits may be desirable. It is up to the individual designer to choose constraints on the control effort, however it is generally best to allow the use of as much of the control effort range as possible.

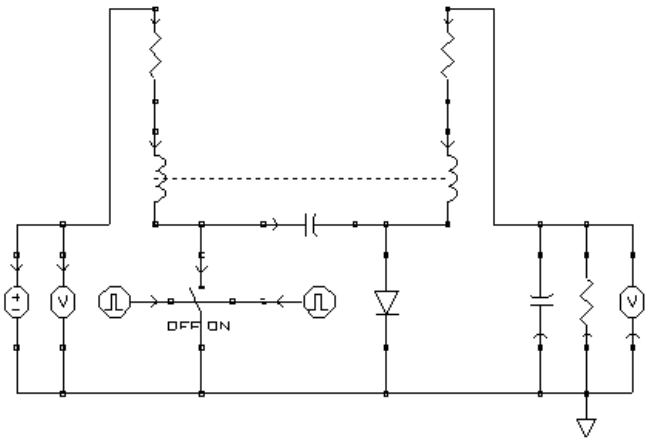


Figure 8.4: The Ćuk converter simulated in PECS.

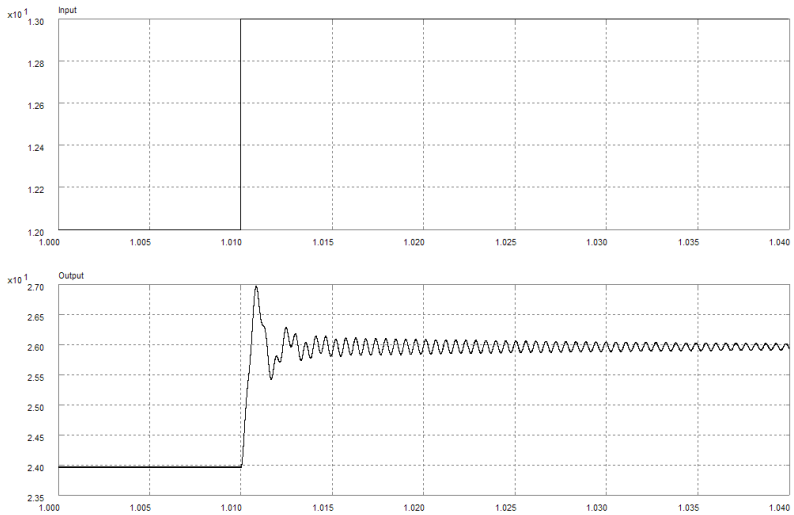


Figure 8.5: Unit step response of the Ćuk converter in PECS.

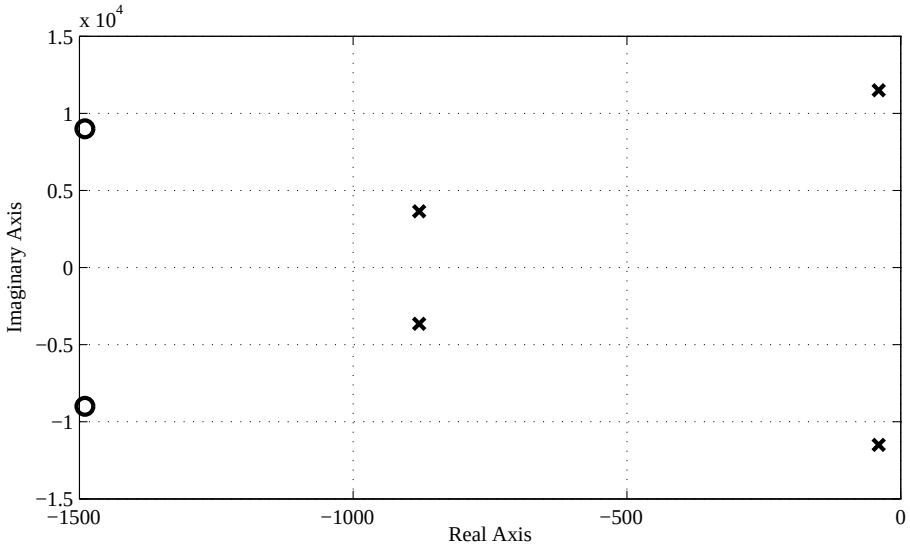


Figure 8.6: Map of the pole and zero locations of $T_{v_o v_g}$.

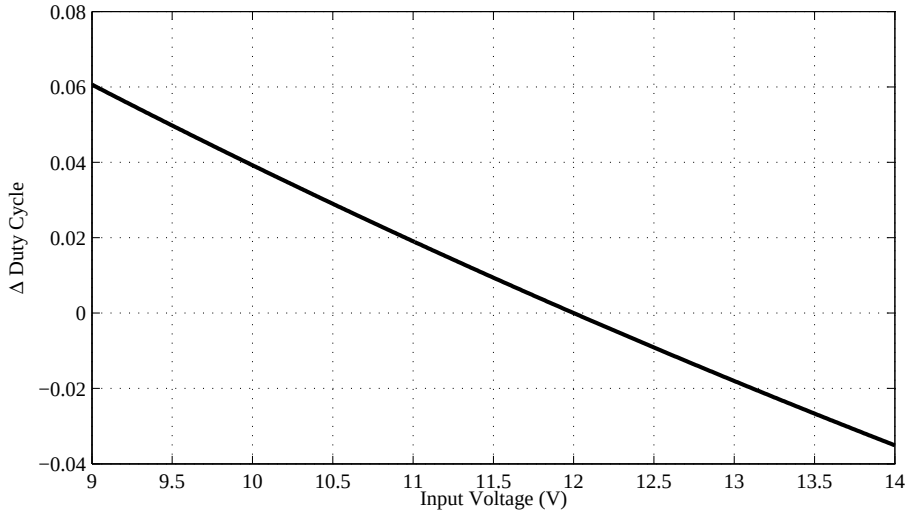


Figure 8.7: The small-signal duty cycle required over the full input voltage range to maintain nominal output voltage.

Chapter 9

Pole Placement

For a system that is completely controllable and where all the states are accessible, feedback of all of the states through a gain matrix can be used to place the poles at any desired location in the complex plane. The control law used for state feedback is:

$$u = -Kx \tag{9.1}$$

which uses the matrix K to place the poles of the system at desired locations [**?**]. This type of compensator is said to employ full state feedback (FSFB). A FSFB regulator is shown in Figure 9.1.

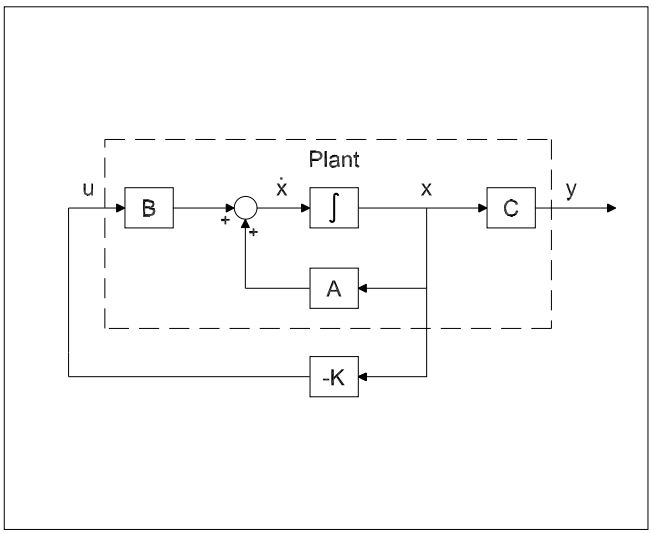


Figure 9.1: State feedback regulation.

9.1 Pole Placement via Ackermann's Formula

Ackermann's formula may be used with single-input, single-output (SISO) systems like the Ćuk converter. Ackermann's formula is:

$$K = \begin{bmatrix} 0 & 0 & \dots & 1 \end{bmatrix} M_c^{-1}(A^n + \alpha_1 A^{n-1} + \dots + \alpha_{n-1}A + \alpha_n I) \qquad (9.2)$$

This method of determining K may be used with the system in any representation. It is this method of pole placement that is used in the designs of the state feedback controllers that follow.

9.2 Ćuk Converter with State Feedback Compensator

One problem with pole placement is how to go about selecting desirable pole locations. Two main methods of design are commonly followed [**?**]:

- Select pole locations such that a dominant complex pole pair exists. This technique is generally used when designing tracking systems, for which the transient time domain requirements (e.g., rise time, overshoot, settling time, etc.) are able to be recast into desired dominant pole locations.
- Select pole locations that have been determined to give a prototype time-domain response, e.g., filter pole locations.

The latter method is used in this chapter for pole placement with full state feedback control.

Graham and Lathrop [**?**] discuss assigning the system poles of higher-order systems to prototype locations that minimizes a performance index (or cost function) known as the integral of the time-weighted absolute error (ITAE) to an input signal:

$$J_{ITAE} = \int_0^\infty t\,|e(t)|\,dt \qquad (9.3)$$

By placing poles in an ITAE filter pattern to minimize J_{ITAE}, the designer achieves a response that is optimized with respect to deviation from setpoint (provided by the absolute error) and settling time (errors that occur later in the time history contribute more to the J_{ITAE} cost). Since the goal of the control system designer is to regulate the Ćuk converter output voltage with respect to input voltage disturbances, J_{ITAE} provides a scalar figure of merit by which to judge controller performance. For regulator problems, the desired output is rejection of disturbance deviations from the nominal operating point. The error between the desired output and the plant output is defined as $e(t) = r(t) - y(t)$. Since $r(t) = 0$ for all time t in a regulator problem, the error $e(t)$ is simply $-y(t)$.

Table 9.1: Frequency-Normalized Characteristic Equations for ITAE Response

Order	Characteristic Equation
1	$s+\omega$
2	$s^2+1.414\omega s+\omega^2$
3	$s^3+1.75\omega s^2+2.15\omega^2 s+\omega^3$
4	$s^4+2.1\omega s^3+3.4\omega^2 s^2+2.7\omega^3 s+\omega^4$
5	$s^5+2.8\omega s^4+5\omega^2 s^3+5.5\omega^3 s^2+3.4\omega^4 s+\omega^5$

The frequency-normalized characteristic equations for minimum ITAE response are given in Table 9.1 up through order five (so that a full-order state feedback controller with an integrator may be applied to the Ćuk converter).

A control system designer can use a computer program (e.g., MATLAB from The Mathworks with the Control Systems Toolbox) to iteratively design and test state feedback controllers over a range of values for the scalar multiplier frequency ω. It is easiest to work with the characteristic equations given in Table 9.1 in MATLAB in a factored format as shown in Table 9.2. The control system designer must determine the value of ω that places the poles in such a way as to achieve the desired time domain response. By using the steady state error

Table 9.2: Frequency-Normalized Pole Locations for ITAE Response

Order	Factored Pole Locations
1	$\omega[-1]$
2	$\omega^2[-0.7071 \pm j0.7071]$
3	$\omega^3[-0.7081, -0.521 \pm j1.068]$
4	$\omega^4[-0.424 \pm j1.263, -0.626 \pm j0.4141]$
5	$\omega^5[-0.8955, -0.3764 \pm j1.292, -0.5758 \pm j0.5339]$

as a measurement metric for each iteration during the design, ω can be chosen that produces a steady state error within the performance specification of 1%. Figure 9.2 shows a plot of steady-state error vs. ω, and this figure was used to select a value of ω that corresponded to 0.24 V (1% voltage regulation). Initially, a wide range of frequencies was selected with a large increment, then the range and the increment were made smaller in order to narrow in on the first frequency with less than 0.24 V of steady state error, which occurs at $\omega = 10.0125$ rad/s. The unit step disturbance response of the system with a full state feedback controller designed in this manner is shown in Figure 9.3. Note that there is 0.24 V of steady-state error to the 1 V step disturbance in input voltage, indicating that the disturbance is rejected to within the performance specifications. The amplitude and settling time of the transient meet design specifications, so this controller has very desirable time-domain response characteristics. The loop gain of the regulated system is shown in Figure 9.4, where the loop is broken at the large X shown on the control input d in Figure 9.5. MATLAB calculations

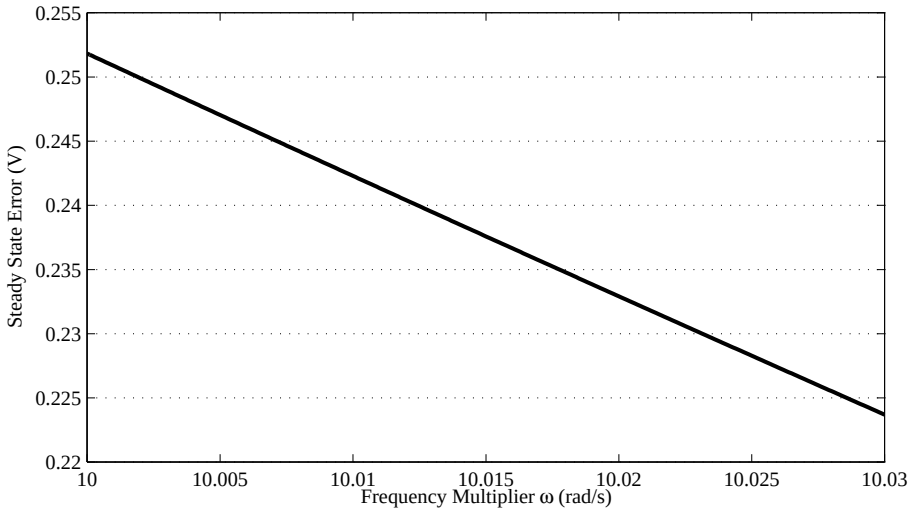


Figure 9.2: Steady state error of unit step disturbance as frequency multiplier is swept.

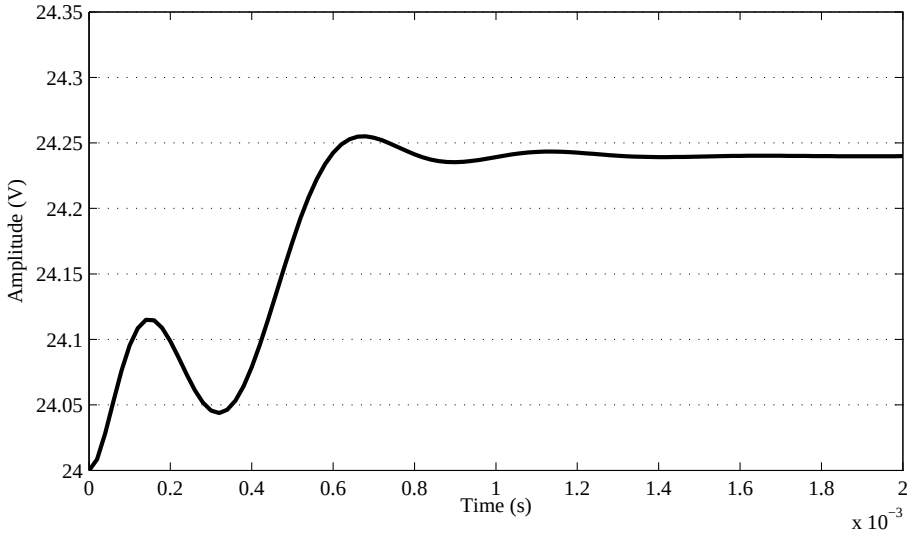


Figure 9.3: Response to unit step disturbance of input voltage.

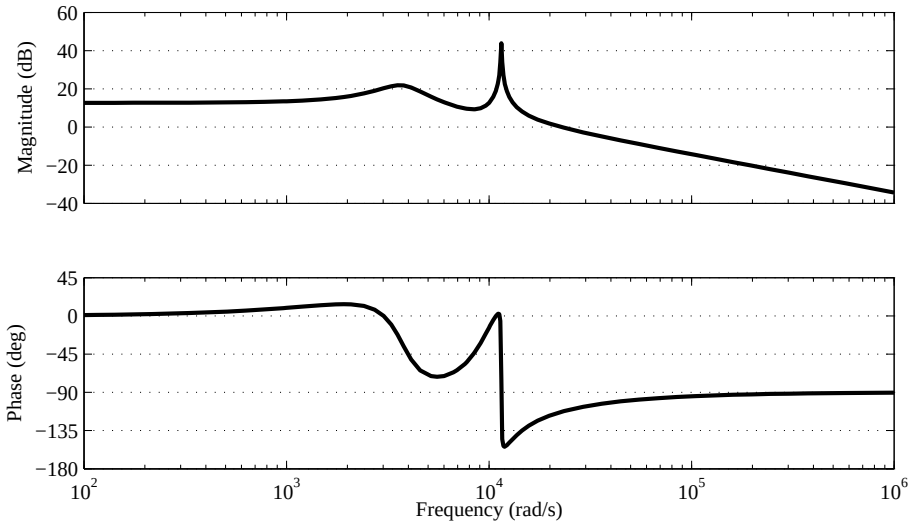


Figure 9.4: Loop gain with the full state feedback controller.

give the gain margin as ∞ and a phase margin of 67°, which are very desirable frequency-domain response characteristics.

Finally, the control effort of the design should be examined. Once again, the control input to the Ćuk converter is the change in duty cycle d used to turn on and off $Q1$. The control effort is plotted in Figure 9.6, and it can be seen that the effort is not approaching the limits assigned to d. It can also be seen that the steady-state deviation control effort is approximately -0.0163, which corresponds roughly to calculations using Equation 8.7.

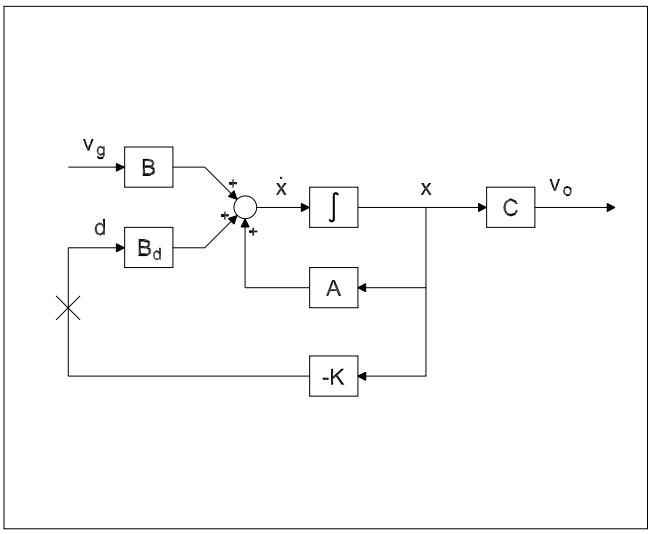


Figure 9.5: The full state feedback controller applied to the Ćuk converter.

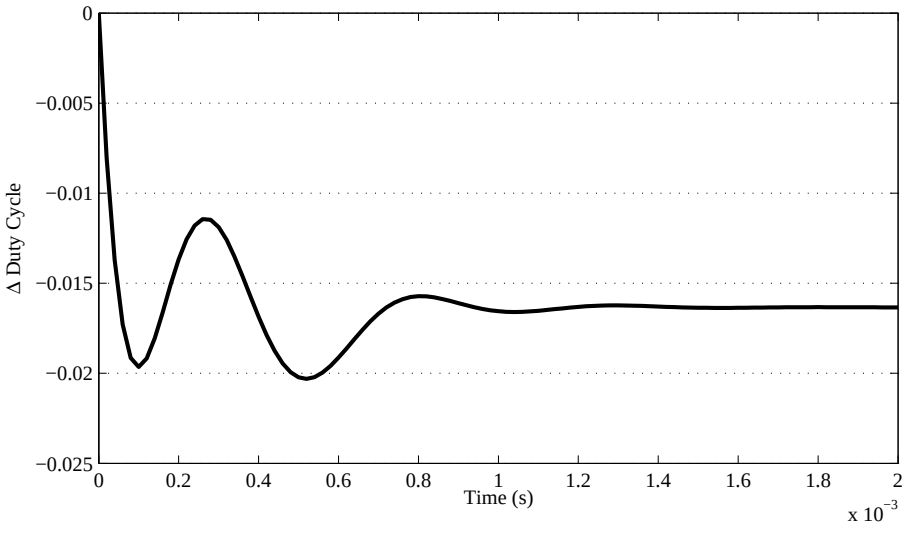


Figure 9.6: Control effort with the full state feedback controller.

Chapter 10

Integral Action

The previous state feedback design for the Ćuk converter resulted in 0.24 V of steady-state error to the 1 V disturbance in input voltage, which is just within design specifications. Additional gain could reduce this error, though it could never be eliminated, as the Ćuk converter is a type 0 system, which means that there will always be some finite steady-state error to a unit step disturbance or setpoint change, even in a controlled system, no matter how high the gain. However, it is desirable to eliminate steady-state error entirely if possible. The only way to do this is to have the controller raise the type number. Full state feedback does not introduce an integrator into the closed loop, therefore does not change the type number.

10.1 Adding Integrators

In order to eliminate any steady-state offset that may occur, an integrating controller may be added to the controlled system. Integral control is a method of output feedback, as shown in Figure 10.1. The integrating controller integrates the error between any reference signal and the output $e(t) = r(t) - y(t)$ and adds it to the state feedback control effort to eliminate steady-state error. The equation for the integrator is $x_i = \int e dt$, or $\dot{x_i} = e$. Since each row in the state space representation is a first-order linear differential equation, and the integrator adds one new differential equation to the system $\dot{x_i} = -y = -Cx$, one new state x_i must be added to the state vector to raise the Ćuk system from type 0 to type 1. The augmented state vector is $[x\ x_i]'$ and the new state

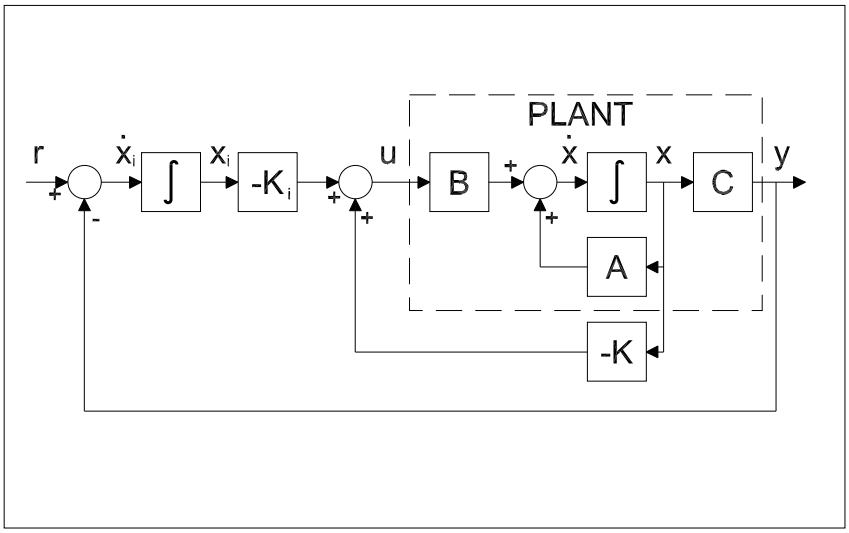


Figure 10.1: Generic system controlled with a FSFB regulator and output integral feedback.

space quadruple is:

$$\begin{aligned} A &= \begin{bmatrix} A & 0 \\ -C & 0 \end{bmatrix} \\ B &= \begin{bmatrix} B & 0 \end{bmatrix}' \\ C &= \begin{bmatrix} C & 0 \end{bmatrix} \\ D &= 0 \end{aligned} \tag{10.1}$$

The control law for this augmented system is $u = -kx - k_i x_i$. From the above modifications, the desired poles (with an added desired closed-loop pole location to account for the pole associated with the integrator) can be used to determine the state feedback gain, which has the structure $K = [k \;\; k_i]$.

10.2 Ćuk Converter with State Feedback and Integral Compensator

The augmented controlled system of the Ćuk converter is shown in Figure 10.2. This control method is described as full state feedback with an integrator (FSFBI).

The state quadruple for the system augmented with the new state and con-

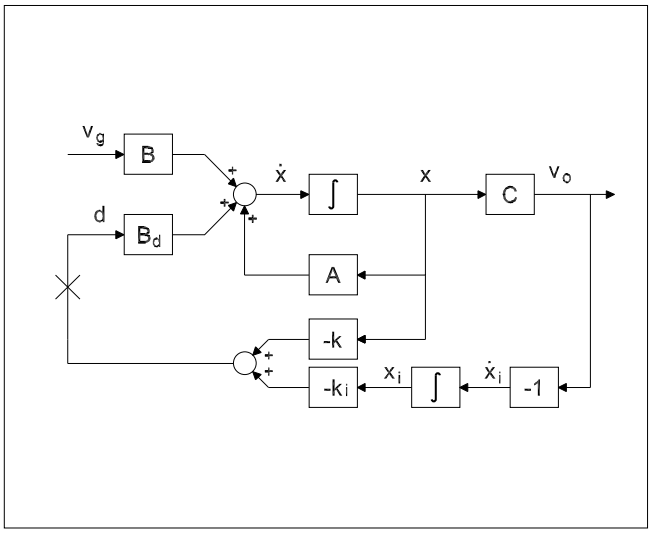


Figure 10.2: System controlled with a FSFBI regulator.

trolled with the new control law may be derived from the block diagram.

$$\begin{aligned} \dot{x} &= (A - B_d k)x - B_d k_i x_i + B v_g \\ v_o &= Cx \end{aligned} \tag{10.2}$$

along with the augmented closed-loop state space matrices

$$\begin{aligned} \bar{A} &= \begin{bmatrix} A - B_d k & -B_d k_i \\ -C & 0 \end{bmatrix} \\ \bar{B} &= \begin{bmatrix} B & 0 \end{bmatrix}' \\ \bar{C} &= \begin{bmatrix} C & 0 \end{bmatrix} \\ \bar{D} &= [D] \end{aligned} \tag{10.3}$$

The controlled system then becomes:

$$\begin{aligned} \dot{x} &= \bar{A}x + \bar{B}v_g \\ v_o &= \bar{C}x \end{aligned} \tag{10.4}$$

A frequency-sweep technique similar to that used for the FSFB controller was used to determine the pole placement for the system augmented with an integrator, and the results are shown in Figure 10.3. However, because the steady state error of a step disturbance response is always zero with a type 1 system, steady state error cannot be used as the performance metric for determining the frequency weighting used with the ITAE filter pole locations given in Table 9.1. Instead, the ITAE value of each unit step transient is calculated, and the frequency multiplier is found for the transient that has the minimum ITAE value.

The frequency multiplier was swept and the minimum ITAE determined to occur at $\omega = 6.564$ rad/s. The step disturbance transient is shown in Figure 10.4. The

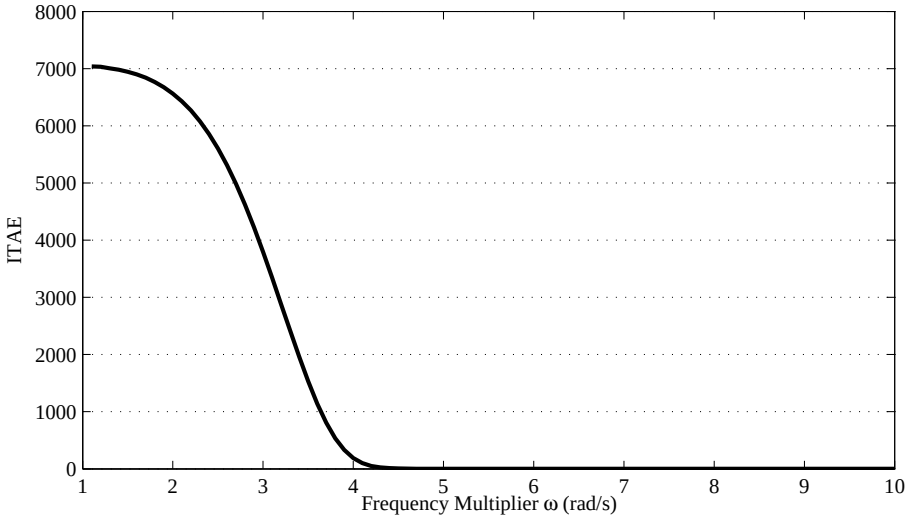


Figure 10.3: ITAE pole frequency multiplier determination.

loop gain of the controlled system may be seen in Figure 10.5, where the loop is broken at the large X shown on the control input d in Figure 10.2. MATLAB calculations give the gain margin as ∞ and a phase margin of 68°. Figure 10.6 shows the change in duty cycle effected by the FSFBI controller to control the Ćuk converter. Note that the final value of the control effort is -0.018. This is the approximate change in duty cycle that is necessary to completely reject the unit step disturbance in v_g as shown in Figure 8.7.

From this point forward in this paper, all of the example compensator designs will include an integrator term to completely reject the effects of the step disturbance in v_g, and though sometimes not explicitly stated in the compensator name, terms related to the integrator will appear in the state equations as well as the block diagrams relating to control of the Ćuk converter.

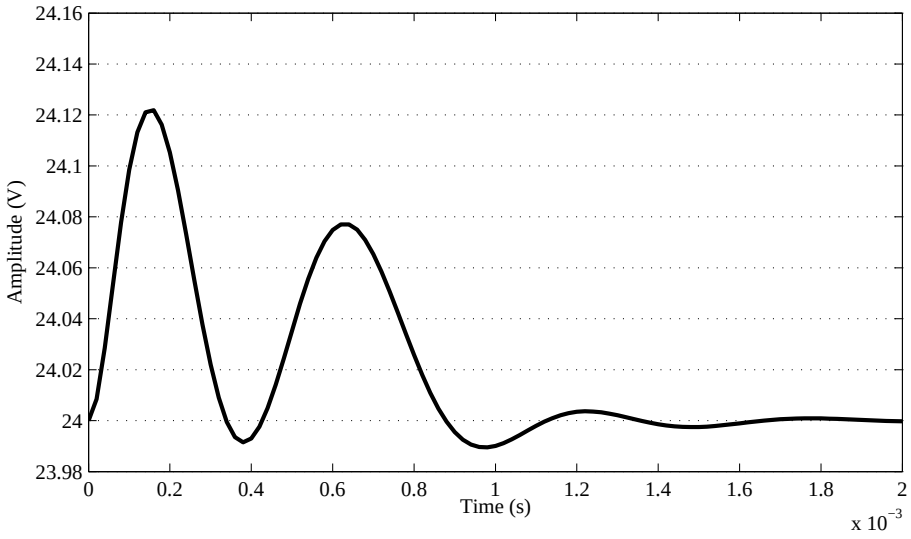


Figure 10.4: Unit step disturbance response of system with FSFBI controller.

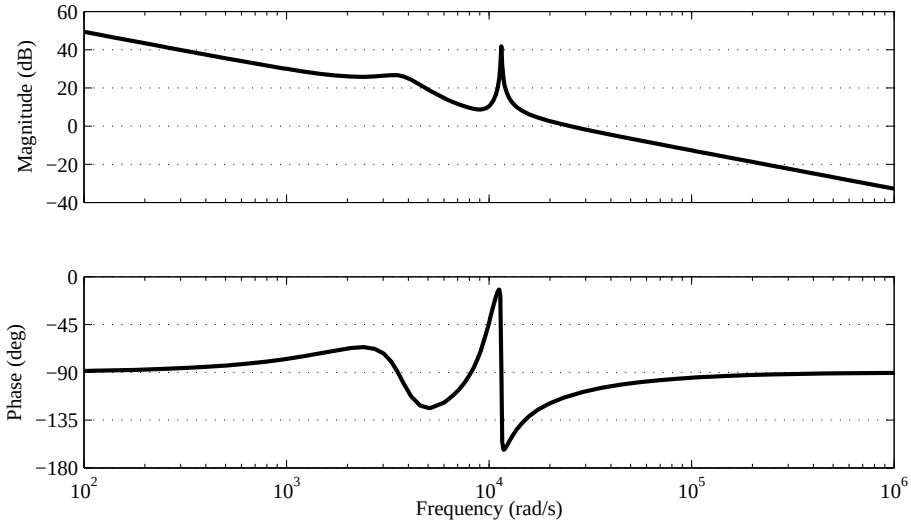


Figure 10.5: Loop gain of Ćuk converter controlled by FSFBI.

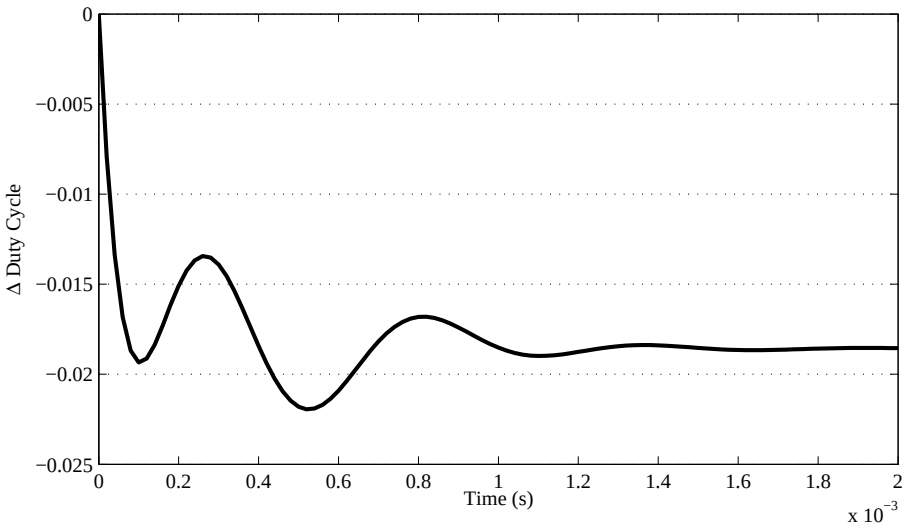


Figure 10.6: Control effort of FSFBI compensator.

Chapter 11

State Estimation

Since an n-th order system requires n states be fed back to the gain matrix K to allow pole placement anywhere in the complex plane, this requires at least n measurements of the state variables. This can be prohibitively expensive or complex. In some cases, the internal system states may not even be measurable. In general, only the input and output of a system are available to the control system designer. However, if the system is fully observable, a state estimator (also known as an observer) may be used to provide estimated state values for use in feedback control. The use of an observer requires that the state estimates converge to the actual state values (if starting from different initial states) more rapidly than the system itself responds. The control law used is then:

$$u = -K\hat{x} \tag{11.1}$$

where $\hat{x}$ indicates that the states fed back into the system are estimates.

In order to quickly force the state estimate to converge to the actual values of the state from arbitrary initial conditions, a correction term must be applied to the estimator dynamics such that the error dynamics approach zero rapidly.

11.1 Full-Order State Estimators

A state estimator may be constructed from the same system state space model used for control law gain determination as long as the system is fully observable. The output of the estimator $C\hat{x}$ can be compared to the output of the system, and any difference between them may be multiplied by a gain vector and fed back to the state estimator dynamics. Therefore:

$$\begin{aligned} e &= y - C\hat{x} \\ &= C(x - \hat{x}) \end{aligned} \tag{11.2}$$

Multiplying this error by a gain vector L, the desired state error correction term is formed, which can then be added to the dynamics of the estimator to form:

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + Bu - LC(x - \hat{x}) \\ &= (A - LC)\hat{x} + Bu + LCx \end{aligned} \tag{11.3}$$

When L is chosen such that the eigenvalues of $A - LC$ lie in the left half of the complex plane, the estimator error $e \to 0$ as $t \to \infty$. Since the state estimate must converge to the controlled state faster than the state itself can change, the eigenvalues of $A - LC$ should be placed farther to the left than the eigenvalues of $A - BK$. A good rule of thumb is to make the estimator dynamics at least twice as fast as the controlled system dynamics.

To form an output feedback compensator based on an estimator, the separation principle of controller design holds, which states that the controller gain K and the observer gain L can be found independently. The proof of this is in many other references (e.g., [**?**]), so it shall not be repeated here, but application shall be made of the principle in the design examples to follow.

When paired with the linear state feedback control law, the estimator-based compensator is formed. For the case of state feedback without an integral state added, the compensator is given by:

$$\begin{aligned} \dot{\hat{x}} &= (A - BK - LC)\hat{x} + Ly \\ u &= -K\hat{x} \end{aligned} \tag{11.4}$$

Where the state of the system has been augmented by an integrator state, the compensator is given by:

$$\begin{aligned} \begin{bmatrix} \dot{\hat{x}} \\ \dot{x}_i \end{bmatrix} &= \begin{bmatrix} A - Bk - LC & -Bk_i \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{x} \\ x_i \end{bmatrix} + \begin{bmatrix} L \\ -1 \end{bmatrix} y \\ u &= \begin{bmatrix} -k & -k_i \end{bmatrix} \begin{bmatrix} \hat{x} \\ x_i \end{bmatrix} \end{aligned} \tag{11.5}$$

11.2 Full-Order Estimator-Based Compensator

The block diagram for the Ćuk converter controlled with a full-order state estimator with linear control law and integral action is shown in Figure 11.1, and was used to derive the following closed-loop state equations:

$$\begin{aligned} \dot{x} &= Ax - B_d k\hat{x} - B_d k_i x_i + Bv_g \\ \dot{x}_i &= -Cx \\ \dot{\hat{x}} &= LCx - B_d k_i x_i + (A - B_d k - LC)\,\hat{x} \\ v_o &= Cx \end{aligned} \tag{11.6}$$

and the associated state space matrices:

$$\begin{aligned}
\bar{A} &= \begin{bmatrix} A & -B_d k_i & -B_d k \\ -C & 0 & 0 \\ LC & -B_d k_i & A - B_d k - LC \end{bmatrix} \\
\bar{B} &= \begin{bmatrix} B & 0 & 0 \end{bmatrix}' \\
\bar{C} &= \begin{bmatrix} C & 0 & 0 \end{bmatrix} \\
\bar{D} &= [D]
\end{aligned} \tag{11.7}$$

The step disturbance transient is shown in Figure 11.2. There is more oscillatory

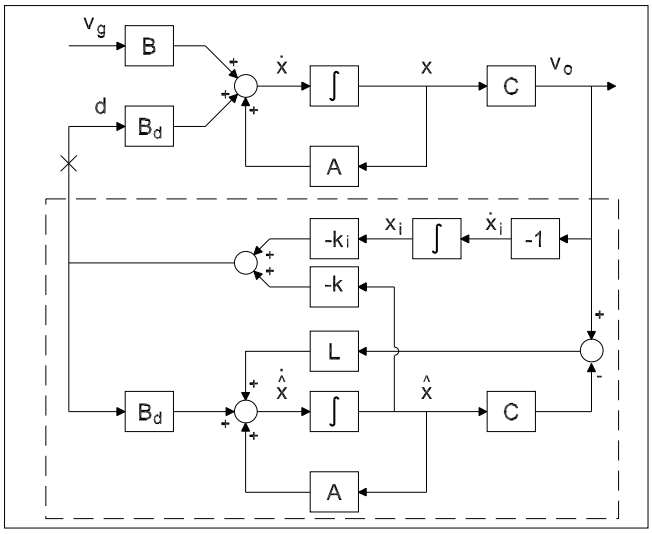


Figure 11.1: An estimated state feedback compensator with integral action.

behavior in the initial part of the transient response compared to the response under FSFBI control. This is likely caused by the initial estimation of states and their convergence to the actual state values. Comparison of the settling times shows that they are approximately the same, and the only transient differences occur early in the transient. The loop gain of the controlled system may be seen in Figure 11.3, where the loop is broken at the large X shown on the control input d in Figure 11.1. MATLAB calculations give the gain margin as 33.6 dB and a phase margin of 105°. Figure 11.4 shows the control effort of the ESFBI controller. Since the Ćuk converter has four states, the observer itself will be a fourth-order system. Along with the integral state, the compensator becomes a fifth-order system. When evaluating desired observer pole locations, keep in mind that the poles of the observer must be placed to the left of the poles of the plant by a large margin to ensure that the state estimator dynamics are faster than those of the plant.

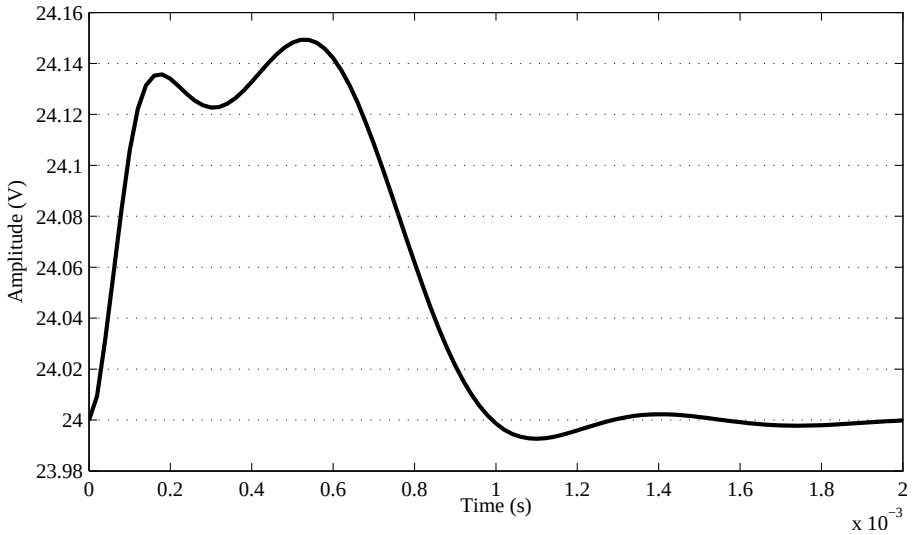


Figure 11.2: Unit step disturbance response of Ćuk converter with ESFBI compensator.

11.3 Reduced-Order State Estimators

If some of the states appear directly in the output as a function of the measurement equation (i.e., are not a linear combination of other states), those states do not need to be estimated. Hence, a reduced-order estimator may be constructed that only estimates the unmeasured states.

If C is a full rank matrix, a nonsingular linear transformation matrix can be formed by choosing a matrix T of dimension $(n-r)$ x n and forming:

$$P = \begin{bmatrix} C \\ T \end{bmatrix} \tag{11.8}$$

The matrix T may be any arbitrary matrix that produces a nonsingular P matrix, as P must be invertible.

Applying the standard linear transformation $x = Px$ with Equation (11.8) puts the system into an equivalent representation where C is of the form:

$$\begin{bmatrix} I_r & 0 \end{bmatrix} \tag{11.9}$$

(I is a square identity matrix with dimension r x r, $r < n$). It can be assumed that this representation exists without loss of generality since it is the result of a linear transformation.

The system and feedback gain matrix can now be partitioned into measured

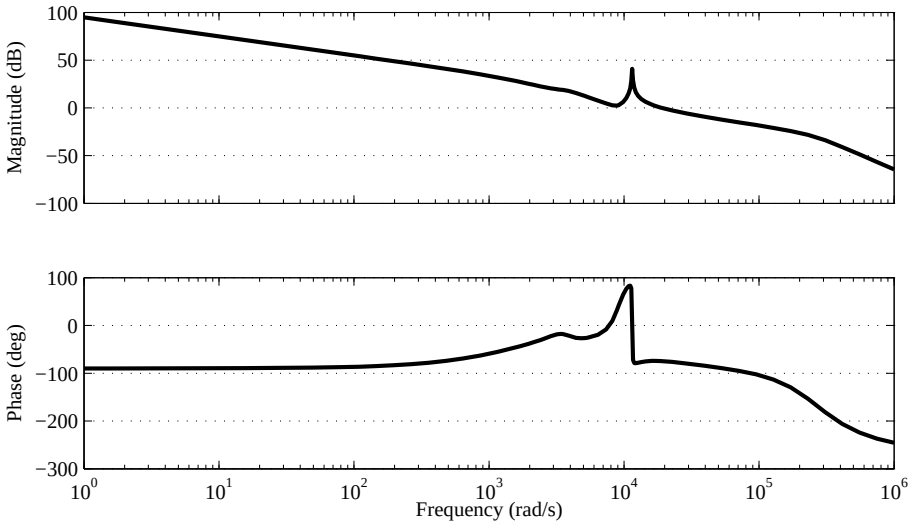


Figure 11.3: Loop gain of Ćuk converter controlled by ESFBI compensator.

and unmeasured portions:

$$\begin{aligned} \begin{bmatrix} \dot{x}_m \\ \dot{x}_u \end{bmatrix} &= \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} x_m \\ x_u \end{bmatrix} + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u \\ y &= x_m \\ K &= [k_m \; k_u] \end{aligned} \tag{11.10}$$

Since x_m corresponds to the states that appear in the output of the measurement equation, x_u represents the remaining unmeasured states. As x_m is present in the output, these states do not require estimation. This means that a reduced-order state estimator can be constructed that allows the estimation of x_u in such a manner that all states (either measured or estimated) are available for feedback via a linear control law:

$$u = -k_m x_m - k_u \hat{x}_u \tag{11.11}$$

In order to ensure that the reduced-order observer dynamics converge to the true state values of x, the error dynamics must converge to zero. A full-order observer uses a correction term to perform this, which is a gain matrix that multiplies the error between plant output and observer output. Unfortunately, since only the x_m states appear in the plant output, using the plant output contributes no information about the unmeasured states to the estimator and therefore has no dynamic effect on the estimate $\hat{x}_u$. However, a variable change can be performed:

$$\hat{x}_u = Ly + z \tag{11.12}$$

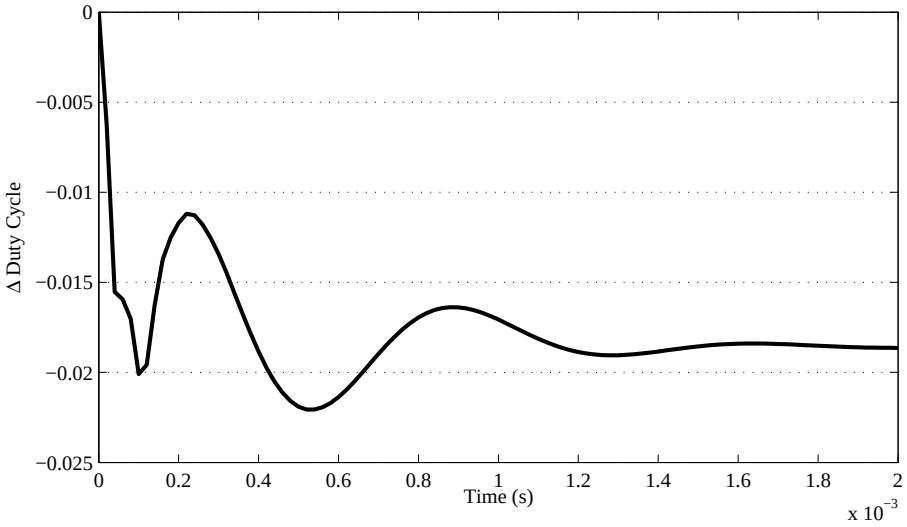


Figure 11.4: Control effort of ESFBI compensator.

where z is the output of a system of order $r < n$:

$$\dot{z} = Ez + Fy + Gu \tag{11.13}$$

with E, F, and G and the observer gain L yet to be determined.

Since observer design is concerned with elimination of the error between the actual state and its estimate, the estimation error can be defined as $e_u = x_u - \hat{x}_u$ and the error dynamics will converge to zero if $\hat{x}_u \to x_u$.

Using the partitioned format of x_u from Equation 11.10 along with $\hat{x}_u$ determined from the block diagram in Figure 11.5, it can be shown that:

$$\begin{aligned} \dot{\hat{x}}_u &= L(A_{11}x_m + A_{12}x_u + B_1u) + E(\hat{x}_u - Lx_m) + Fx_m + Gu \\ \dot{x}_u &= A_{21}x_m + A_{22}x_u + B_2u \end{aligned} \tag{11.14}$$

Adding zero to the right side of $\dot{\hat{x}}_u$ in the form of $Ex_u - Ex_u$:

$$\begin{aligned} \dot{\hat{x}}_u &= (LA_{11} - EL + F)x_m + (LA_{12} + E)x_u \ldots \\ &\quad +(LB_1 + G)u + E(x_u - \hat{x}_u) \end{aligned} \tag{11.15}$$

This gives the following equation for the estimator error dynamics when substituted into the time derivative of the unmeasured error $\dot{e}_u = \dot{x}_u - \dot{\hat{x}}_u$:

$$\begin{aligned} \dot{e}_u &= (A_{21} - LA_{11} + EL - F)x_m + (A_{22} - LA_{12} - E)x_u \ldots \\ &\quad +(B_2 - LB_1 - G)u + Ee_u \end{aligned} \tag{11.16}$$

In order for the estimator error dynamics to be independent of the state x, plant output y, and the input u, the first three terms on the right side of

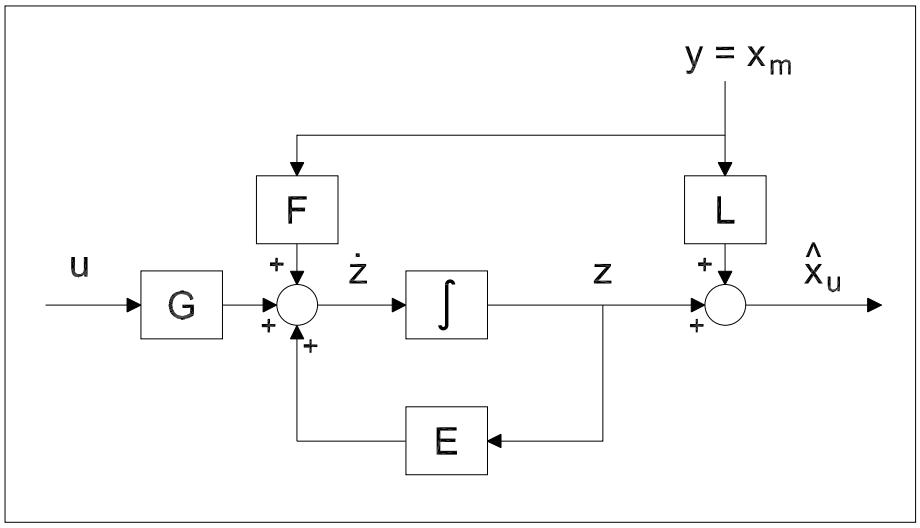


Figure 11.5: Reduced-order estimator construction.

Equation 11.16 must be zero. This is accomplished by selecting:

$$\begin{aligned} E &= A_{22} - LA_{12} \\ F &= A_{21} - LA_{11} + EL \\ G &= B_2 - LB_1 \end{aligned} \tag{11.17}$$

This leaves $\dot{e}_u = Ee_u$, which converges to zero when E is an asymptotically stable matrix. Thus, the error dynamics die out, leaving an estimate that equals the state. This means that L must be selected such that $A_{22} - LA_{12} \to 0$ as $t \to \infty$, i.e., the poles of E must lie in the left half of the complex plant. As with the full-order observer, the reduced-order observer poles should be placed such that the estimator dynamics are much more rapid than the controlled plant dynamics.

When paired with the properly-partitioned linear state feedback control law, the reduced-order estimator-based compensator is formed. For the case of state feedback without an integral state added, the reduced-order compensator is given by:

$$\begin{aligned} \dot{z} &= (E - Gk_u)z + (F - Gk_uL - Gk_m)y \\ u &= -k_uz + (-k_uL - k_m)y \end{aligned} \tag{11.18}$$

Where the state of the system has been augmented by an integrator state, the

reduced-order compensator is given by:

$$\begin{aligned}\begin{bmatrix} \dot{z} \\ \dot{x}_i \end{bmatrix} &= \begin{bmatrix} E - Gk_u & -Gki \\ 0 & 0 \end{bmatrix} \begin{bmatrix} z \\ x_i \end{bmatrix} + \begin{bmatrix} F - Gk_uL - Gk_m \\ -1 \end{bmatrix} y \\ u &= \begin{bmatrix} -k_u & -k_i \end{bmatrix} \begin{bmatrix} z \\ x_i \end{bmatrix} + (-k_uL - k_m)y \end{aligned} \quad (11.19)$$

11.4 Reduced-Order Estimator-Based Compensator

For the Ćuk converter model, matrix C is of the form $C = \begin{bmatrix} I & 0 \end{bmatrix}$ therefore v_2 is a measured state, and the unmeasured states are v_1, i_2, and i_1. This means that a reduced order observer may be designed that estimates only the three unmeasured states. The block model for a system controlled by a compensator made of a reduced-order estimator and a linear state feedback law is shown in Figure 11.6, and was used to derive the following state equations:

$$\begin{aligned}\dot{x} &= (A - B_dk_uLC - B_dk_mC)\,x - B_dk_ix_i - B_dk_uz + Bv_g \\ \dot{x}_i &= -Cx \\ \dot{z} &= (FC - Gk_mC - Gk_uLC)\,x - Gk_ix_i + (D - Gk_u)\,z \\ v_o &= Cx \end{aligned} \quad (11.20)$$

from which were determined the matrices:

$$\begin{aligned}\bar{A} &= \begin{bmatrix} A - B_dk_mC - B_dk_uLC & -B_dk_i & -B_dk_u \\ -C & 0 & 0 \\ FC - Gk_mC - Gk_uLC & -Gk_i & E - Gk_u \end{bmatrix} \\ \bar{B} &= \begin{bmatrix} B & 0 & 0 \end{bmatrix}' \\ \bar{C} &= \begin{bmatrix} C & 0 & 0 \end{bmatrix} \\ \bar{D} &= [D] \end{aligned} \quad (11.21)$$

where

$$\begin{aligned} E &= A_{22} - LA_{12} \\ F &= EL + A_{21} - LA_{11} \\ G &= B_{d_2} - LB_{d_1} \end{aligned} \quad (11.22)$$

To determine estimator pole placement, the same type of iterative algorithm used for the full order observer was implemented. The reduced order observer poles were placed to have faster dynamics than the poles of the controlled system.

The step disturbance transient is shown in Figure 11.7. The loop gain of the controlled system may be seen in Figure 11.8, where the loop is broken at

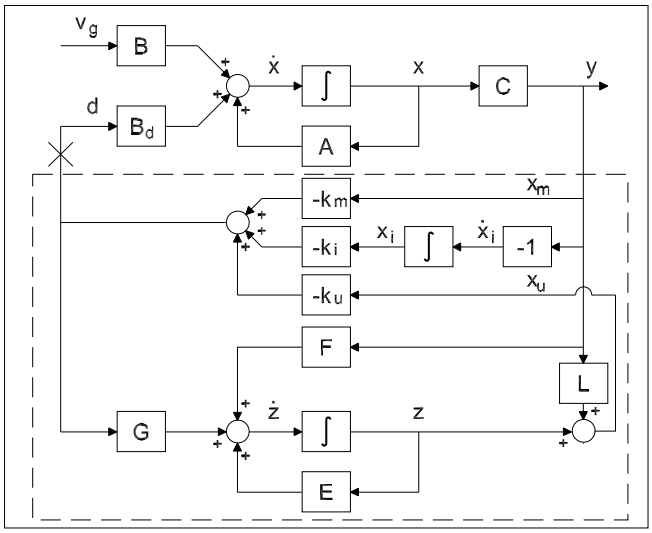


Figure 11.6: A state feedback regulator with integral action based on a reduced-order estimator.

the large X shown on the control input d in Figure 11.6. MATLAB calculations give the gain margin as ∞ dB and a phase margin of 36.5°. The latter clearly does not meet the design specification for phase margin, and uncertainty in the system model may make the controlled system unstable.

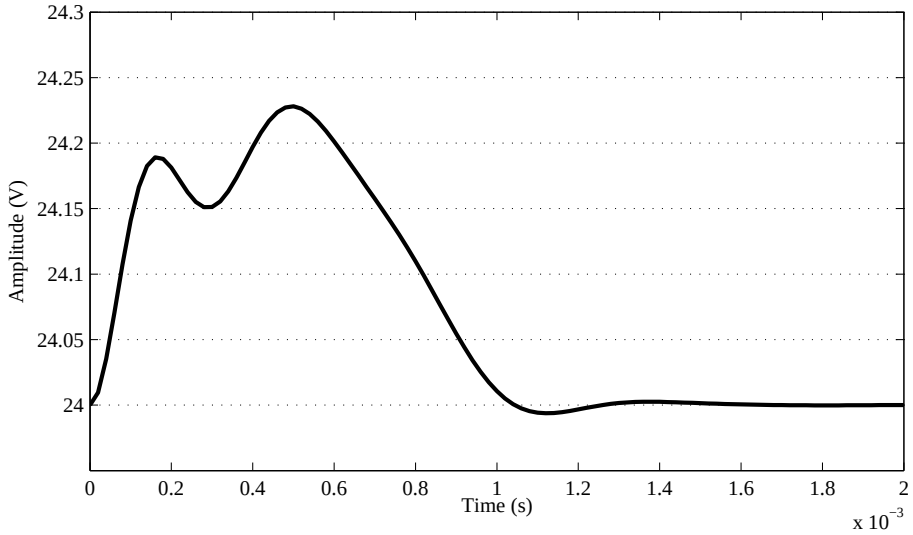


Figure 11.7: Unit step disturbance response of Ćuk converter with ROESFBI compensator.

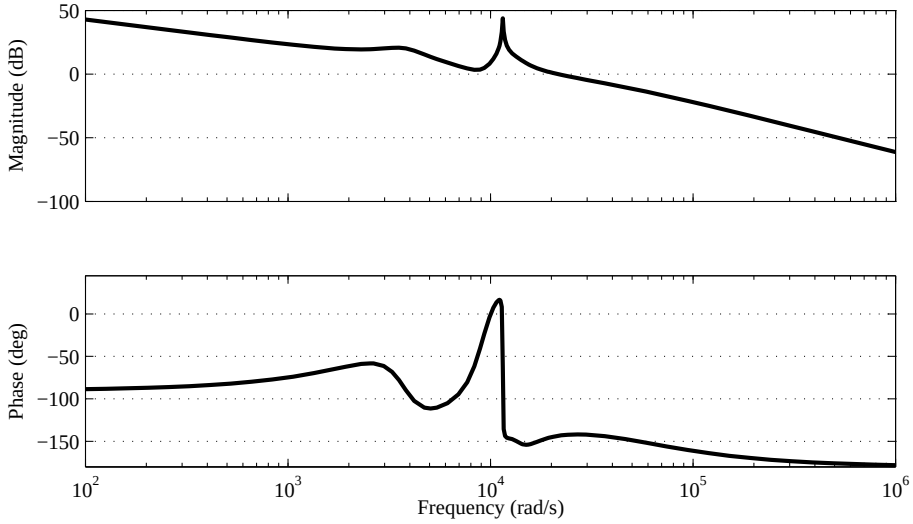


Figure 11.8: Loop gain of Ćuk converter controlled by ROESFBI compensator.

Chapter 12

Linear Quadratic Optimal Control

Linear quadratic optimal control uses penalties on state transients x and control effort u to optimize system performance with respect to a figure of merit determined by a cost function. There is typically a classical trade-off designed into the cost function: one cannot have tight control over state transients with small control effort. In other words, small output transients require large controller gains (and therefore control effort). Additionally, quadratic forms are used to ensure that only the magnitude and not the sign of the transient contributes to the cost determined by the penalty function.

12.1 Linear Quadratic Regulators

To optimally control state transients and control effort within performance specifications, a compensator is sought that seeks to provide a control effort u that minimizes a Lagrangian cost function:

$$J = \int_0^\infty (x^T Q x + u^T R u) dt \tag{12.1}$$

subject to the constraint of the state equation:

$$\dot{x} \quad = \quad Ax + Bu \tag{12.2}$$

This is known as the linear quadratic regulator (LQR) problem. The weight matrix Q is an $n \times n$ positive semidefinite matrix (for a system with n states) that penalizes variation of the state from the desired state. The weight matrix R is an $m \times m$ positive definite matrix that penalizes control effort. Solutions for the constrained optimal system can be found in [?], [?], and [?]. The well-published time invariant solution to this problem is:

$$K = R^{-1} B^T P \tag{12.3}$$

where P is the unique, symmetric, positive definite solution to the steady-state algebraic Riccati equation (ARE):

$$PA + A^T P - PBR^{-1}B^T P + Q = 0 \tag{12.4}$$

The minimum value of the cost function is based on the initial state x_0, and is given by:

$$J_{min} = x_0^T P x_0 \tag{12.5}$$

The LQR designed for a SISO system can be shown to possess very desirable stability properties: it always has a gain margin between {-6 dB, ∞} and a phase margin of at least 60°. However, it has a high frequency roll-off rate of only 20 dB per decade so the open loop frequency response shows susceptibility to high frequency noise.

Since the weight matrices Q and R are both included in the summation term within the cost function, it is really the relative size of the weights within each quadratic form which are important. Simple inspection of the cost function shows that multiplying both weight matrices by the same real constant (e.g., κ) will not affect their ratio. The multiplier κ may be factored out of the integral, thus returning the cost function to its original form. Thus, the problem of minimizing κJ becomes the same as minimizing J. Therefore, holding one weight matrix constant while varying either the individual elements or a scalar multiplier of the other is an acceptable technique for iterative design. It is good for the designer to maintain an understanding of the effects of manipulating individual weights, however. In general, raising the effective penalty a single state or control input by manipulating its individual weight will tighten the control over the variation in that parameter, however it may do so at the expense of larger variation in the other states or inputs.

12.2 Ćuk Converter with LQR Compensator

The fifth-order system formed by augmenting the Ćuk converter with an integral state requires that Q be a five-by-five matrix. To review, the state vector is $[v_2\, v_1\, i_2\, i_1\, x_i]'$, where x_i corresponds to the integral of the reference error e. Since the states have physical significance in this model, it is easy to see that each voltage, current, or error transient may be individually penalized using the diagonal elements of the Q matrix. As the objective of controlling the Ćuk converter is to regulate the output $v_o = v_2$ in the face of disturbances to v_g, penalizing transients that occur on state v_2 is a logical choice, as is penalizing the state x_i associated with the reference error integral as the integral of that error should be minimized to provide for good regulation. Hence, the Q matrix chosen for design of the LQR has two positive entries corresponding to the first (Q_{11}) and last (Q_{55}) entries along the diagonal to ensure it is positive semidefinite. The Ćuk converter has only a single control input, and for initial design R was set equal to 1 arbitrarily. If the control effort exceeds the limitations put on it

(refer to Section 8.5), the value of R may need to be increase to penalize the control effort.

After proceeding through an iterative process where Q_{11} and Q_{55} were varied with R fixed, a finalized design was determined. The step disturbance response of the controlled Ćuk converter is shown in Figure 12.1 The loop gain of the

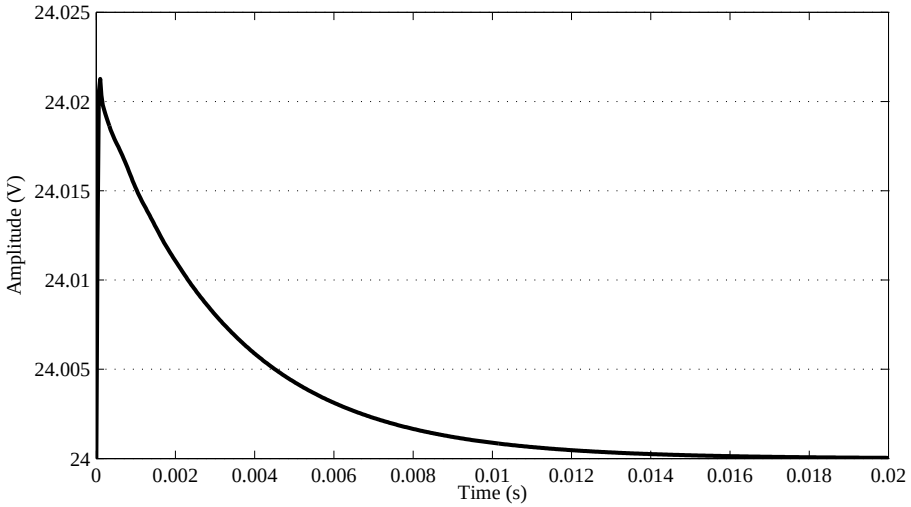


Figure 12.1: Unit step disturbance response of the Ćuk converter controlled by LQR.

controlled system is shown in Figure 12.2, where the loop is broken at the large X shown on the control input d. Figure 12.3 shows the control effort produced by the optimal controller. Note that the time of the unit step disturbance transient with the LQR compensator was significantly longer than the settling times of the previously designed compensators. However, the amplitude deviation was significantly smaller. This is an acceptable design tradeoff since the performance specifications were still met.

12.3 Linear Quadratic Gaussian Regulators

The LQR problem requires that full state feedback be used. This is not always possible, as was discussed in Section 11. The Kalman-Bucy filter is the dual to the LQR problem; it forms an optimal state estimator in the presence of process and measurement noise for a system that is observable. The presence of noise introduces stochastic effects on the state trajectory, therefore, the optimal state estimator must deal with these stochastic effects appropriately by removing them. Since the process of removing noise from a signal is commonly known as filtering, the optimal observer became known as the Kalman filter, or Kalman-Bucy filter, after its creator(s). The Kalman filter is based on essen-

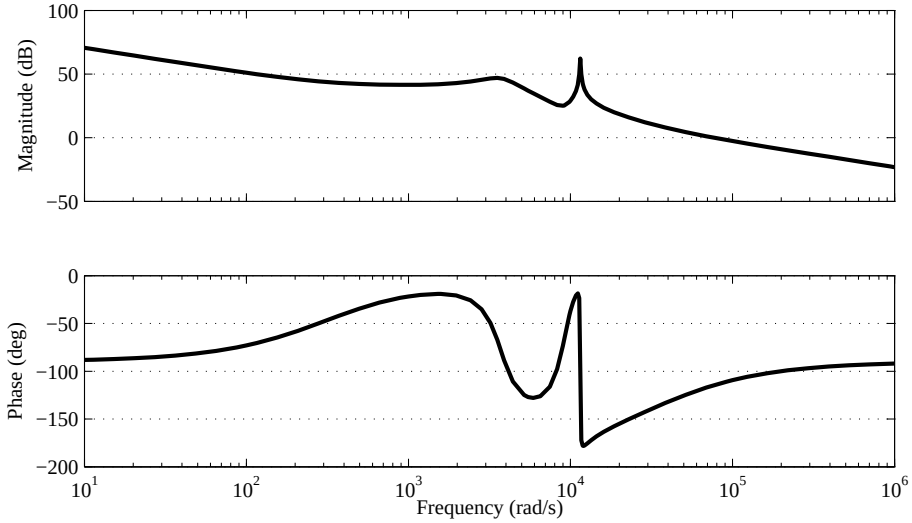


Figure 12.2: Loop gain of Ćuk converter controlled by LQR compensator.

tially the same mathematics as the LQR and, as such, has come to be known as a linear quadratic estimator (LQE). The cost function J_0 that is minimized is the error variance between the state vector and its estimate. LQE calculates the solution to an ARE (which happens to be the error covariance) and uses it to determine L, the estimator gain vector, along the lines of the same equations given for the LQR gain K. Q_0, the covariance matrix of the process noise, and R_0, the covariance matrix of the sensor noise, have to be selected for optimal determination of the observer gain vector L.

When combined, the linear quadratic controller and estimator form a structure known as a linear quadratic Gaussian (LQG) compensator. Once the state variables have been estimated, they are fed back through the controller gain K to close the loop. The separation principle previously mentioned still holds true for LQG design: the LQR and LQE problems can be solved independently via two algebraic Riccati equations.

Adding process disturbances and measurement noise to the state space system description results in:

$$\begin{aligned} \dot{x} &= Ax + Bu + \omega \\ y &= Cx + \nu \end{aligned} \tag{12.6}$$

where ω is the disturbance signal (typically modeled by Gaussian white noise of spectral density Q_0) and ν is additive measurement noise (Gaussian white noise, with spectral density R_0). Note that the fact that neither ω or ν has a coefficient implies a coefficient of I, meaning each state and output has its own distinct noise [?]. The time invariant solution to the optimal estimator problem

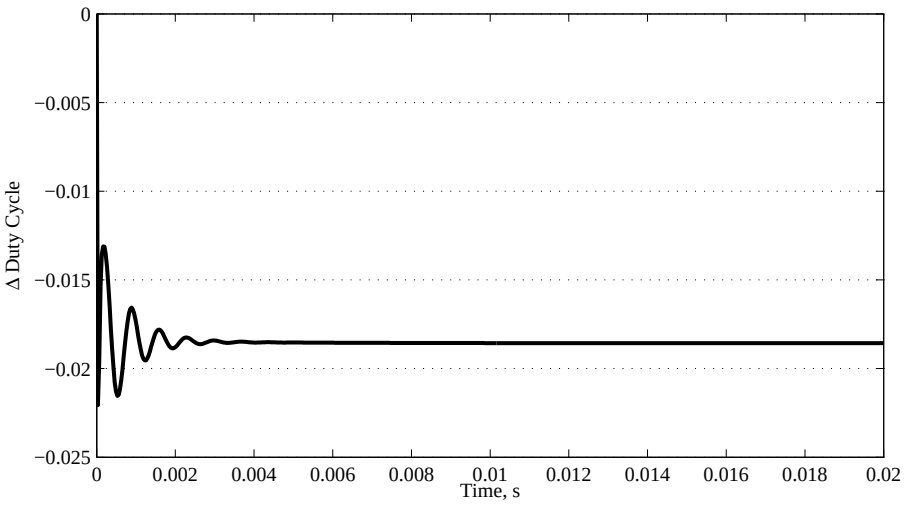


Figure 12.3: LQR control effort.

is then:

$$L = P_0 C^T R_0^{-1} \tag{12.7}$$

where P (known as the estimation error variance) is the unique, symmetric, positive definite solution to the steady-state algebraic Riccati equation:

$$AP_0 + P_0 A^T - P_0 C^T R_0^{-1} C P_0 + Q_0 = 0 \tag{12.8}$$

Since the spectral density of the process and measurement noise in a system is typically unknown, designers frequently treat Q_0 and R_0 as additional design parameters that can be manipulated. The bandwidth of the open-loop system frequency response can be controlled using these matrices. This can allow reduction of the susceptibility of the controlled system to noise at higher frequencies.

12.4 Ćuk Converter with LQG Compensator

The unit step response of the Ćuk converter controlled by a LQG compensator is shown in Figure 12.4. A comparison of the loop gains of the LQR and LQG controlled systems is shown in Figure 12.5, where the loop is broken at the control input d. Loss of gain and phase margins has clearly occurred. Figure 12.6 shows the control effort produced by the LQG controller. Minimal discussion is given to this design as it requires the improvements described in the next section.

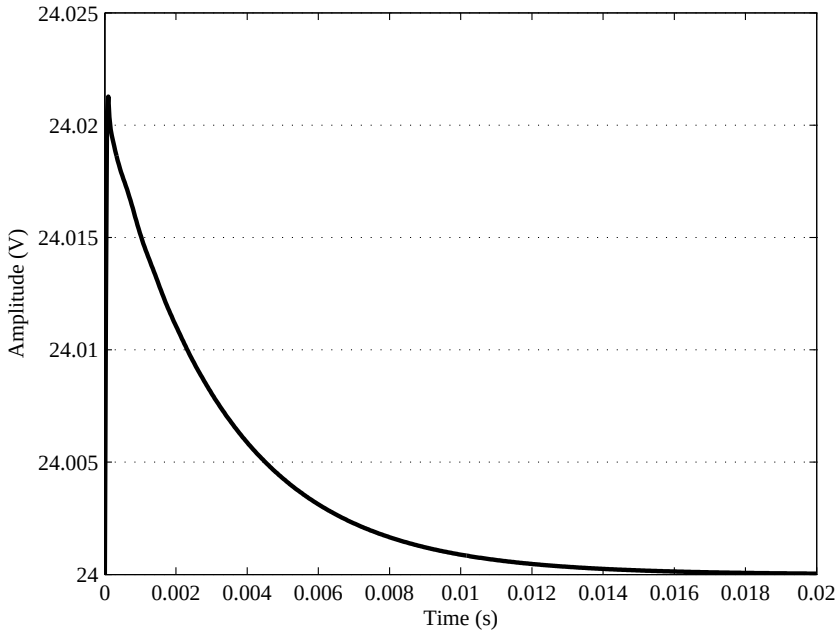


Figure 12.4: Unit step disturbance response of Ćuk converter controlled by LQG compensator.

12.5 Control with LQG/LTR Compensators

Newcomers to the world of optimal control might think that the pairing of the optimal controller formed by the solution of the LQR problem and the optimal estimator formed by the construction of a Kalman filter would have optimal properties. This is not necessarily the case. Doyle [?] provided an example to show that the LQG design loses the guaranteed stability margins of the LQR design when feeding back estimated states. Doyle and Stein [?] then showed how this problem could be addressed. In order to recover the good stability margins and sensitivity properties of an LQR design, an iterative procedure known as loop transfer recovery (LTR) may be performed during the LQG design. (A variety of other methods for LTR have been presented in the controls literature, including several which require employment of subspace methods or special coordinate bases [?], [?], but these techniques are beyond the scope of this work.) The Doyle-Stein method of LTR is performed by iteratively increasing the intensity of the noise covariance matrices used in Kalman filter design. LTR causes the open loop frequency domain characteristics associated with the LQR design to be either exactly or asymptotically recovered as an input noise matrix weighting parameter q is increased. As $q \to \infty$, the properties of the LQR

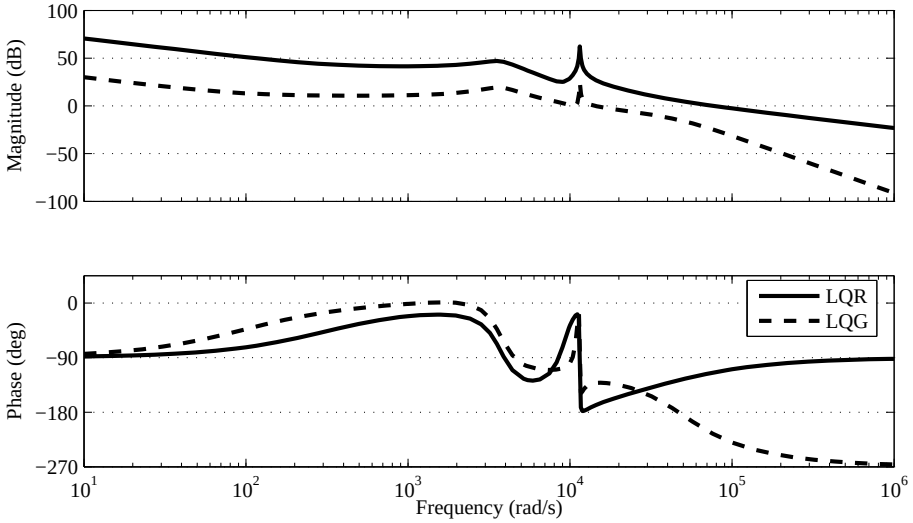


Figure 12.5: Loop gain of Ćuk converter controlled by LQR vs. LQG.

are recovered. Essentially, LTR produces a state estimator whose estimates $\hat{x}$ are independent of the control input u (or only weakly depended on u) and dependent only on the input provided by the plant output y.

Performing the Doyle-Stein method of asymptotic loop transfer recovery on a full-order compensator requires:

- The system must be minimum-phase and strictly proper.
- $R_o = 1$ and $Q_o = q^2 BB'$

The fact that the plant must be minimum-phase (all poles and zeros in the left half of the complex plane and no pure delays) prevents the compensator designed from being unstable, since the LTR technique moves some of the compensator poles toward the plant zeros where pole-zero cancellation makes them unobservable. (Other LTR methods may be used with nonminimum-phase systems by using subspace [?] or loop-shaping techniques [?].) The remainder of the poles (an excess of poles exists because the plant is strictly proper) move toward infinity in the left-half of the complex plane in a Butterworth filter pattern [?].

The effect of loop transfer recovery is to essentially decouple the observer from the control input u by raising the observer gain L so that the state estimate $\hat{x}$ depends only on the plant output y. This is illustrated in Figure 12.7. The decoupling is accomplished by the increasing noise intensity on u, which causes L to increase such that y has a larger contribution to the state estimate.

In order to accomplish LTR, the loop is broken at the large X on the control input shown in Figure 11.1. The loop is explicitly shown in Figure 12.8. The frequency response of the loop from d to d' is driven to asymptotically approach the frequency response of the system with LQR control. Figure 12.9 shows the

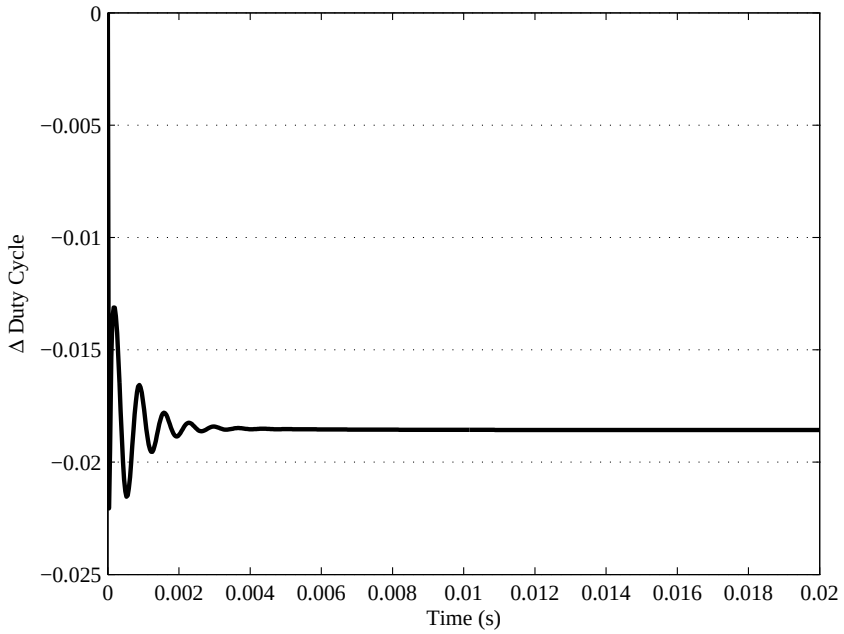


Figure 12.6: LQG control effort.

LQGI/LTR iterative design process applied to the Ćuk converter. Initial LQGI design resulted in a gain margin reduction from infinity to 28.2 dB and a loss of phase margin from 65.4° to 32.7°. The iterative loop transfer recovery process resulted in a controlled system gain margin of 30.2 dB and phase margin of 61.7°. Iteration was stopped at that point since these margins are adequate. Further iterations would result in larger observer gains that may be undesirable during implementation, and recovery of the undesirable high frequency characteristics of the LQR compensator has already begun.

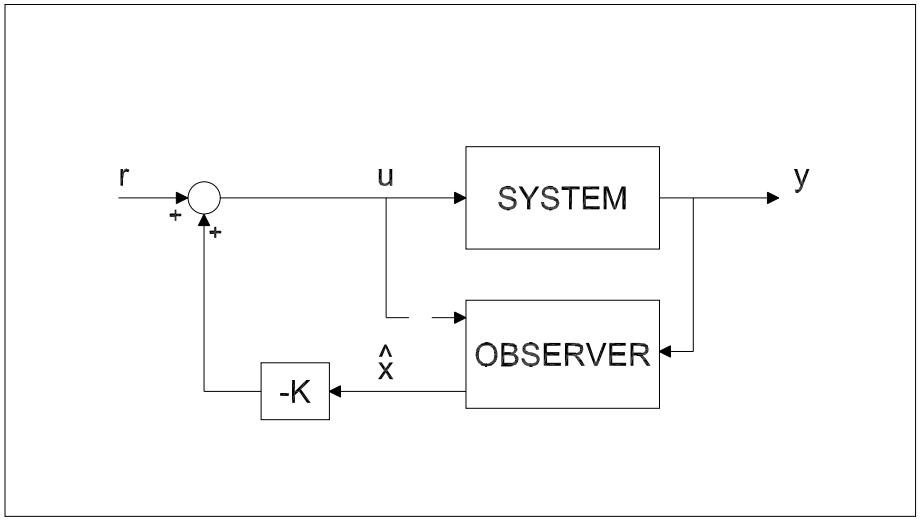


Figure 12.7: Input decoupling effect of loop transfer recovery.

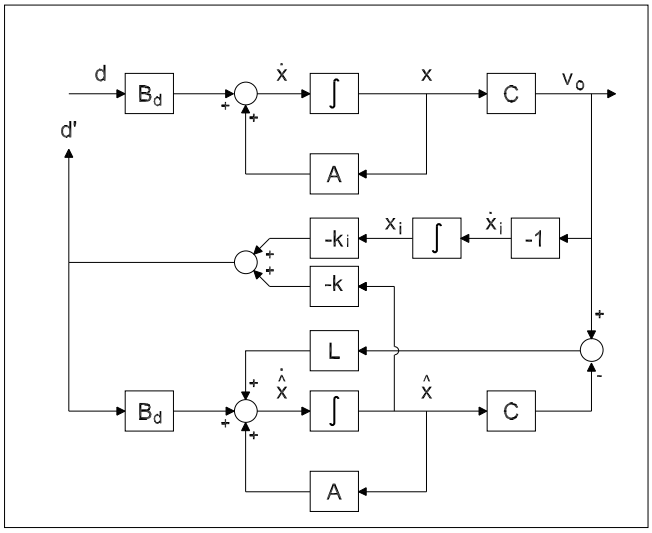


Figure 12.8: The loop to be recovered during loop transfer recovery with a full-order observer.

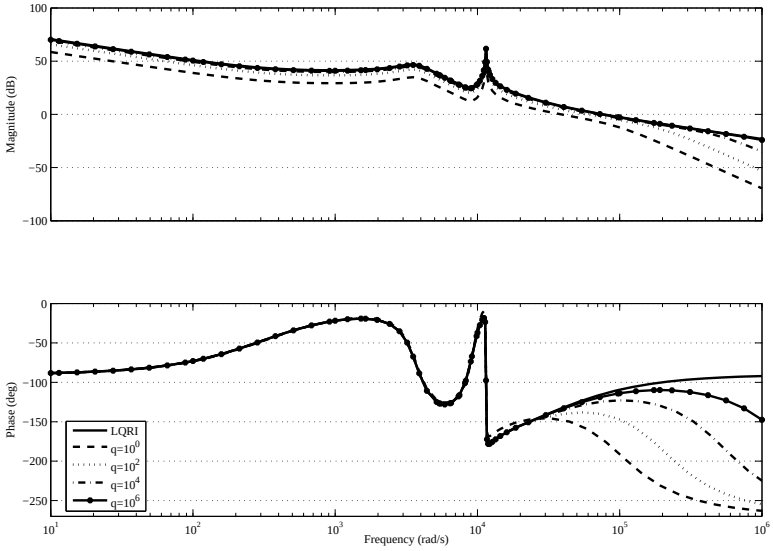


Figure 12.9: Loop transfer recovery of an LQGI compensator.

Chapter 13

Compensator Order Reduction

With the advent of computer control of systems, high-order system models can be created that allow model-based control methods (such as observer-based compensators) to be easily implemented. These digital controller implementations have many advantages over analog controllers, which may be considered to be outdated. However, analog control can often still be performed at the circuit level with a few discrete components and may be more cost-effective to implement when compared to a microprocessor and its associated support circuitry and programming. Thus, this section examines the idea of controller order reduction for use with analog circuitry. It focuses first on reducing the order of an LQGI/LTR compensator using model reduction techniques, then design of an LQGI/LTR compensator using a reduced-order Kalman filter (ROKF), and finally, application of model reduction techniques to the ROKF-based compensator. This final two-step order reduction technique has not been previously seen in the literature.

13.1 Model Reduction of the LQGI/LTR Compensator

Model reduction (MR) may be accomplished by creating a balanced realization (i.e., equal and diagonal controllability and observability Gramian matrices) of the system to be reduced using a linear transformation such as the *balreal* command in MATLAB [?]. Examination of the eigenvalues of the Gramian matrix of the balanced realization allows the designer to identify states that are weakly coupled to both the input and output of the compensator. These states, which are at once both weakly controllable and weakly observable, have small Hankel singular values associated with them. Hankel singular values are determined by taking the square root of the product of the eigenvalues of the controllability

and observability Gramian matrices. In a balanced realization, the Hankel singular values are the diagonal entries of the common controllability/observability Gramian matrix, and the states are ordered from highest to lowest Hankel singular value [**?**]. Compensator states with small Hankel singular values may be eliminated with little impact to the performance of the compensator using the *modred* command in MATLAB.

In this case, the system to be reduced is the compensator. The *balreal* command identifies only two states that may be eliminated from the LQGI/LTR compensator designed previously without significant loss of accuracy, as may be predicted by the information provided from the pole-zero plot in Figure 13.1. Model reduction resulted in the addition of a high-frequency zero for this particular compensator. This zero was a simulation artifact created by the *modred* command, therefore it was removed by truncation.

Examination of the LQGI/LTR compensator poles, zeros, and gain of the transfer function yields:

$$\begin{aligned} p &= \begin{bmatrix} -1490 \pm j9000 & -1129500 \pm j1129500 & 0 \end{bmatrix} \\ z &= \begin{bmatrix} -32410 & -319 & -1440 \pm j9090 \end{bmatrix} \\ k &= 7.195 \times 10^7 \end{aligned} \tag{13.1}$$

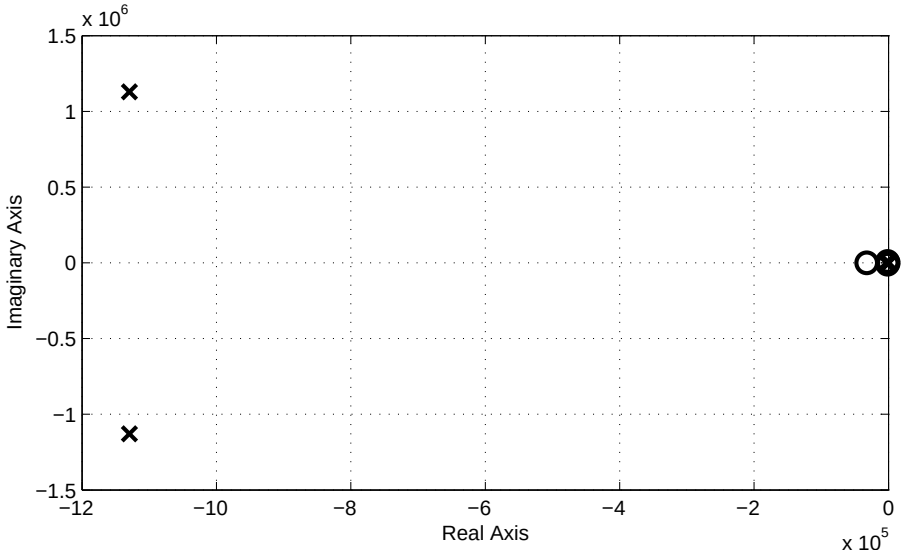


Figure 13.1: Pole-zero plot of the LQGI/LTR compensator.

By comparing the frequencies at which the poles and zeros occur and their complex plane locations, it can be seen that a complex pair of zeros at $-1490 \pm j9000$ essentially cancels out a complex pair of poles at $-1440 \pm j9090$. This is more readily viewed in the close-up view of the pole-zero plot in Figure 13.2. Examination of the compensator after model reduction methods yields:

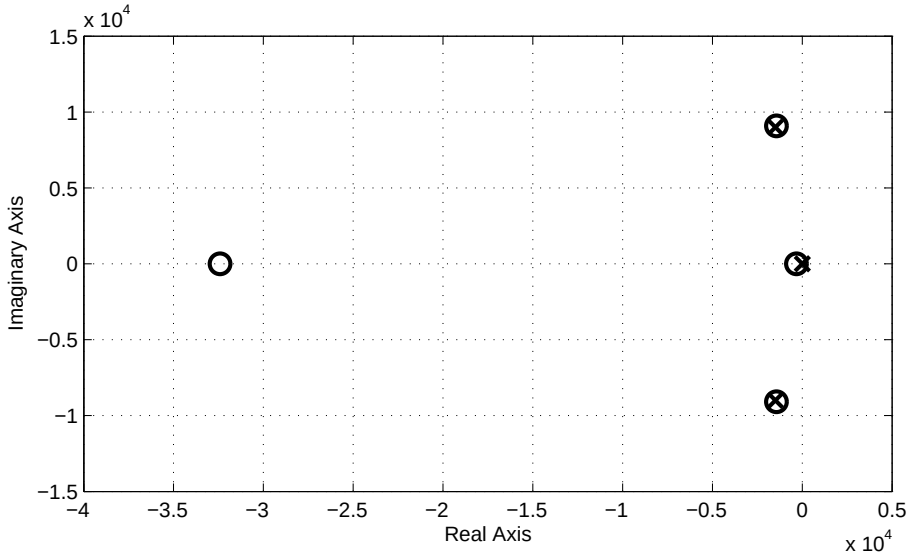


Figure 13.2: Compensator pole-zero plot showing likely pole-zero pair cancellation.

$$\begin{aligned} pr &= \begin{bmatrix} 0 & -1126800 \pm j1132300 \end{bmatrix} \\ zr &= \begin{bmatrix} -319.5 & -33035 \end{bmatrix} \\ kr &= 7.18 \times 10^7 \end{aligned} \tag{13.2}$$

Once model reduction has been accomplished, validation must occur to verify that significant differences do not exist between the full-order and model-reduced compensators. Comparison of the full-order and model-reduced compensator frequency responses is shown in Figure 13.3. Based on this diagram, it is readily apparent that the model-reduced compensator may be used to replace the full-order compensator without significant difference, thus reducing the controller order. The MRLQGI/LTR compensator can then be achieved with less analog circuitry than the LQGI/LTR yet still perform adequately, and therefore may be selected for implementation.

Care must be taken when performing model reduction to ensure desirable stability margins are not lost. Comparable frequency responses between the full-order and model-reduced compensators tell the designer that margins will probably not change appreciably during model reduction. Verification of margins was performed for system with the MRLQGI/LTR compensator; no change in gain margin resulted but phase margin was reduced to 61.2°, a loss of 0.5°, which is not a significant difference.

The step disturbance response for the model-reduced compensator is shown in Figure 13.4. The step disturbance input is attenuated well, with a maximum deviation of just over 20 mV. This would be a perfectly acceptable controller

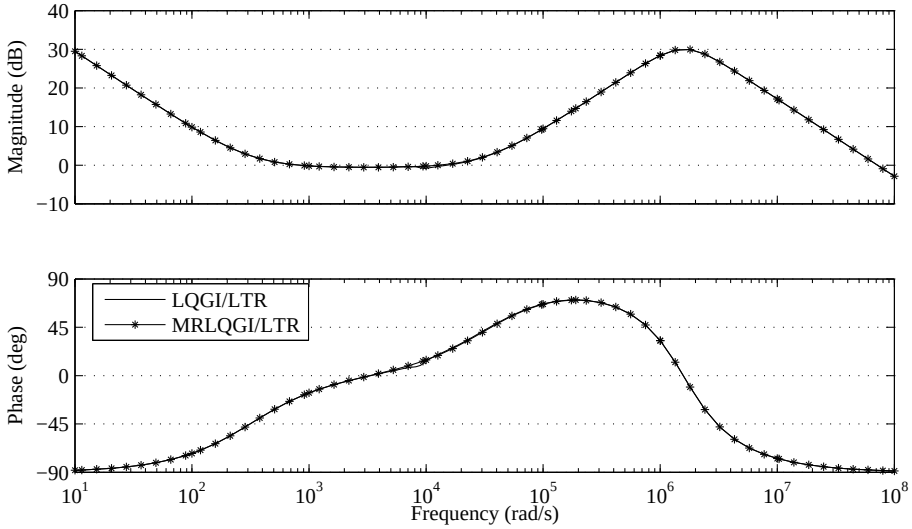


Figure 13.3: Compensator frequency response comparison following model reduction.

for the Ćuk converter, however, additional order reduction (though impossible to achieve in this controller incarnation without significantly impacting performance) would be desirable and is explored in the next section.

13.2 A Reduced-Order LQGI/LTR Compensator

The model-reduced compensator designed in Section 13.1 is based on pole-zero cancellation in a balanced state-space realization of the Kalman filter and truncation to remove a high-frequency zero. However, a compensator based on a LQRI paired with a reduced-order Kalman filter (ROKF) can be designed and the LTR technique applied during the design process in order to develop a ROLQGI/LTR compensator. Madiwale and Williams [**?**] described the mathematics necessary for performing loop transfer recovery with reduced-order linear quadratic compensators and provided proofs that the equations used in this section achieve LTR.

The design of the ROLQGI/LTR compensator begins with construction of a linear quadratic regulator. Once the regulator gain K has been determined, the system matrices and K are partitioned to form a reduced-order observer as in Equation 11.10.

Consider a minimum phase system with process noise ω (with positive definite Gaussian spectral density matrix V) that is distributed into the state dynamics by W and let the system be free from measurement noise in the measured

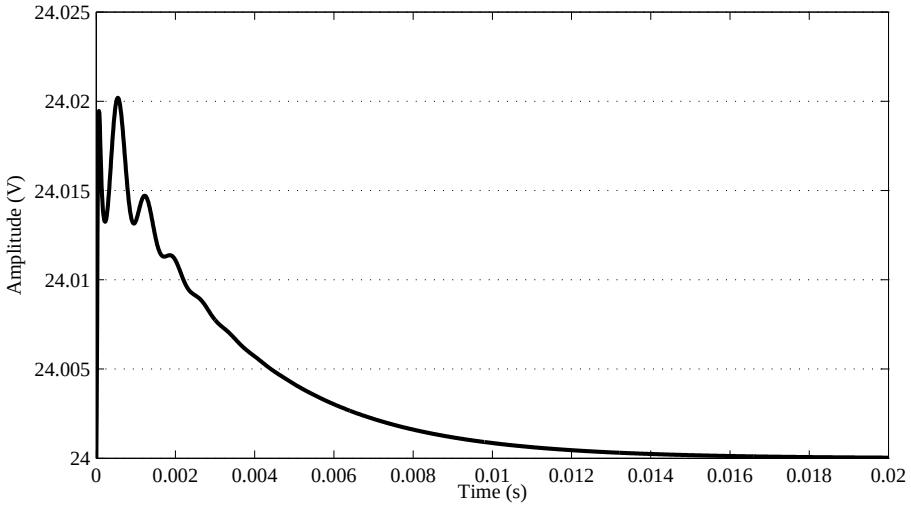


Figure 13.4: Unit step disturbance response of Ćuk converter - MRLQGI/LTR compensator.

state vector x_m:

$$\begin{aligned} \dot{x} &= Ax + Bu + W\omega \\ y &= x_m \end{aligned} \tag{13.3}$$

Process noise characteristics are usually difficult to determine or unknown. Thus, both W and the corresponding noise spectral density V are manipulated as design parameters for determining the optimal reduced-order estimator gain L in a manner similar to the manipulation of Q_0 and R_0 in full-order estimator design methods. Both W and V are also partitioned as in Equation 11.10 in order to form the reduced-order Kalman filter. Let:

$$V_{11} = W_1 V_1 W_1' + q^2 B_1 V_2 B_1' \tag{13.4}$$
$$V_{12} = W_1 V_1 W_2' + q^2 B_1 V_2 B_2' \tag{13.5}$$
$$V_{22} = W_2 V_1 W_2' + q^2 B_2 V_2 B_2' \tag{13.6}$$

Then with:

$$\begin{aligned} \bar{A} &= A_{22} - V_{12}' V_{11}^{-1} A_{12} \\ \bar{V} &= V_{22} - V_{12}' V_{11}^{-1} V_{12} \end{aligned} \tag{13.7}$$

where V_{11} is nonsingular, the following ARE is solved for for Q_o:

$$\bar{A} Q_o + Q_o \bar{A}' - Q_o A_{12}' V_{11}^{-1} A_{12} Q_o + \bar{V} = 0 \tag{13.8}$$

The Kalman filter gain L can then be determined from:

$$L = (Q_o A_{12}' + V_{12}') V_{11}^{-1} \tag{13.9}$$

Now, as q is increased in Equations 13.4-13.6, the target feedback loop of the LQR controller is recovered.

Once again, the loop is broken at the large X on the control input as shown in Figure 11.6. The open loop is shown explicitly in Figure 13.5. The frequency response of the loop from d to d' is again driven to asymptotically approach the frequency response of the system with LQR control as shown in Figure 13.6, which is a plot of the iterative LTR process for this reduced-order compensator and the Ćuk converter.

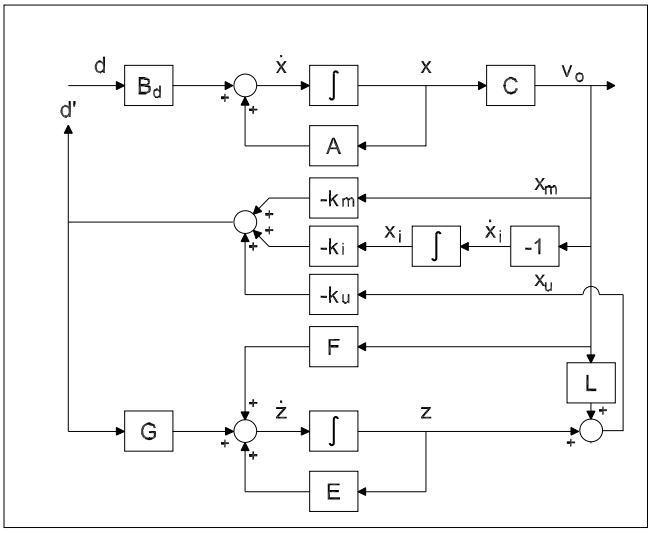


Figure 13.5: Loop transfer recovery with a reduced-order observer.

During simulation, it was found that the original matrices selected to represent the process noise had values that were too large. The initial results showed loop transfer recovery had already occurred, therefore the noise values had to be made smaller to verify that LTR was taking place. For the model of the Ćuk converter to be controlled, the following partitions of the W and V matrices were used to simulate the fictitious noise:

$$W_1 = \begin{bmatrix} 1\times10^{-4} & 0 & 0 \end{bmatrix},\ W_2 = \begin{bmatrix} 1\times10^{-5} & 0 & 0 \\ 0 & 1\times10^{-5} & 0 \\ 0 & 0 & 1\times10^{-5} \end{bmatrix}$$

$$V_1 = \begin{bmatrix} 1\times10^{-5} & 0 & 0 \\ 0 & 1\times10^{-5} & 0 \\ 0 & 0 & 1\times10^{-5} \end{bmatrix},\ V_2 = 1\times10^{-5}$$

The scalar q was allowed to vary from 1×10^{-10} to 1×10^{-7} during the recovery process.

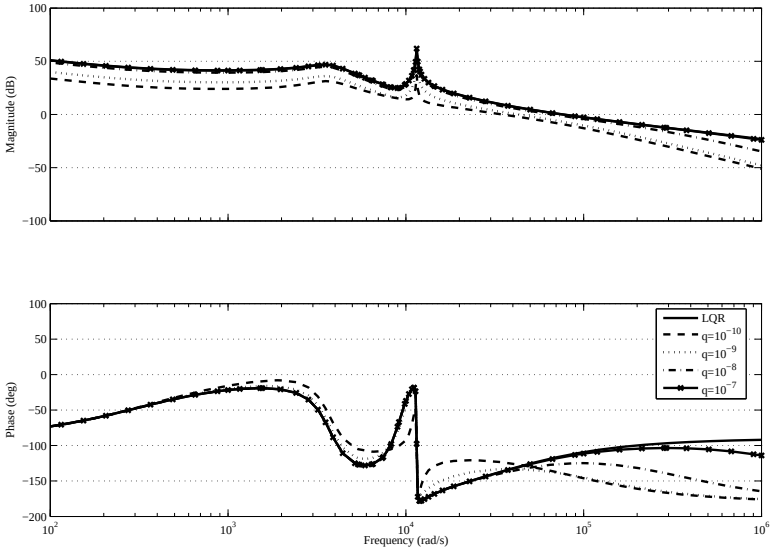


Figure 13.6: Loop transfer recovery of a ROKF-based LQGI compensator.

Examination of the ROLQGI/LTR compensator transfer function yields:

$$\begin{aligned} pr &= \begin{bmatrix} -1490.0 \pm j9000.0 & -2466000.0 & 0.0 \end{bmatrix} \\ zr &= \begin{bmatrix} -32990.0 & -319.2 & -1442.0 \pm j9087.0 \end{bmatrix} \\ kr &= 70.74 \end{aligned} \tag{13.10}$$

which shows a pole-zero pair that could possibly be canceled via model reduction methods. The balanced realization approach to model reduction discussed in Section 13.1 was applied. Comparison of the Hankel singular values produced by the *balreal* command revealed that only two states could be eliminated without significant loss of accuracy in the controller model. Elimination of these states resulted in a second-order compensator that had the following characteristics for its transfer function:

$$\begin{aligned} pr &= \begin{bmatrix} 0.0 & -2469000.0 \end{bmatrix} \\ zr &= \begin{bmatrix} -319.4 & -33570.0 \end{bmatrix} \\ kr &= 70.76 \end{aligned} \tag{13.11}$$

This model-reduced compensator has a pole at the origin and two zeros on the negative real axis left of the pole, which is a classical PID controller. It also has another pole on the negative real axis beyond the zeros, which corresponds to high frequency low-pass filtering. It may therefore be thought of as a feedback

PID compensator with the derivative term acted upon by a first-order low-pass filter. This type of filtered derivative action is implemented in PID controllers to reduce the bandwidth of the controller and associated undesirable amplification of high-frequency noise, as well as to make them implementable (the ideal PID equation is non-causal due to the fact that there is an excess of zeros). This PID controller is very simple to implement with a single inverting operational amplifier configuration. A second inverter buffer stage is needed to eliminate the undesirable inversion caused by the first stage.

A frequency response comparison of the two compensators designed in this section is shown in Figure 13.7. There is excellent correlation between the Bode plots, showing that the MRROLQGI/LTR compensator performance will be almost exactly the same as the ROLQGI/LTR compensator.

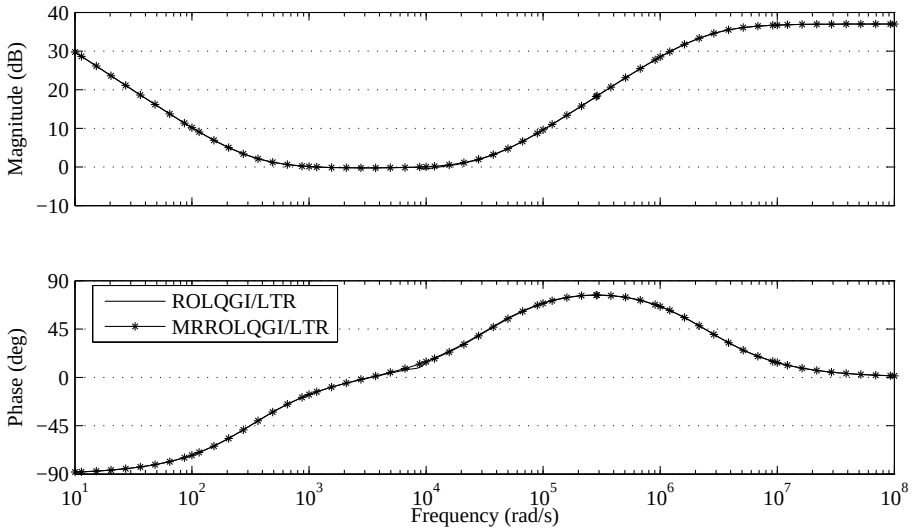


Figure 13.7: Comparison of compensator frequency response - ROLQGI/LTR and MRROLQGI/LTR.

Initial ROLQGI design resulted in no gain margin reduction from infinity but had a loss of phase margin from 65.4° to 56.3°. The iterative loop transfer recovery process resulted in a controlled system phase margin of 63.7°. Further iterations would result in larger observer gains that may be undesirable during implementation. Verification of margins was performed for system with the MRROLQGI/LTR compensator; no change in gain margin resulted but phase margin was reduced to 63.3°, a loss of 0.4°. Again, this is not a significant difference.

The step disturbance response for the model-reduced compensator is shown in Figure 13.8. The step disturbance input is attenuated well, with a maximum deviation of less than 20 mV. This is a perfectly acceptable controller for the Ćuk converter.

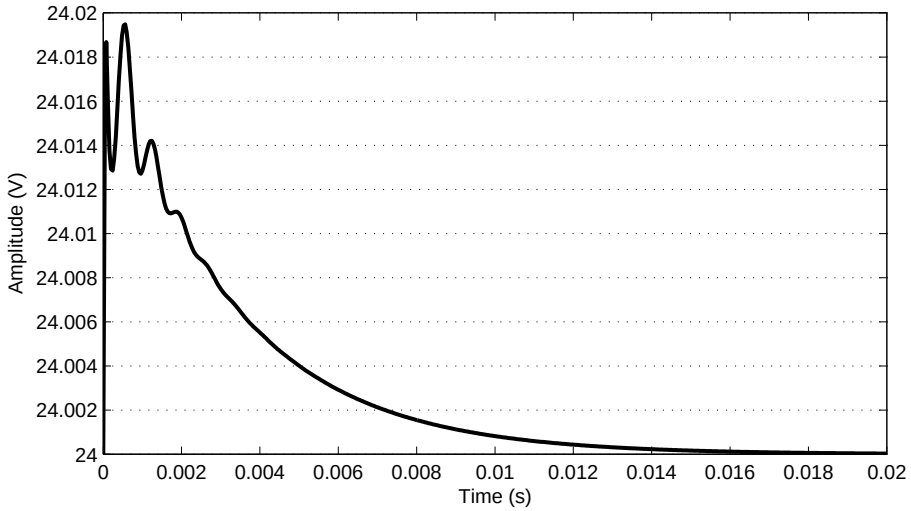


Figure 13.8: Unit step v_g response of Ćuk converter - MRROLQGI/LTR compensator

Chapter 14

Compensator Implementation

At this point, four optimal compensator designs that rely on output feedback and state estimation have been developed. The initial design of the optimal compensator began with a fifth-order controller, with estimated states for each of the four states in the plant and an augmented integral state (LQGI/LTR). Model reduction techniques applied directly resulted in a third-order controller (MRLQGI/LTR), which was a significant improvement in terms of minimizing the circuitry for implementation. The final design began with a fourth-order compensator based on three states from a reduced-order observer augmented by an integral state (ROLQGI/LTR), to which model reduction techniques were applied to form a second-order transfer function (MRROLQGI/LTR). This final regulator had the form of a classical PID controller. The final design had a significant reduction in circuitry yet maintained excellent performance in both the time and frequency domains.

The reduced-order compensators developed in Chapter 13 using model reduction techniques can be implemented with analog circuits using operational amplifiers. The goal is to use the minimum amount of components and circuitry for control (to minimize manufacturing costs) while maintaining adequate controller performance.

14.1 MRLQGI/LTR Compensator Construction

The model-reduced compensator designed in Section 13.1 has two zeros on the negative real axis, a LHP pair of complex poles, and a pole at the origin. This compensator can be implemented by a PI compensator cascaded with a Tow-Thomas biquadratic filter as seen in Figure 14.1. The Tow-Thomas filter is a general second-order filter able to implement low-pass, high-pass, band-pass, notch, and all-pass filters with appropriate choices of coefficients of the filter transfer function [**?**]:

$$T_b(s) = \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{14.1}$$

The biquad filter section is used to implement the second-order denominator term with a simple zero by setting $a_2 = 0$. The PI section is used to implement the other real zero and the pole at the origin. For both sections, it is desirable to keep the poles and zeros within a certain frequency tolerance of each other to keep the component values reasonable in size. The transfer function of the

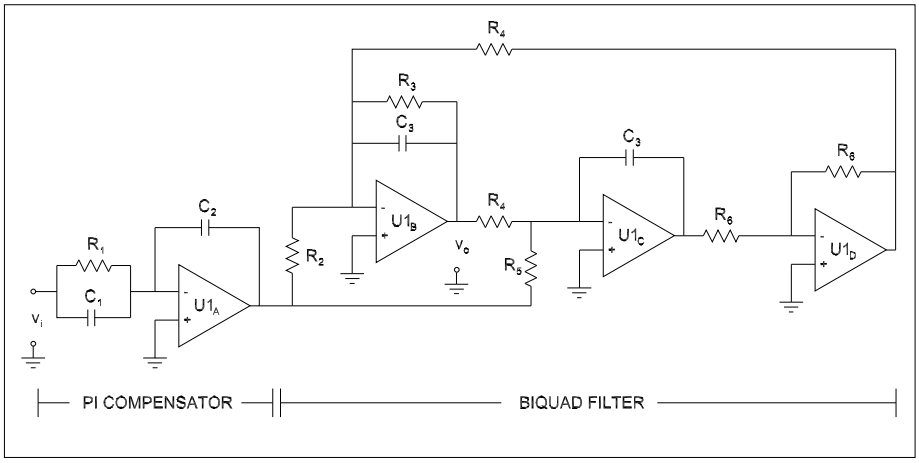


Figure 14.1: The MRLQGI/LTR compensator implemented using operational amplifiers.

PI section is given by:

$$T_p(s) = -\frac{\frac{C_1}{C_2}(s + \frac{1}{C_1 R_1})}{s} \tag{14.2}$$

The transfer function of the biquad filter section is given by:

$$T_b(s) = -\frac{\frac{1}{C_3 R_2}s + \frac{1}{C_3^2 R_4 R_5}}{s^2 + \frac{1}{C_3 R_3}s + \frac{1}{C_3^2 R_4^2}} \tag{14.3}$$

14.2 MRROLQGI/LTR Compensator Construction

A practical example of the MRROLQGI/LTR compensator requires fewer components to implement than the MRLQGI/LTR circuit. It is simply an analog PID controller with a filtered derivative term [**?**]. Consider the circuit in Figure 14.2. With the inverting opamp configuration and some algebraic manipu-

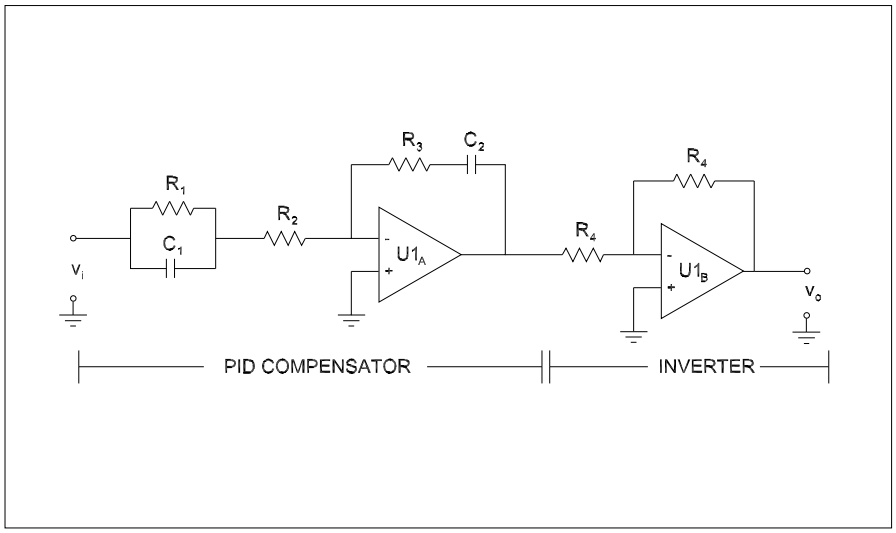


Figure 14.2: The analog MRROLQGI/LTR compensator implementation.

lation, the transfer function is shown to be:

$$T(s) = \frac{\frac{R_3}{R_2}(s+\frac{1}{C_2R_3})(s+\frac{1}{R_1C_1})}{s(s+\frac{R_2+R_1}{R_1R_2C_1})} \tag{14.4}$$

which shows the following zeros, poles, and gain:

$$\begin{aligned} poles &= \left[\begin{array}{cc} 0 & \frac{-(R_2+R_1)}{R_1R_2C_1} \end{array}\right] \\ zeros &= \left[\begin{array}{cc} \frac{-1}{C_2R_3} & \frac{-1}{R_1C_1} \end{array}\right] \\ gain &= \frac{R_3}{R_2} \end{aligned} \tag{14.5}$$

Component values may be determined by equating the expressions in 14.5 with the compensator values given in 7.11. Since there are fewer equations than unknowns, one of the component values must be fixed before the other component values may be determined. The final design used the component values given in Table 14.1.

Table 14.1: Component values for MRROLQGI/LTR compensator implementation.

Component	**Value**
R_1	100 $k\Omega$
R_2	1.4 $k\Omega$
R_3	100 $k\Omega$
C_1	0.29 nF
C_2	31.3 nF

Chapter 15

Power Electronic Circuit Simulation

The MRROLQGI/LTR compensator required the least amount of circuitry and was therefore selected for implementation and testing in PECS. The PECS environment provides for relatively short run times compared to SPICE-based circuit simulation environments since power electronics circuits can typically be simulated with simpler component models than other types of analog circuits.

15.1 Simulating the Controlled Ćuk Converter in PECS

The PECS implementation of the MRROLQGI/LTR compensator design from Section 14.2 connected to the Ćuk converter can be seen in Figure 15.1.

First, the small-signal operation was tested using a step disturbance in v_g as was used during controller design. A simulation was set up to provide for input voltage steps up and down from the nominal 12 V using a unit step to 13 V on the Ćuk input. The simulation used a time step of 1 μs and a run time of 0.1 s. The results of this simulation are shown in Figure 15.2. The maximum deviation in the output voltage is only 0.022 V in response to a step input of 1 V. (Note that ripple voltage exists in the simulation which is not present in the state space averaged model simulations in MATLAB. Neglecting the ripple did not pose a problem, however, during the control system design process.)

Next, a large-signal simulation was set up to provide for input voltage steps up and down from the nominal 12 V through a specified operating range of 9-14 V on the Ćuk input. The results of the large-signal simulation are shown in Figure 15.3. The maximum deviation of 0.11 V in the output voltage occurred when the input voltage drops sharply from 14 V to 9 V but is rapidly brought back under control. This value is well within the 0.24 V tolerance that was specified for controller performance.

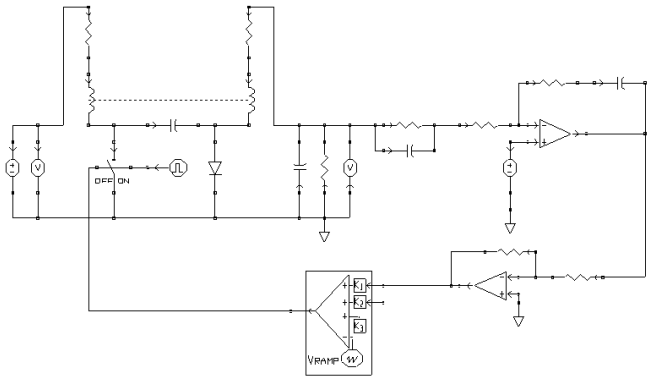


Figure 15.1: PECS simulation of Ćuk converter - MRROLQGI/LTR compensator.

Finally, a simulation was set up to provide for 25% load current steps (0.214 A) around the nominal load current of 0.857 A. The results of this simulation are shown in Figure 15.4. The maximum deviation of 0.175 V in the output voltage occurred when the load current dropped sharply from 1.071 A to 0.643 A, but this is within the transient design specification of regulation to within 1% of the nominal output voltage.

The ability to reject large scale input voltage and load disturbances shows that the compensator design is excellent. The MRROLQGI/LTR controller allowed the system to not only meet the performance specifications, but to exceed them, and achieved these results after two separate reduction of order techniques (reduced-order observer and model reduction) were applied during the design process.

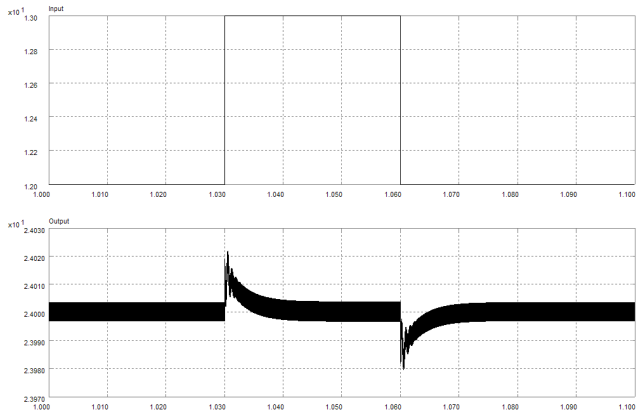


Figure 15.2: Unit step v_g disturbances and v_o response - MRROLQGI/LTR compensator.

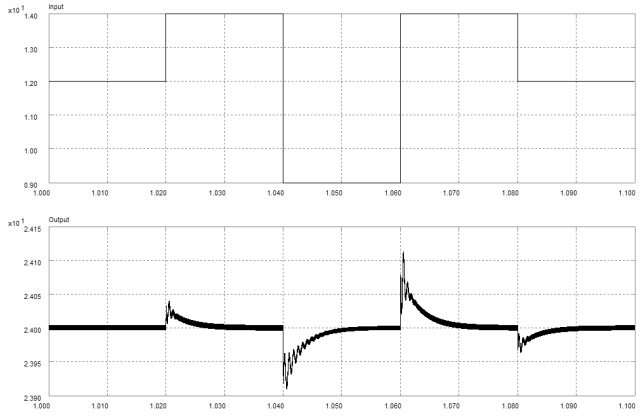


Figure 15.3: Large signal v_g disturbances and v_o response - MRROLQGI/LTR compensator.

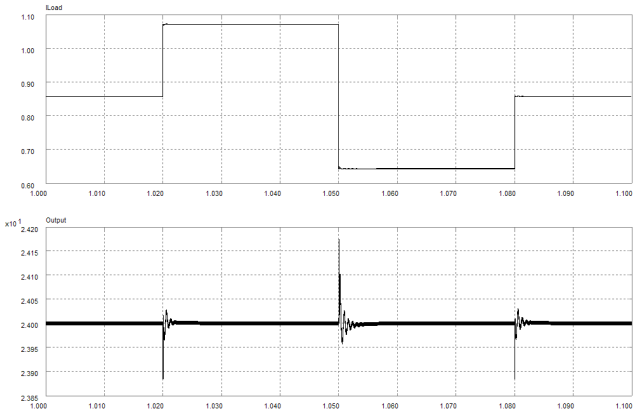


Figure 15.4: Load current disturbance and v_o response - MRROLQGI/LTR compensator.

Chapter 16

Conclusion

Part II demonstrated the process of applying modern control design methods to regulator design for DC-DC converters, and prototypically, to a Ćuk DC-DC converter. Full state feedback control for pole placement was applied - first without integral effort, then with an integrator added. Output compensation using state estimation techniques with full- and reduced-order observers was discussed and simulated. LQR and LQG/LTR techniques were then used to design compensators that were optimized with respect to quadratic performance indices based on state and control effort transients. Balanced realization of the LQGI/LTR compensator identified weakly controllable/observable states, which were then removed using truncation to create a third-order compensator (MR-LQGI/LTR) that could be implemented with a combination PI/Tow-Thomas biquad circuit.

The steps up to this point were typical application of modern state space control methods found in most textbooks. The method that followed (in Section 13.2) resulted in a minimal-order compensator. Namely, when the reduced-order Kalman filter-based compensator design (ROLQGI/LTR) was combined with model reduction using a balanced realization, the result was a second-order compensator (MRROLQGI/LTR) that could be implemented by an analog PID circuit. This MRROLQGI/LTR controller was applied to the Ćuk converter in a power electronics modeling environment and showed excellent input voltage and load current disturbance rejection abilities. The two-step order reduction combination of reduced-order observer design and truncated balanced realization is a novel design method that, while applied to one of the more complex DC-DC converters, appears to be applicable to compensator design in general.

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Routh-Hurwitz Stability Analysis

To determine if a system is stable, it is necessary to determine if the system denominator polynomial has right half-plane roots. For polynomials of a higher order than two, the quadratic formula is insufficient to determine stability.

A widely used method of determining the number of RHP roots for higher order systems is the Routh-Hurwitz test. The Routh-Hurwitz test is a numerical procedure for determining the numbers of RHP and imaginary axis (IA) roots of a polynomial.

Consider the following polynomial:

$$p(s) = a_n s^n + a_{n-1} + ... + a_1 s + a_0$$

The coefficients of the polynomial are arranged as follows in Figure 1:

The system is considered stable if there are no sign changes in the first column. The coefficients populated in Figure 1 are calculated as follows:

$$b_1 = \frac{-\begin{vmatrix} a_n & a_{n-2} \\ a_{n-1} & a_{n-3} \end{vmatrix}}{a_{n-1}} = \frac{a_{n-1}a_{n-2} - a_n a_{n-3}}{a_{n-1}}$$

$$b_2 = \frac{-\begin{vmatrix} a_n & a_{n-4} \\ a_{n-1} & a_{n-5} \end{vmatrix}}{a_{n-1}} = \frac{a_{n-1}a_{n-4} - a_n a_{n-5}}{a_{n-1}}$$

s^n	a_n	a_{n-2}	a_{n-4}	
s^{n-1}	a_{n-1}	a_{n-3}	a_{n-5}	
s^{n-2}	b_1	b_2	b_3	...
s^{n-3}	c_1	c_2	c_3	
s^{n-4}	d_1	d_2	d_3	
$\vdots$				
s^0				

Figure 1: Routh Hurwitz analysis

$$c_1 = \frac{-\begin{vmatrix} a_{n-1} & a_{n-3} \\ b_1 & b_2 \end{vmatrix}}{b_1} = \frac{b_1 a_{n-3} - b_2 a_{n-1}}{b_1}$$

$$c_2 = \frac{-\begin{vmatrix} a_{n-1} & a_{n-5} \\ b_1 & b_3 \end{vmatrix}}{b_1} = \frac{b_1 a_{n-5} - b_3 a_{n-1}}{b_1}$$

An example to illustrate the Routh-Hurwitz method is presented with the polynomial below:

$$p(s) = 4s^4 + 3s^3 + 10s^2 + 8s + 1$$

$$b_1 = \frac{-\begin{vmatrix} 4 & 10 \\ 3 & 8 \end{vmatrix}}{3} = -\frac{2}{3}$$

$$b_2 = \frac{-\begin{vmatrix} 4 & 1 \\ 3 & 0 \end{vmatrix}}{3} = 1$$

$$b_3 = \frac{-\begin{vmatrix} 4 & 0 \\ 3 & 0 \end{vmatrix}}{3} = 0$$

$$c_1 = \frac{-\begin{vmatrix} 3 & 8 \\ -\frac{2}{3} & 1 \end{vmatrix}}{-\frac{2}{3}} = \frac{25}{2}$$

$$c_2 = \frac{-\begin{vmatrix} 3 & 0 \\ -\frac{2}{3} & 0 \end{vmatrix}}{-\frac{2}{3}} = 0$$

$$d_1 = \frac{-\begin{vmatrix} -\frac{2}{3} & 1 \\ \frac{25}{2} & 0 \end{vmatrix}}{\frac{25}{2}} = 1$$

$$d_2 = \frac{-\begin{vmatrix} -\frac{2}{3} & 0 \\ \frac{25}{2} & 0 \end{vmatrix}}{\frac{25}{2}} = 0$$

s^4	4	10	1
s^3	3	8	0
s^2	$-\frac{2}{3}$	1	0
s^1	$\frac{25}{2}$	0	
s^0	1	0	

Figure 2: Routh Hurwitz analysis worked example

The two sign changes in the left column indicate that $p(s)$ has two RHP roots.

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