EE 445/545

POWER ELECTRONICS DESIGN I

TYMERSKI

INDEX

HOMEWORK (HW) AND PROJECTS

HW : BUCK CONVERTER

HW : ERICKSON (1st EDITION) 2.2 + 2.3

HW : STATE EQUATIONS

HW : BUCK - BOOST CONVERTER

HW : ERICKSON (1st EDITION) 3.3 + 3.6

HW : ERICKSON (1st EDITION) 4.4

HW : DCM (DISCONTINUOUS CONDUCTION MODE)

HW : ERICKSON (1ST EDITION) 5.5 + 5.6

HW : FORWARD CONVERTER

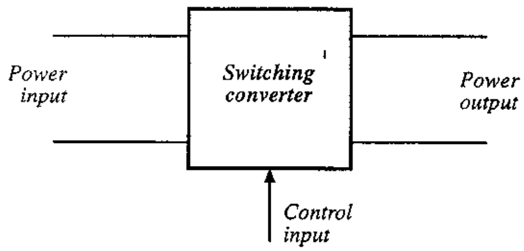
SAMPLE EXAM

PROJECT # 1

LAB.

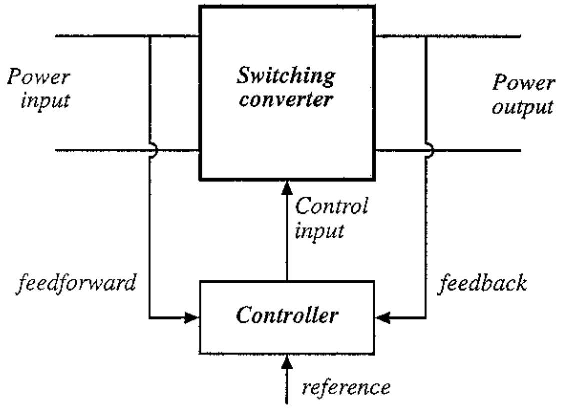
Chapter 1: Introduction

1.1 Introduction to Power Processing



Dc-dc conversion:	Change and control voltage magnitude
Ac-dc rectification:	Possibly control dc voltage, ac current
Dc-ac inversion:	Produce sinusoid of controllable magnitude and frequency
Ac-ac cycloconversion:	Change and control voltage magnitude and frequency

Control is invariably required



High efficiency is essential

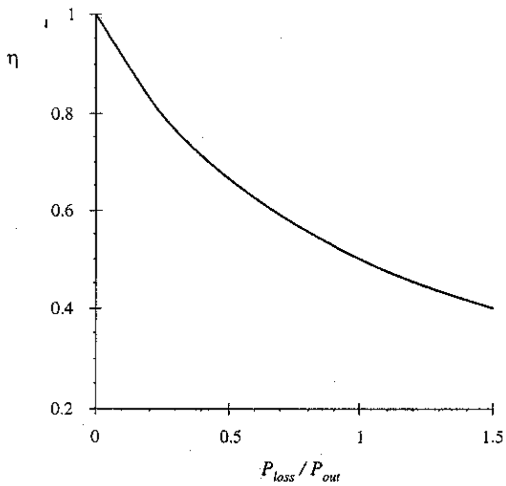
$$\eta = \frac{P_{out}}{P_{in}}$$

$$P_{loss} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta} - 1\right)$$

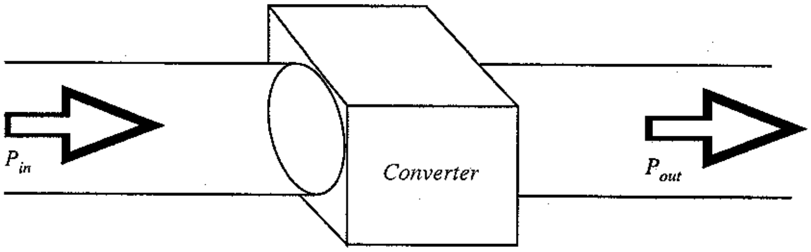
High efficiency leads to low power loss within converter

Small size and reliable operation is then feasible

Efficiency is a good measure of converter performance

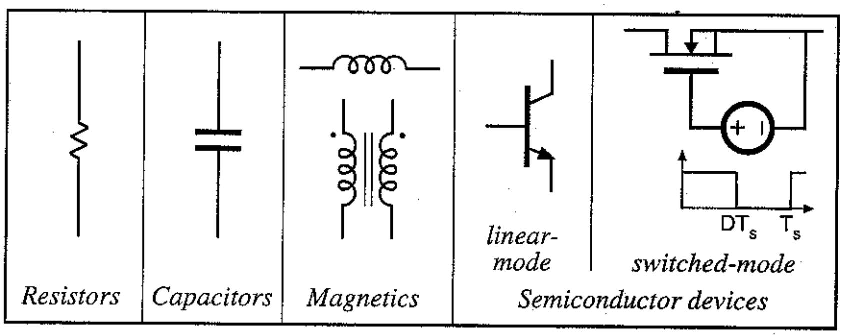


A high-efficiency converter

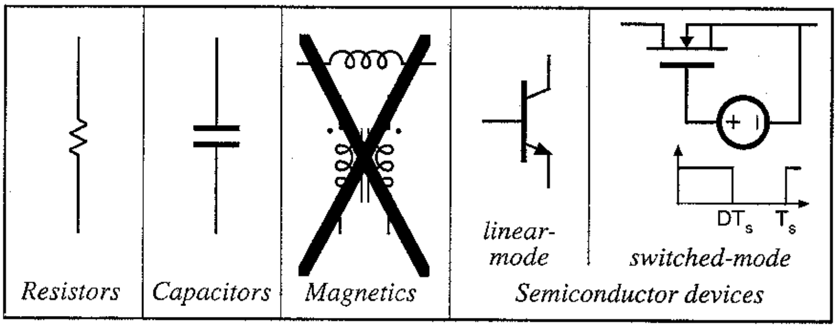


A goal of current converter technology is to construct converters of small size and weight, which process substantial power at high efficiency

Devices available to the circuit designer

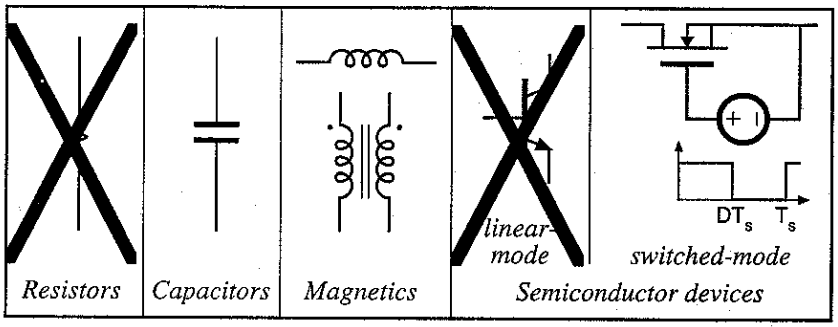


Devices available to the circuit designer



Signal processing: avoid magnetics

Devices available to the circuit designer



Power processing: avoid lossy elements

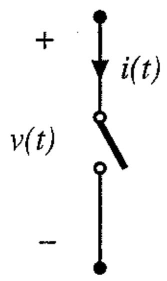
Power loss in an ideal switch

Switch closed: $v(t) = 0$

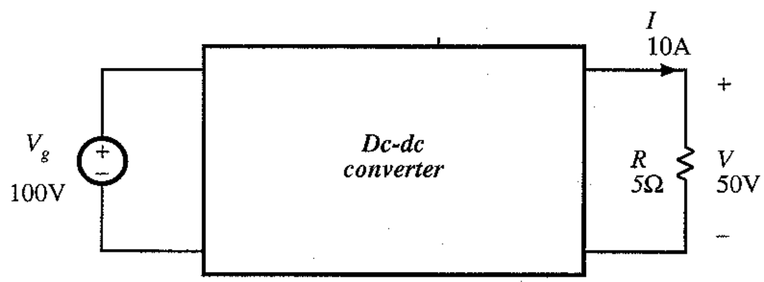
Switch open: $i(t) = 0$

In either event: $p(t) = v(t)\, i(t) = 0$

Ideal switch consumes zero power



A simple dc-dc converter example



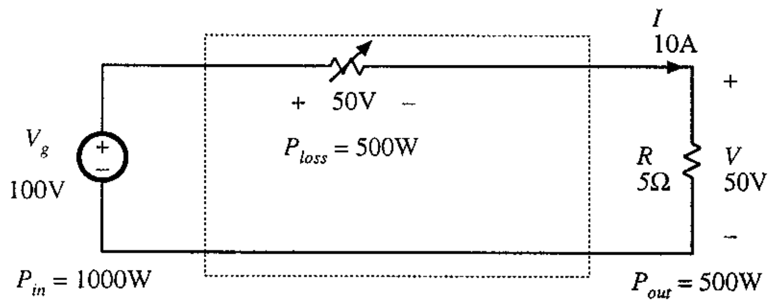
Input source: 100V

Output load: 50V, 10A, 500W

How can this converter be realized?

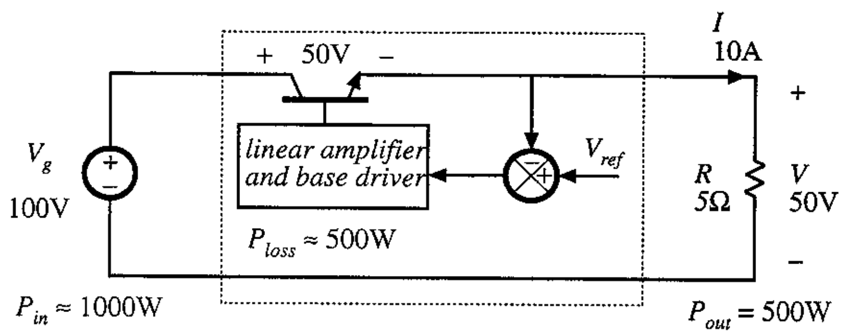
Dissipative realization

Resistive voltage divider

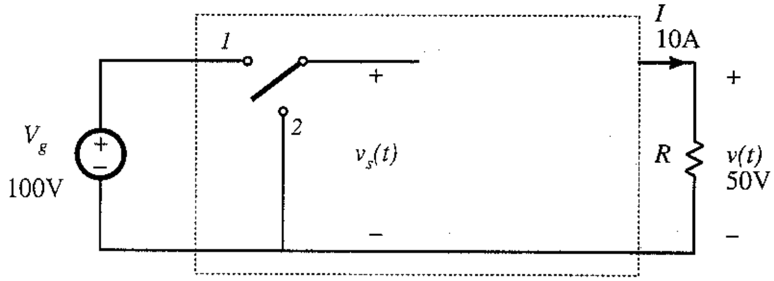


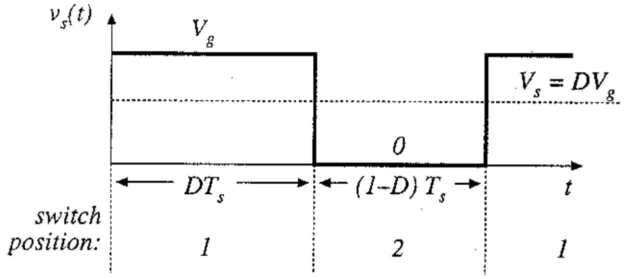
Dissipative realization

Series pass regulator: transistor operates in active region

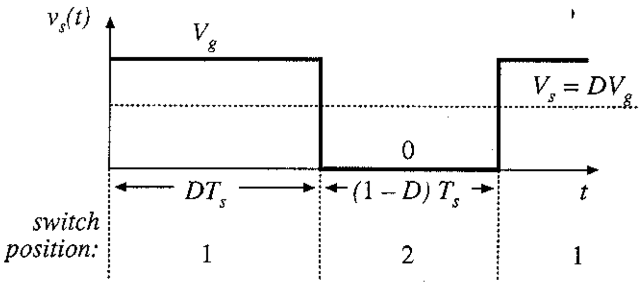


Use of a SPDT switch





The switch changes the dc voltage level



D = switch duty cycle
$0 \leq D \leq 1$

T_s = switching period

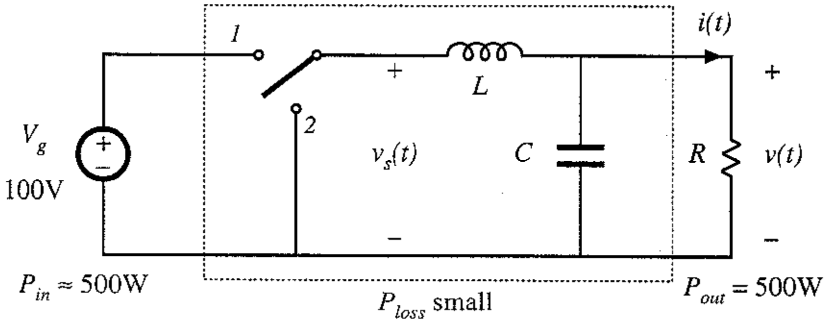
f_s = switching frequency
$= 1 / T_s$

DC component of $v_s(t)$ = average value:

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt = DV_g$$

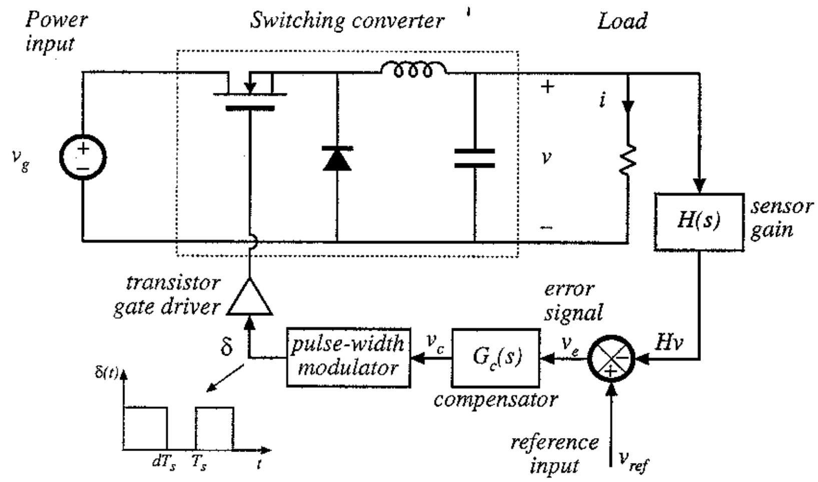
Addition of low pass filter

Addition of (ideally lossless) L-C low-pass filter, for removal of switching harmonics:

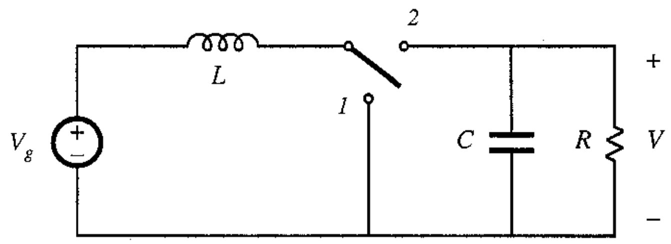


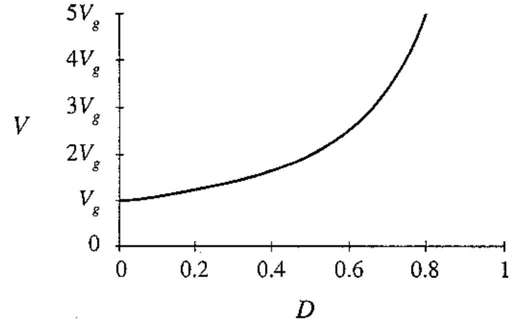
- Choose filter cutoff frequency f_0 much smaller than switching frequency f_s
- This circuit is known as the “buck converter”

Addition of control system for regulation of output voltage

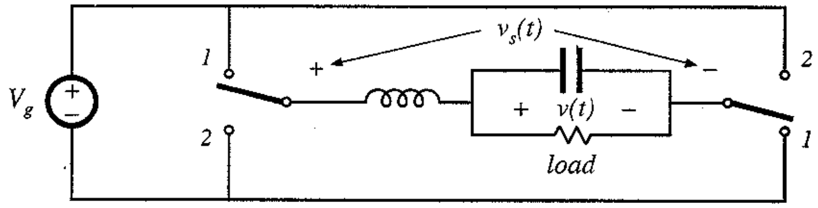


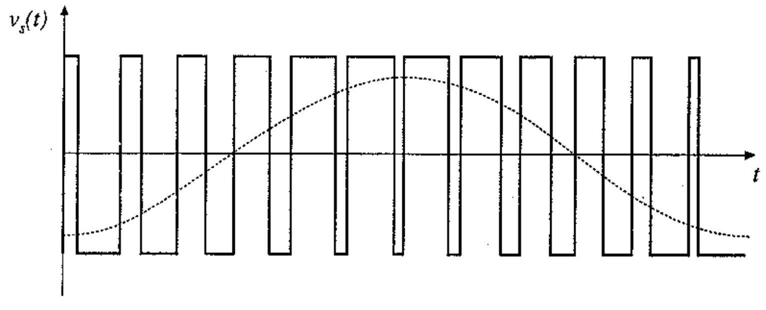
The boost converter





A single-phase inverter





"H-bridge"

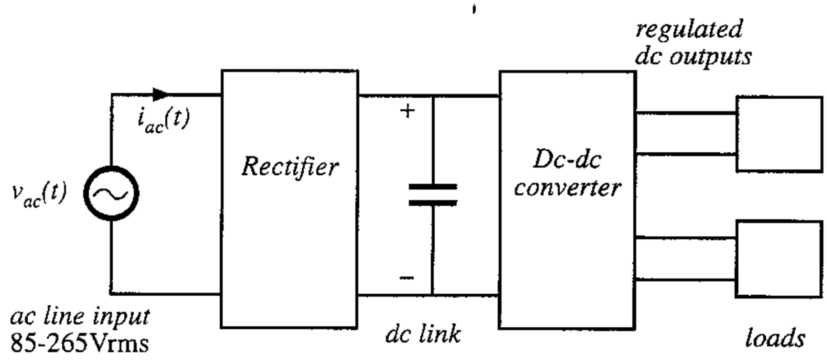
Modulate switch duty cycles to obtain sinusoidal low-frequency component

1.2 Several applications of power electronics

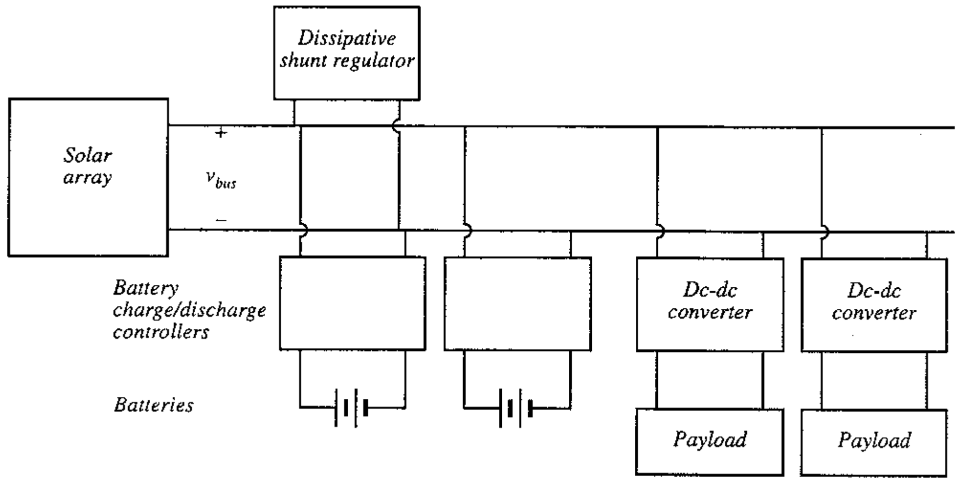
Power levels encountered in high-efficiency converters

- less than 1 W in battery-operated portable equipment
- tens, hundreds, or thousands of watts in power supplies for computers or office equipment
- kW to MW in variable-speed motor drives
- 1000 MW in rectifiers and inverters for utility dc transmission lines

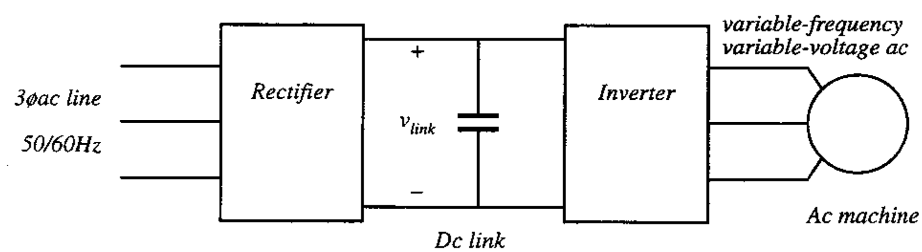
A computer power supply system



A spacecraft power system



A variable-speed ac motor drive system



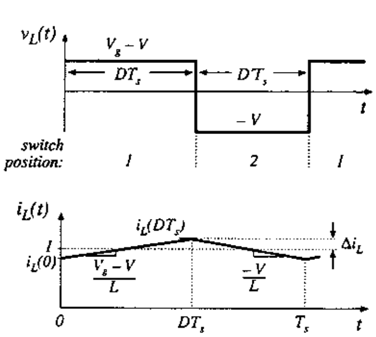
1.3 Elements of power electronics

Power electronics incorporates concepts from the fields of

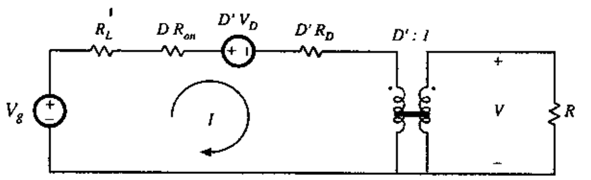
- analog circuits
- electronic devices
- control systems
- power systems
- magnetics
- electric machines
- numerical simulation

Part I. Converters in equilibrium

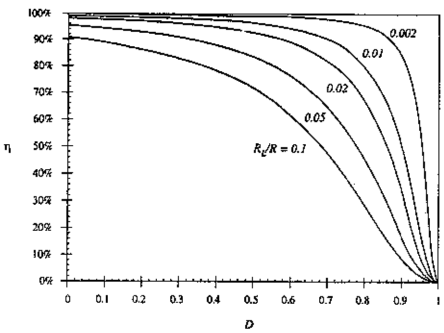
Inductor waveforms



Averaged equivalent circuit



Predicted efficiency

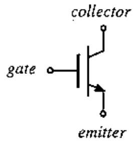


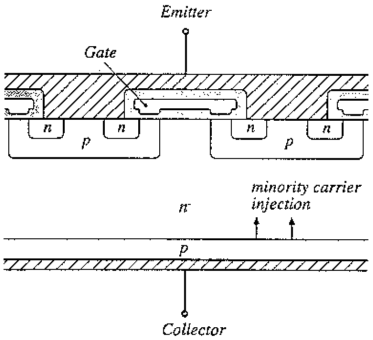
Discontinuous conduction mode

Transformer isolation

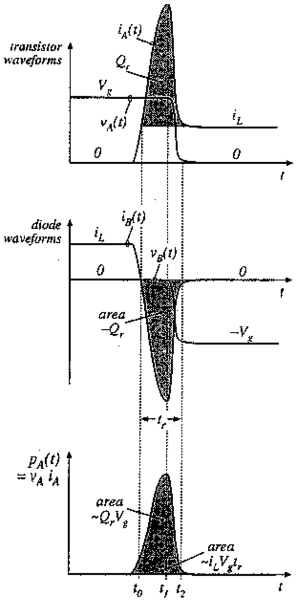
Switch realization: semiconductor devices

The IGBT





Switching loss

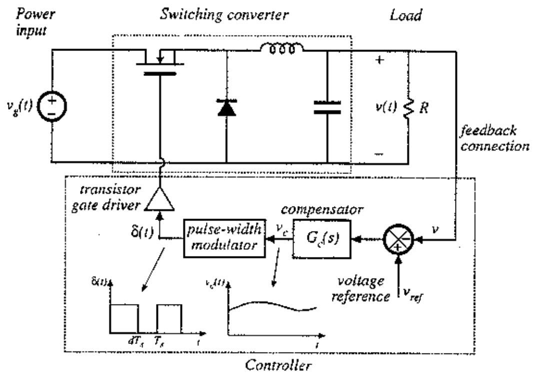


Part I. Converters in equilibrium

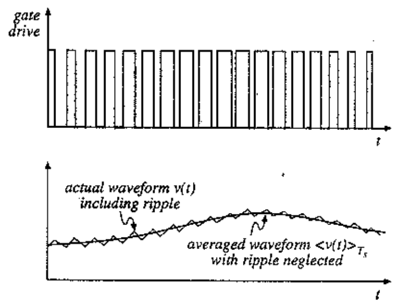
2. Principles of steady state converter analysis
3. Steady-state equivalent circuit modeling, losses, and efficiency
4. Switch realization
5. The discontinuous conduction mode
6. Converter circuits

Part II. Converter dynamics and control

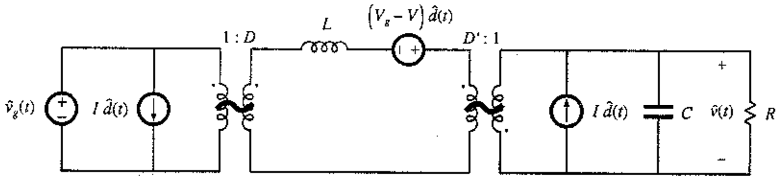
Closed-loop converter system



Averaging the waveforms



Small-signal averaged equivalent circuit

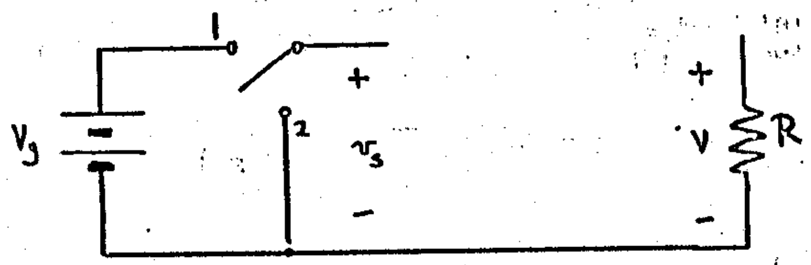


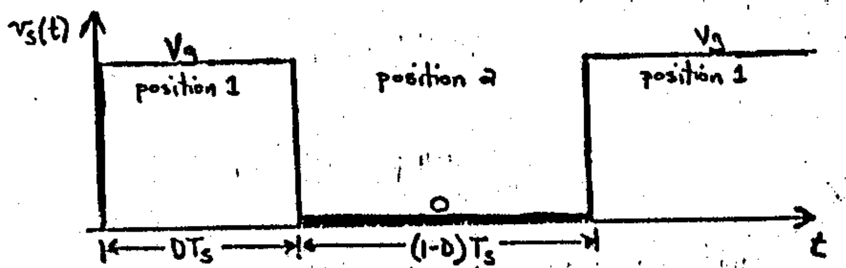
Part II. Converter dynamics and control

7. Ac modeling
8. Converter transfer functions
9. Controller design
10. Ac and dc equivalent circuit modeling of the discontinuous conduction mode
11. Current-programmed control

Lecture 2: Principles of steady-state analysis

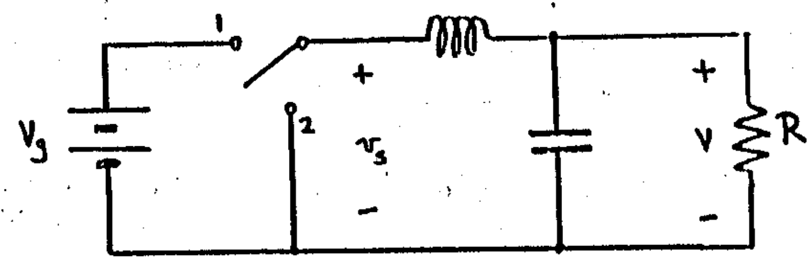
Buck Converter



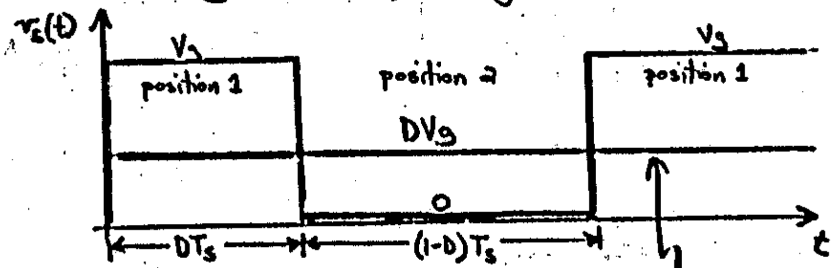


T_s = Switching Period = $1/f_s$
D = Duty Ratio

Buck Converter



Insertion of low-pass filter to remove switching harmonics, leaving dc component.



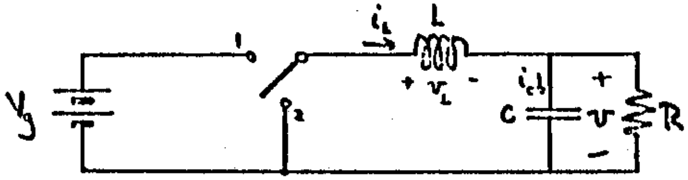
T_s = Switching Period = $1/f_s$
D = Duty Ratio

DC component = average value of $v_s(t)$

$$\langle v_s \rangle = \frac{1}{T_s}\int_0^{T_s} v_s(\tau)\,d\tau = DV_g$$

$$\boxed{V = DV_g}$$

Buck converter



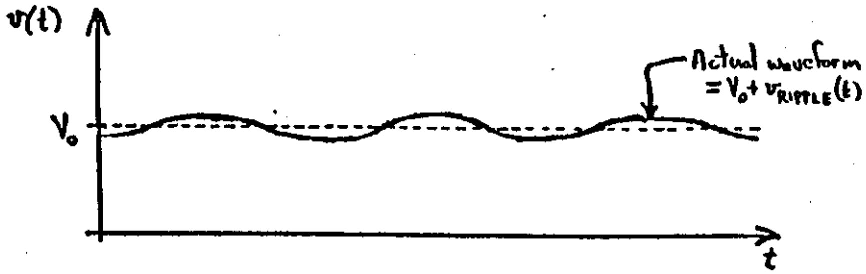
Switching ripple – Results from incomplete attenuation of high-frequency components by the low-pass filter.

Hence, $v(t) = V_0 + v_{RIPPLE}(t)$

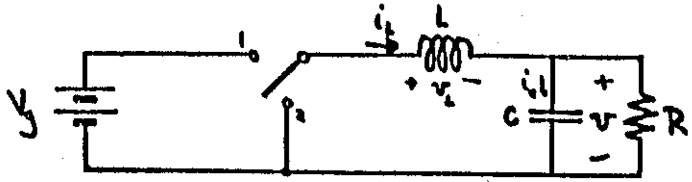
$v(t)$ = actual output voltage
V_0 = desired dc output
v_{RIPPLE} = undesired switching ripple

In a well-designed converter,

$$\boxed{|v_{RIPPLE}| << V_0 \quad \Rightarrow \quad v(t) \approx V_0}$$

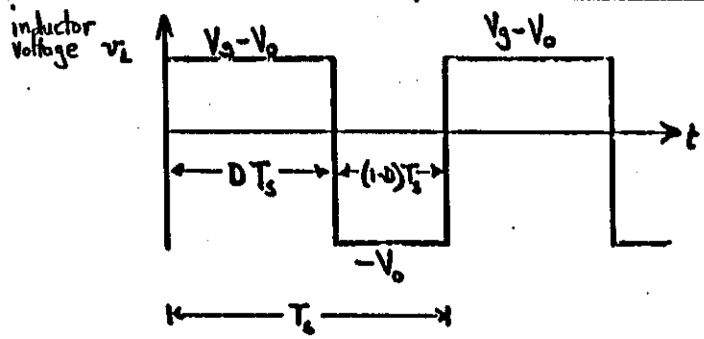


Buck converter



Inductor current and voltage waveforms

Switch in position 1	Switch in position 2
	
$v_L = V_g - v \approx V_g - V_0$	$v_L = -v \approx -V_0$



Knowing the inductor voltage waveform, the current can be found by use of

$$v_L = L\,\frac{di_L}{dt}$$

Thus during the first interval when $v_L \cong V_g - V_o$, the slope of the inductor current waveform is

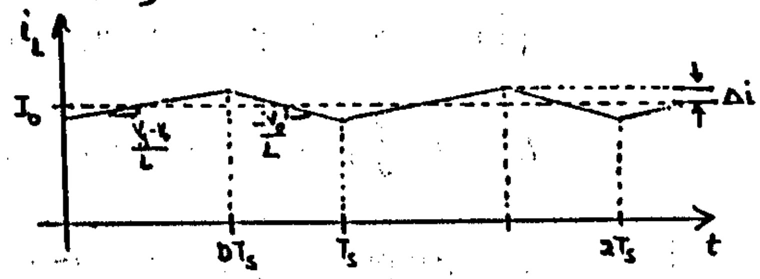
$$\frac{di_L}{dt} = \frac{v_L}{L} \approx \frac{V_g - V_o}{L}$$

Since v_L is essentially constant (during the first interval) in a well-designed converter, then the inductor current waveform i_L is essentially linear.

Similar arguments apply during the second interval: $v_L \cong -V_o$, and hence

$$\frac{di_L}{dt} \cong -\frac{V_o}{L}$$

Thus, the inductor current waveform is



The peak-to-peak inductor current ripple is

$$2\Delta i = \underbrace{\frac{V_g - V_o}{L}}_{\text{slope}} DT_s = \frac{V_o}{L}(1-D)T_s$$

$$\Rightarrow \boxed{\Delta i = \frac{V_g - V_o}{2L}\,DT_s}$$

Thus, for the buck converter, the inductor current ripple depends on the input voltage V_g, the output voltage V_o, the duty ratio D, the switching period T_s, and inductance L.

Calculation of Steady-State Voltages and Currents

1. The principle of inductor volt-second balance

Integration of the relation $v_L = L\frac{di_L}{dt}$ over one switching interval yields

$$i_L(T_s) - i_L(0) = \frac{1}{L}\int_0^{T_s} v_L(t)\,dt$$

In steady-state, the initial and final values of inductor current must be equal: $i_L(T_s) = i_L(0)$. Hence, in steady-state we have

$$0 = \int_0^{T_s} v_L(t)\,dt$$

Dividing by T_s yields

$$\boxed{0 = \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt = \text{average inductor voltage}}$$

Thus, the average (dc component) of the inductor voltage must be zero in steady-state.

A similar principle applies to capacitors:

2. Capacitor steady-state charge balance

Integration of the relation $i_c = C\frac{dv_c}{dt}$ over one switching interval yields

$$v_c(T_s) - v_c(0) = \frac{1}{C}\int_0^{T_s} i_c(t)\,dt$$

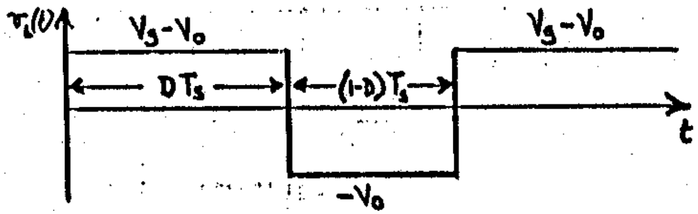
In steady-state, we must have $v_c(T_s) = v_c(0)$.

Hence, in steady-state,

$$0 = \frac{1}{T_s}\int_0^{T_s} i_c(t)\,dt = \text{average capacitor current}$$

The capacitor current must have zero average (no dc component).

These principles may be used to find the steady-state voltages and currents in any switched-mode converter. For the buck converter example, the inductor voltage waveform is



Therefore, $\langle v_L(t)\rangle = D(V_g - V_o) + (1-D)(-V_o) = 0$

solve for V_o: $DV_g = DV_o + (1-D)V_o = V_o$

$\Rightarrow V_o = DV_g$

Summary of techniques for steady-state analysis of switched-mode converters

1. Linear Ripple Approximation

$$\begin{pmatrix}\text{ripple components} \\ \Delta i_L,\ \Delta v_c\end{pmatrix} \ll \begin{pmatrix}\text{dc components} \\ I_o,\ V_o\end{pmatrix}$$

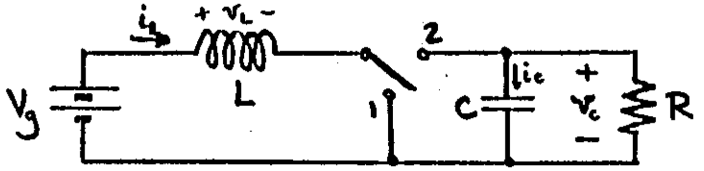
$\Rightarrow$ inductor current $\mid$ $i_L \approx I_o$
capacitor voltage $\mid$ $v_c \approx V_o$

2. Inductor volt-sec balance
average inductor voltage $= 0$

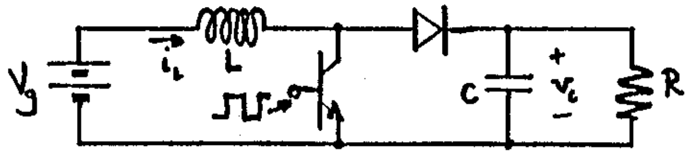
3. Capacitor charge balance
average capacitor current $= 0$

Boost Converter Example

The boost converter is another well-known switched-mode converter:



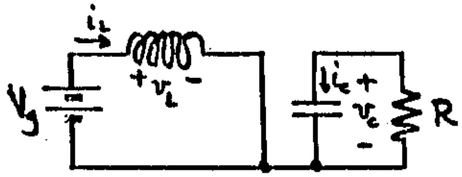
Practical realization of switch using transistor and diode:



This converter produces an output voltage greater in magnitude than the input voltage.

Switch in position 1

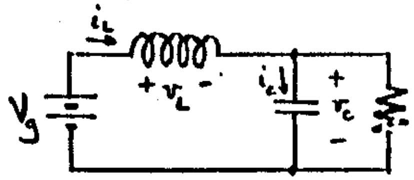
$(0 \le t \le DT_s)$



$$v_L = V_g$$
$$i_c = -v_c/R$$

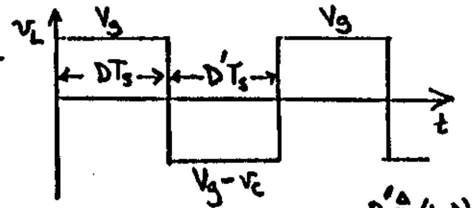
Switch in position 2

$(0 \le t \le (1-D)T_s)$



$$v_L = V_g - v_c$$
$$i_c = i_L - v_c/R$$

inductor voltage

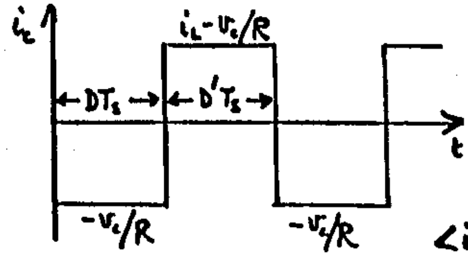


$D' \triangleq (1-D)$

Inductor volt-sec balance:

$$\langle v_L \rangle = \underset{=0}{D V_g + D'(V_g - v_c)}$$
$$\Rightarrow D' v_c = \underbrace{(D+D')}_{1} V_g$$
$$\boxed{v_c = \frac{1}{D'} V_g}$$

capacitor current

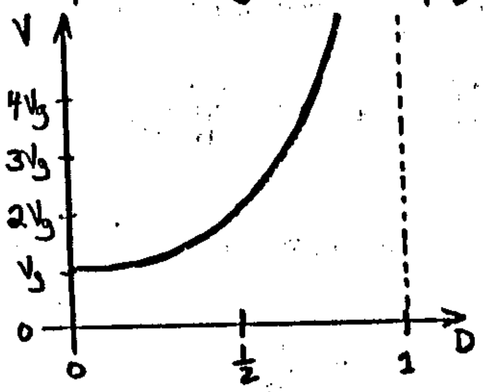


Capacitor charge balance:

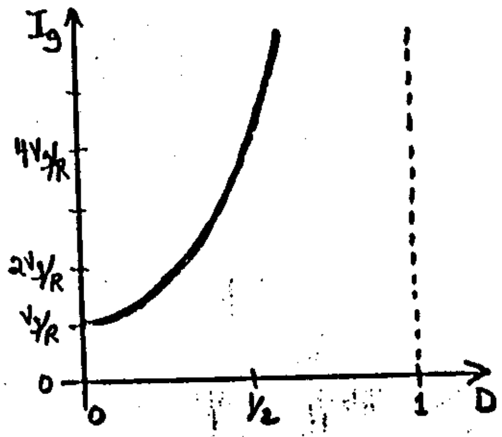
$$\langle i_c \rangle \underset{=0}{=} D(-v_c/R) + D'(i_L - v_c/R)$$
$$\Rightarrow D' i_L = (D+D')\frac{v_c}{R} = v_c/R$$
$$\boxed{i_L = \frac{v_c}{D'R}}$$

Boost Converter – Equilibrium Relations

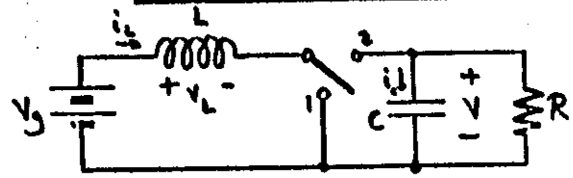
Output Voltage $V = v_C = \frac{1}{1-D} V_g$



Input Current $I_g = i_L = \frac{1}{1-D}\frac{V}{R} = \frac{1}{(1-D)^2}\frac{V_g}{R}$



Boost Converter – inductor current ripple



switch in position 1

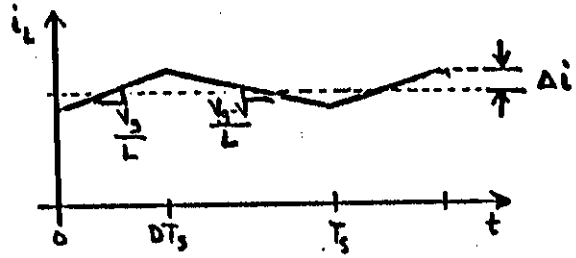
$$v_L = L\frac{di_L}{dt} = V_g$$

$$\Rightarrow \frac{di_L}{dt} = \frac{V_g}{L}$$

switch in position 2

$$v_L = L\frac{di_L}{dt} = V_g - V$$

$$\Rightarrow \frac{di_L}{dt} = \frac{V_g - V}{L}$$



$$2\,\Delta i = DT_s \frac{V_g}{L} \Rightarrow \Delta i = \frac{DT_s V_g}{2L}$$

capacitor voltage ripple

switch in position 1

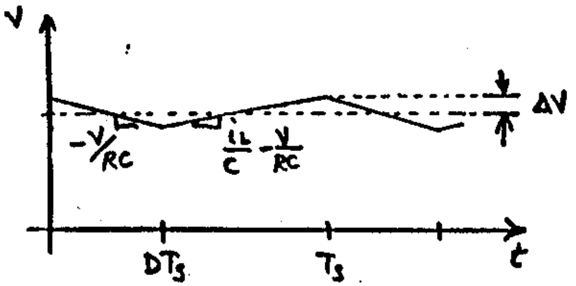
$$C\frac{dv}{dt} = i_c = -V/R$$

$$\Rightarrow \frac{dv}{dt} = -\frac{V}{RC}$$

switch in position 2

$$C\frac{dv}{dt} = i_c = i_L - V/R$$

$$\Rightarrow \frac{dv}{dt} = \frac{i_L}{C} - \frac{V}{RC}$$

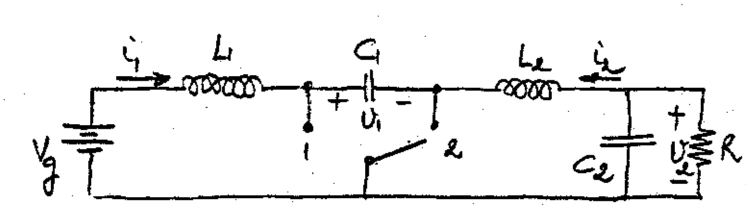


$$2\Delta V = DT_s \frac{V}{RC} \Rightarrow \Delta V = \frac{DT_s V}{2RC}$$

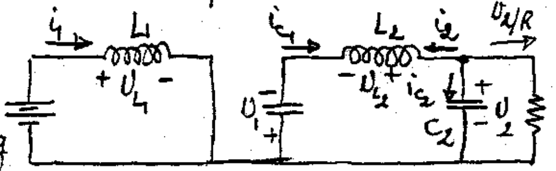
These expressions for Δi and ΔV can be used to choose L and C such that the voltage and current ripples are sufficiently small.

2-17

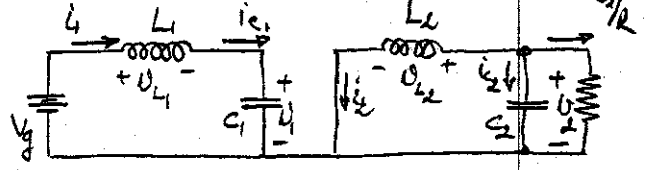
Example: 'Cuk Converter (Continuous Conduction)



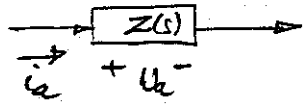
Switch in position 1



Switch in position 2



Note: must define voltages consistently with currents:



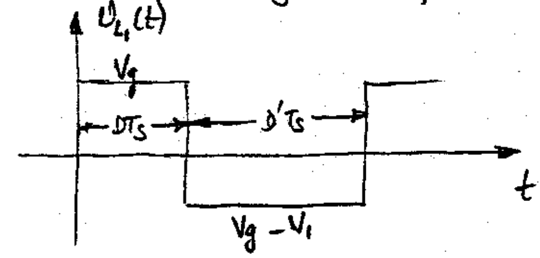
$v_a(s) = Z(s)\, i_a(s)$

$v_{L_1} = V_g$ $\qquad$ $v_{L_2} = v_{c_1} + v_{c_2} \simeq V_1 + V_2$ $\qquad$ $v_{L_1} = V_g - v_1 \simeq V_g - V_1$ $\qquad$ $v_{L_2} = v_2 \simeq V_2$

$i_{c_1} = -i_2 \simeq -I_2$ $\qquad$ (linear ripple approximation) $\qquad$ $i_{c_1} = i_1 \simeq I_1$ $\qquad$ $i_{c_2} = -i_2 - \frac{v_2}{R} \simeq I_2 - \frac{V_2}{R}$

$i_{c_2} = -i_2 - \frac{v_2}{R} \simeq -I_2 - \frac{V_2}{R}$

Inductor Voltage waveform



T_s = switching period

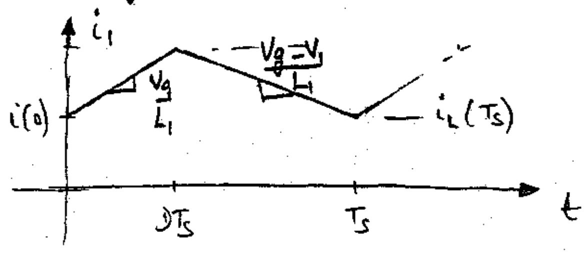
D = duty ratio, $0 \leq D \leq 1$

$D' \simeq 1 - D$, $\quad D + D' = 1$

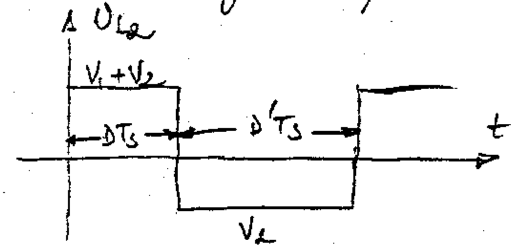
Volt-sec balance on L_1:

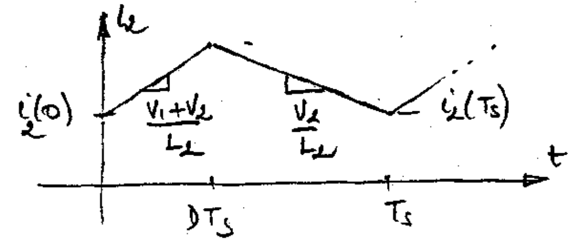
$$DV_g + D'(V_g - V_1) = 0$$

$$V_g(D + D') - D'V_1 = 0 \quad \Rightarrow \quad V_1 = \frac{V_g}{D'}$$



Inductor Voltage waveform





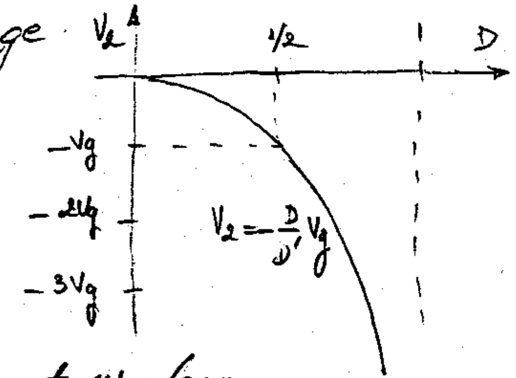
Voltage-sec balance on L_2:

$$D(V_1+V_2) + D'(V_2) = 0$$

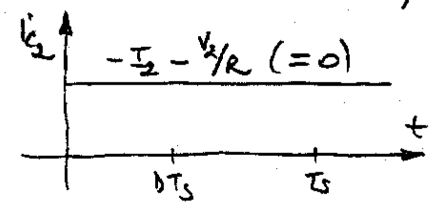
$$V_1(D) + V_2(\cancel{D+D'}) = 0$$

$$\Rightarrow \quad V_2 = -DV_1 = -\frac{D}{D'}V_g$$

Output voltage



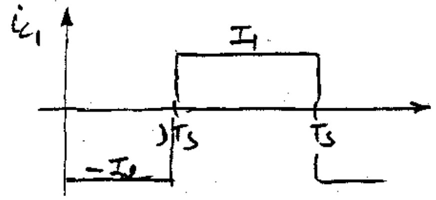
Capacitor current waveform



Same during DT_s and $D'T_s$.

$$\langle i_{C2} \rangle = -I_2 - \frac{V_2}{R} = 0$$

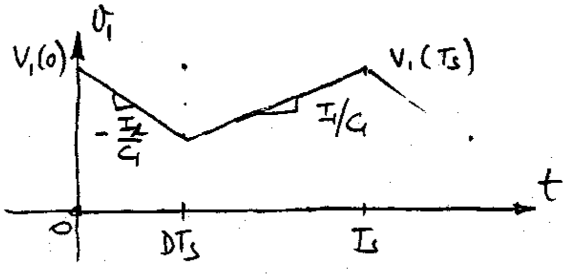
$$\Rightarrow I_2 = -\frac{V_2}{R} = \frac{D}{D'}\frac{V_g}{R}$$



charge balance on C_1:

$$D(-I_2) + D'(I_1) = 0$$

$$I_1 = \frac{D}{D'}I_2 = \left(\frac{D}{D'}\right)^2\frac{V_g}{R}$$



R. TYMERSKI

STATE - SPACE REPRESENTATION OF SYSTEMS

DEFINITIONS:

THE STATE OF A SYSTEM AT TIME t_0 INCLUDES THE MINIMUM INFORMATION NECESSARY TO SPECIFY COMPLETELY THE CONDITION OF THE SYSTEM AT TIME t_0 AND ALLOW DETERMINATION OF ALL SYSTEM OUTPUTS AT TIME $t > t_0$ WHEN INPUTS UP TO TIME t ARE SPECIFIED.

IN A LINEAR, TIME-INVARIANT ELECTRICAL NETWORK, FOR EXAMPLE, KNOWLEDGE OF ALL CAPACITOR VOLTAGES AND INDUCTOR CURRENTS UNIQUELY SPECIFIES THE NETWORK CONDITION AT ANY PARTICULAR TIME.

THUS THE STATE OF A SYSTEM AT TIME t_0 IS SIMPLY THE SET OF VALUES, AT TIME t_0, OF APPROPRIATELY CHOSEN SET OF STATE VARIABLES, USUALLY DENOTED AS $x_1, x_2, \ldots, x_n$ WHERE n IS THE ORDER OF THE SYSTEM.

WE CAN THINK OF AN n-DIMENSIONAL SPACE IN WHICH EACH COORDINATE IS DEFINED BY ONE OF THE STATE VARIABLES, x_i, $i = 1, \ldots, n$. THIS SPACE IS CALLED THE STATE SPACE.

THE STATE VARIABLES MAY BE ARRANGED IN AN COLUMN n-VECTOR $x = [x_1, x_2, \ldots, x_n]^T$.

FOR A GIVEN SYSTEM OF n-th ORDER A SET OF n FIRST ORDER DIFFERENTIAL EQUATIONS MAY BE WRITTEN. THIS SET MAY BE ARRANGED IN MATRIX FORM AS FOLLOWS FOR A SYSTEM WITH m INPUTS u_i, $i = 1, \ldots, m$ AND p OUTPUTS y_i, $i = 1, \ldots, p$.

$$\dot{x} = Ax + Bu \qquad (1)$$

$$y = Cx + Du \qquad (2)$$

WHERE

$$x = \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{bmatrix}, \quad u = \begin{bmatrix} u_1 \\ u_2 \\ \vdots \\ u_m \end{bmatrix}, \quad y = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_p \end{bmatrix}$$

AND

$$A \in R^{n \times n}, \quad B \in R^{n \times m},$$

$$C \in R^{p \times n}, \quad D \in R^{p \times m}$$

EQUATIONS (1) ARE KNOWN AS THE STATE EQUATIONS
EQUATIONS (2) ARE THE OUTPUT EQUATIONS.

THE SOLUTION OF (1) CAN BE SHOWN TO BE

$$x(t) = e^{A(t-t_0)} x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)} B u(\tau)\, d\tau \qquad (3)$$

THE OUTPUT $y(t)$ FOLLOWS DIRECTLY FROM (3) AND (2).

THE MATRIX e^{At} IN (3) IS KNOWN AS THE STATE TRANSITION MATRIX AND MAY BE EXPRESSED AS AN INFINITE TAYLOR SERIES.

$$e^{At} = I + At + \frac{A^2t^2}{2!} + \frac{A^3t^3}{3!} + \dots \qquad (4)$$

WHERE I IS AN $n \times n$ IDENTITY MATRIX.

STATE - SPACE FORMULATION APPLIED TO SWITCHED - MODE DC - TO - DC CONVERTERS

DURING EACH POSITION OF THE SWITCH IN PWM CONVERTERS A LINEAR TIME INVARIANT NETWORK IS OBTAINED WHICH FOR A SINGLE INPUT (THE SOURCE VOLTAGE) WE MAY WRITE THE STATE EQUATIONS AS :

$$\dot{x} = A_i x + b_i V_g \quad , \quad i = 1, 2 \qquad (5)$$

WHICH BY (3) LEADS TO

$$x(t) = e^{A_i(t - t_j)} x(t_j) + \int_{t_j}^{t} e^{A_i(t-\tau)} d\tau \; b_i V_g \; ; \; i = 1, 2 \qquad (6)$$

WHERE V_g IS ASSUMED CONSTANT, t_j IS THE INITIAL TIME.

$\Rightarrow$

$$x(t) = e^{A_i(t - t_j)} x(t_j) + A_i^{-1}\left[e^{A_i(t - t_j)} - I \right] b_i V_g \qquad (7)$$

PROVIDED A_i^{-1}, $i = 1, 2$ EXIST.

APPENDIX

SOLUTION OF THE STATE EQUATIONS

$$\dot{x}(t) = A\,x(t) + B\,u(t) \qquad (1)$$

$$y(t) = Cx(t) + Du(t) \qquad (2)$$

METHOD 1:

Rewrite (1) as

$$\dot{x}(t) - Ax(t) = Bu(t)$$

Premultiply both sides by e^{-At} $\Rightarrow$

$$e^{-At}\,\dot{x}(t) - e^{-At}\,A\,x(t) = e^{-At}\,Bu(t)$$

The left-hand side can be expressed as

$$\frac{d}{dt}\left[e^{-At}\,x(t)\right] = e^{-At}\,Bu(t)$$

Upon integration we conclude that

$$e^{-At}x(t) - e^{-At_0}x(t_0) = \int_{t_0}^{t} e^{-A\tau}\,Bu(\tau)\,d\tau$$

$$\Rightarrow \quad x(t) = e^{A(t-t_0)}x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)}\,Bu(\tau)\,d\tau \qquad (3)$$

substituting (3) into (2) $\Rightarrow$

$$y(t) = Ce^{A(t-t_0)}x(t_0) + \int_{t_0}^{t} Ce^{A(t-\tau)}\,Bu(\tau)\,d\tau + Du(t) \qquad (4)$$

METHOD 2 : Using Laplace Transform

Let us first consider the equation

$$\dot{x} = Ax \qquad (5)$$

which is (1) with $u(t) = 0$.

Taking the $\mathcal{L}$ - transform of (5),

$$sX(s) - x(0) = AX(s)$$

$$\Rightarrow \quad X(s) = (sI - A)^{-1} x(0) \qquad (6)$$

The time response can be found by taking the inverse $\mathcal{L}$ - tranform of (6). This is done as follows. Consider

$$(sI - A)^{-1} = \frac{1}{s}\left(I - \frac{1}{s}A\right)^{-1} \qquad (7)$$

Using the fact that

$$\frac{1}{1-x} = 1 + x + x^2 + \dots \quad \text{for } |x| < 1$$

we can expand the right hand side of (7) so that

$$(sI-A)^{-1} = \frac{1}{s}\left[I + \frac{1}{s}A + \frac{1}{s^2}A^2 + \frac{1}{s^3}A^3 + \dots \right]$$

$$= \frac{1}{s}I + \frac{1}{s^2}A + \frac{1}{s^3}A^2 + \frac{1}{s^4}A^3 + \dots \quad \text{for } |s| \text{ large enough} \qquad (8)$$

Recalling that $\mathcal{L}^{-1}\left\{\frac{1}{s^{n+1}}\right\} = \frac{t^n}{n!} 1(t)$

where $1(t)$ is the unit step function.
We can invert (8) to obtain

$$\mathcal{L}^{-1}\left\{(sI-A)^{-1}\right\} = \left[I + At + A^2\frac{t^2}{2!} + A^3\frac{t^3}{3!} + \dots \right] 1(t)$$

$$= \sum_{i=0}^{\infty} \frac{(At)^i}{i!} \, 1(t)$$

$$= e^{At} \, 1(t) \qquad (9)$$

where we define $\quad e^{At} \triangleq \sum_{i=0}^{\infty} \frac{(At)^i}{i}$

Hence the solution of (5) using (6) and (9) is

$$x(t) = e^{At} x(0), \qquad t > 0$$

Now let us find the solution of (1).
Taking the $\mathcal{L}$-transform of (1) gives

$$s\,X(s) - x(0) = A\,X(s) + B\,U(s)$$

$$\Rightarrow \quad X(s) = (sI-A)^{-1} x(0) + (sI-A)^{-1} B\,U(s)$$

we know from (9) that

$$\mathcal{L}^{-1}\left\{(sI-A)^{-1}\right\} = e^{At} \, 1(t)$$

To invent $(sI - A)^{-1} B U(s)$ we use the fact that

$$\mathcal{L}^{-1}\left\{F_1(s)\, F_2(s)\right\} = \int_0^t f_1(t-\tau)\, f_2(\tau)\, d\tau$$

and therefore

$$\mathcal{L}^{-1}\left\{(sI-A)^{-1} B U(s)\right\} = \int_0^t e^{A(t-\tau)} B u(\tau)\, d\tau$$

hence the solution of (1) is

$$x(t) = e^{At} x(0) + \int_0^t e^{A(t-\tau)} B u(\tau)\, d\tau$$

changing the time origin to "t_0" $\Rightarrow$

$$x(t) = e^{A(t-t_0)} x(t_0) + \int_{t_0}^t e^{A(t-\tau)} B u(\tau)\, d\tau$$

which is the same as (3) found by the previous method.

Equation (4) follows as before.

Appendix:

Review of the state-space Description of Linear Time-Invariant Systems.

1. How to write State equations.

The state equations which describe the behavior of any linear electrical network may be written in the form

$$\frac{d\underline{x}(t)}{dt} = A\,\underline{x}(t) + B\underline{u}(t) \qquad (1)$$
$$\underline{y}(t) = C\,\underline{x}(t) + E\,\underline{u}(t)$$

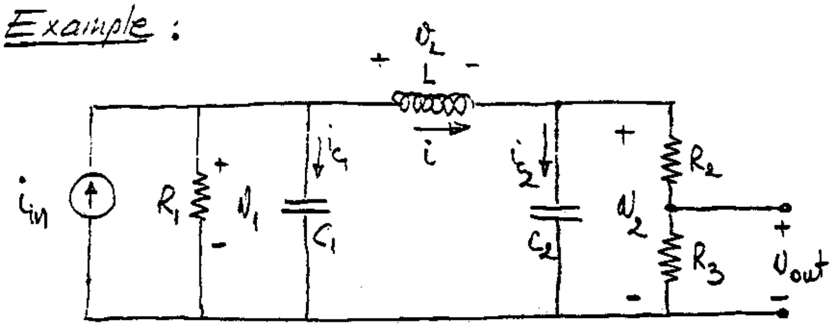
where

$\underline{x}(t)$ = State vector (Contain inductor currents, capacitor voltages, ect.)

$\underline{y}(t)$ = output vector

$\underline{u}(t)$: input vector

Example :



System states are v_1 , v_2 , i

input i_{in} ; output v_{out}

So define $\underline{x}(t) = \begin{bmatrix} v_1 \\ v_2 \\ i \end{bmatrix}$; $\underline{y}(t) = [v_{out}]$

$\underline{u}(t) = [i_{in}]$

State equations:

$$i_{C_1} = C_1 \frac{dv_1}{dt} = i_{in} - \frac{v_1}{R_1} - i$$

$$\Rightarrow \frac{dv_1}{dt} = \frac{i_{in}}{C_1} - \frac{v_1}{R_1 C_1} - \frac{i}{C_1}$$

$$i_{C_2} = C_2 \frac{dv_2}{dt} = i - \frac{v_2}{R_2 + R_3}$$

$$\Rightarrow \frac{dv_2}{dt} = \frac{i}{C_2} - \frac{v_2}{(R_2+R_3)C_2}$$

$$v_L = L \frac{di}{dt} = v_1 - v_2$$

$$\Rightarrow \frac{di}{dt} = \frac{v_1}{L} - \frac{v_2}{L}$$

So we have

$$\underbrace{\frac{d}{dt}\begin{bmatrix} v_1 \\ v_2 \\ i \end{bmatrix}}_{\frac{d\underline{x}}{dt}} = \underbrace{\begin{bmatrix} -\frac{1}{R_1C_1} & 0 & -\frac{1}{C_1} \\ 0 & \frac{-1}{(R_2+R_3)C_2} & \frac{1}{C_2} \\ \frac{1}{L} & -\frac{1}{L} & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} v_1 \\ v_2 \\ i \end{bmatrix}}_{\underline{x}} + \underbrace{\begin{bmatrix} \frac{1}{C_1} \\ 0 \\ 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} i_{in} \end{bmatrix}}_{\underline{u}}$$

<u>Output relation</u>: must express the output v_{out} in terms of the system states v_1, v_2, i and the input i_{in} to obtain the form prescribe in eq (1)

$$v_{out} = v_2 \cdot \frac{R_3}{R_2+R_3}$$

$$\Rightarrow \underbrace{[\, v_{out} \,]}_{\underline{y}} = \underbrace{\begin{bmatrix} 0 & \frac{R_3}{R_2+R_3} & 0 \end{bmatrix}}_{C} \underbrace{\begin{bmatrix} v_1 \\ v_2 \\ i \end{bmatrix}}_{\underline{x}} + \underbrace{[0]}_{E} \underbrace{[\, i_{in} \,]}_{\underline{u}}$$

APPENDIX:

EVALUATING THE CONVOLUTION INTEGRAL IN THE SOLUTION OF THE STATE EQUATIONS

$$x(t) = e^{A(t-t_0)}\,x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)}\,B\,u(\tau)\,d\tau \qquad (1)$$

IF WE ASSUME THE INPUT IS CONSTANT WE CAN SIMPLIFY (1).

$\therefore$ FOR $u(\tau) = u$, a constant

$\Rightarrow$

$$x(t) = e^{A(t-t_0)}\,x(t_0) + e^{At}\int_{t_0}^{t} e^{-A\tau}\,d\tau\,Bu \qquad (2)$$

Now

$$\int_{t_0}^{t} e^{-A\tau}\,d\tau = \int_{t_0}^{t}\left(I - A\tau + \frac{A^2\tau^2}{2!} - \frac{A^3\tau^3}{3!} + \cdots\right)d\tau$$

$$= \left[\tau I - \frac{A\tau^2}{2!} + \frac{A^2\tau^3}{3!} - \frac{A^3\tau^4}{4!} + \cdots\right]_{t_0}^{t}$$

$$= \underbrace{A^{-1}A}_{I}\left[\tau I - \frac{A\tau^2}{2!} + \frac{A^2\tau^3}{3!} - \frac{A^3\tau^4}{4!} + \cdots\right]_{t_0}^{t}, \text{ provided } A^{-1} \text{ exists}$$

$$= A^{-1}\left[A\tau - \frac{A^2\tau^2}{2!} + \frac{A^3\tau^3}{3!} - \frac{A^4\tau^4}{4!} + \cdots\right]_{t_0}^{t}$$

$$= -A^{-1}\left[e^{-A\tau} - I\right]_{t_0}^{t}$$

$$= -A^{-1}\left[\left(e^{-At} - I\right) - \left(e^{-At_0} - I\right)\right]$$

$$= -A^{-1}\left[e^{-At} - e^{-At_0}\right]$$

$$= A^{-1} e^{-At}\left[e^{A(t-t_0)} - I\right] \qquad (3)$$

(3) + (2) $\Rightarrow$

$$x(t) = e^{A(t-t_0)}\, x(t_0) + A^{-1}\left[e^{A(t-t_0)} - I\right] B u$$

Note that A and e^{At} are COMMUTATIVE

i.e. $A e^{At} = e^{At} A$

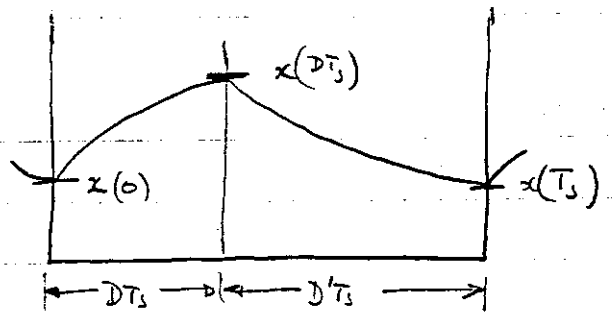
since

$$A\left[I + At + \frac{A^2t^2}{2!} + \dots\right] = \left[I + At + \frac{A^2t^2}{2!} + \dots\right] A$$

R. TYMERSKI (1)

STEADY-STATE ANALYSIS OF PWM CONVERTERS

WE CAN DETERMINE THE STATE TRAJECTORY BY USING THE SOLUTION OF THE STATE EQUATIONS FOR EACH SUBINTERVAL OF OPERATION. THIS WILL LEAD TO THE SOLUTION OF THE PERIODIC STEADY-STATE.



THE SOLUTION OF THE STATE EQUATIONS FOR EACH SUBINTERVAL $i = 1, 2$ IS

$$x(t) = \phi_i \, x(t_j) + \psi_i V_g \; ; \quad i = 1,2 \qquad (1)$$

WHERE V_g IS THE INPUT VOLTAGE WHICH IS ASSUMED TO BE CONSTANT AND, t_j IS THE INITIAL TIME, AND

$$\phi_i = e^{A_i(t-t_j)}$$

$$\psi_i = A_i^{-1}\left[e^{A_i(t-t_j)} - I \right] b_i \; ; \text{ PROVIDED } A_i^{-1} \text{ EXISTS}, \; i=1,2$$

THE VALUE OF THE STATE AT THE END OF THE FIRST SUBINTERVAL IS RELATED TO ITS VALUE AT THE BEGINNING AS FOLLOWS (USING (1))

$$x(DT_s) = \phi_1 \, x(0) + \psi_1 V_g \qquad (2)$$

SIMILARLY, FOR THE SECOND SUBINTERVAL (AGAIN USING (1))

$$x(T_s) = \phi_2 \; x(DT_s) + \psi_2 V_g \qquad (3)$$

SUBSTITUTING (2) INTO (3) GIVES

$$x(T_s) = \phi_2 \left[\phi_1 x(0) + \psi_1 V_g \right] + \psi_2 V_g$$

$$x(T_s) = \phi_2 \phi_1 \; x(0) + \left(\phi_2 \psi_1 + \psi_2 \right) V_g \qquad (4)$$

NOW FOR STEADY STATE OPERATION WE HAVE

$$x(T_s) = x(0) \qquad (5)$$

WHICH USING (4) $\Rightarrow$

$$\boxed{x(0) = \left(\mathbf{I} - \phi_2 \phi_1 \right)^{-1} \left(\phi_2 \psi_1 + \psi_2 \right) V_g} \qquad (6)$$

WE CAN DETERMINE $x(DT_s)$ BY SUBSTITUTING (6) INTO (2). ALTERNATIVELY, WE CAN USE (5) AND SUBSTITUTE (3) INTO (2) WHICH GIVES

$$x(DT_s) = \phi_1 \left[\phi_2 \; x(DT_s) + \psi_2 V_g \right] + \psi_1 V_g$$

$$x(DT_s) = \phi_1 \phi_2 \; x(DT_s) + \left(\phi_1 \psi_2 + \psi_1 \right) V_g$$

$$\Rightarrow \quad \boxed{x(DT_s) = \left(I - \phi_1 \phi_2 \right)^{-1} \left(\phi_1 \psi_2 + \psi_1 \right) V_g} \qquad (7)$$

THE STATE RIPPLE Δx WHERE

$$\Delta x \triangleq x(DT_s) - x(0) \qquad (8)$$

CAN NOW BE DETERMINED USING (6) AND (7).

SIMPLIFICATIONS

IN POWER ELECTRONICS THE USE OF SIMPLIFIED RESULTS IS OFTEN DESIRED SO THAT CALCULATIONS MAY BE QUICKLY DONE BY HAND. THE ABOVE RESULTS MAY BE SIMPLIFIED BY USING THE "LINEAR RIPPLE APPROXIMATION". THIS APPROXIMATION HAS ITS ORIGINS IN NOTING THAT MOST WAVEFORMS IN WELL DESIGNED PWM CONVERTERS ARE COMPOSED OF LINEAR SEGMENTS. THIS IMPACTS IN THE ANALYSIS MATHEMATICS BY LETTING THE EXPONENTIAL MATRIX BE APPROXIMATED BY LINEAR TERMS ONLY; SO THAT

$$\phi_i = e^{A_i(t-t_j)} \approx I + A_i(t-t_j) \qquad (9)$$

$$\Rightarrow \quad \phi_1 = I + DA_1T_s \qquad (10A)$$
$$\phi_2 = I + D'A_2T_s \qquad (10B)$$

THIS REDUCES ψ_i TO

$$\psi_i = (t-t_j)\,b_i \qquad (11)$$

$$\Rightarrow \quad \psi_1 = D\,b_1T_s \qquad (12A)$$
$$\psi_2 = D'\,b_2T_s \qquad (12B)$$

SUBSTITUTING (10) AND (12) INTO (6) GIVES

$$x(0) \approx \left(I - (I + D'A_2T_s)(I + DA_1T_s)\right)^{-1}\left[(I + D'A_2T_s)\, Db_1T_s + D'b_2T_s\right]V_g$$

$$= -\left(DA_1 + D'A_2 + A_2A_1D'DT_s\right)^{-1}\frac{1}{T_s}\; T_s\left[Db_1 + D'b_2 + A_2b_1D'DT_s\right]V_g$$

FOR $\|DA_1 + D'A_2\| \gg \|A_2A_1D'DT_s\|$

AND

$\|Db_1 + D'b_2\| \gg \|A_2b_1D'DT_s\|$ WHERE $\|\cdot\|$ DENOTES A MATRIX NORM

IN WHICH CASE WE NEGLECT ALL TERMS OF ORDER T_s, WE HAVE

$$\boxed{\begin{aligned} x(0) &= -A^{-1}b\,V_g \\ \text{WHERE}\quad A &= DA_1 + D'A_2 \\ b &= Db_1 + D'b_2 \end{aligned}} \qquad (13)$$

A AND b MAY BE CONSIDERED TO BE "AVERAGED" MATRICES.

LET US NOW APPLY THE "LINEAR RIPPLE APPROXIMATION" TO FIND A SIMPLIFIED EXPRESSION $x(DT_s)$.

SUBSTITUTING (10) AND (12) INTO (7) GIVES

$$x(DT_s) \approx \left(I - (I + DA_1T_s)(I + D'A_2T_s)\right)^{-1}\left[(I + DA_1T_s)\, D'b_2T_s + Db_1T_s\right]V_g$$

$$= -\left(DA_1 + D'A_2 + A_1A_2DD'T_S\right)^{-1} \frac{1}{T_S} \; T_S\left[Db_1 + D'b_2 + A_1b_2DD'T_S\right] V_g$$

FOR $\left\| DA_1 + D'A_2 \right\| \gg \left\| A_1A_2DD'T_S \right\|$

AND

$$\left\| Db_1 + D'b_2 \right\| \gg \left\| A_1b_2DD'T_S \right\|$$

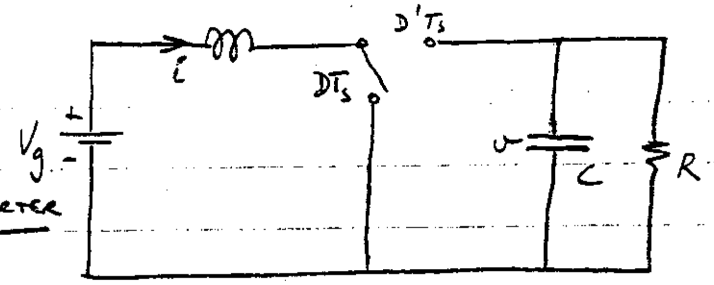
WHERE THE TERMS ON THE RIGHT HAND SIDE OF THE INEQUALITIES REPRESENT TERMS OF ORDER T_S, WHICH WE WILL NEGLECT, WE HAVE

$$\boxed{\begin{gathered} x(DT_S) = x(0) = X = -A^{-1} b V_g \\ \text{WHERE} \quad A = DA_1 + D'A_2 \\ b = Db_1 + D'b_2 \end{gathered}} \qquad (14)$$

WE SEE THAT BY NEGLECTING ALL TERMS OF ORDER T_S, THE STATE RIPPLE HAS BEEN NULLED SINCE $x(DT_S) = x(0)$. THE STATE DETERMINED BY (14) (and also (13)) WILL BE DENOTED X AND IT IS THE "STATE-SPACE AVERAGING" RESULT FOR THE STEADY STATE VECTOR.

EXAMPLE :

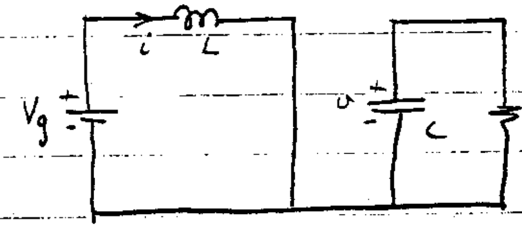
DETERMINE THE STEADY STATE VECTOR FOR THE BOOST CONVERTER SHOWN BELOW.



BOOST CONVERTER

SOLUTION : DETERMINE THE STATE MATRICES

DURING DT_s

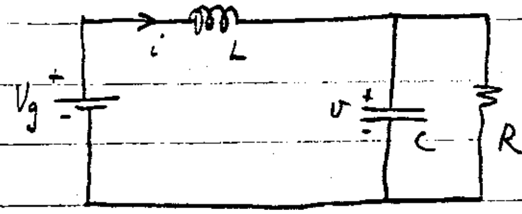


$$-V_g + L\frac{di}{dt} = 0 \Rightarrow \frac{di}{dt} = +\frac{V_g}{L}$$

$$0 = C\frac{dv}{dt} + \frac{v}{R} \Rightarrow \frac{dv}{dt} = \frac{-v}{RC}$$

$$\Rightarrow \begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}}_{A_1} \begin{bmatrix} i \\ v \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{b_1} V_g$$

DURING $D'T_s$



$$-V_g + L\frac{di}{dt} + v = 0 \Rightarrow \frac{di}{dt} = \frac{-v}{L} + \frac{V_g}{L}$$

$$i = C\frac{dv}{dt} + \frac{v}{R} \Rightarrow \frac{dv}{dt} = \frac{i}{C} - \frac{v}{RC}$$

$$\Rightarrow \begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}}_{A_2} \begin{bmatrix} i \\ v \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{b_2} V_g$$

WE NOW FORM THE AVERAGED MATRICES

$$A = DA_1 + D'A_2$$

$$\Rightarrow \quad A = \begin{bmatrix} 0 & -\frac{D'}{L} \\ \frac{D'}{C} & -\frac{1}{RC} \end{bmatrix}$$

AND $\quad b = Db_1 + D'b_2$

$$\Rightarrow \quad b = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

USING (14) WE HAVE

$$X = -A^{-1} b V_g$$

$$= -\begin{bmatrix} 0 & \frac{-D'}{L} \\ \frac{D'}{C} & -\frac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_g$$

$$= -\frac{LC}{D'^2} \begin{bmatrix} -\frac{1}{RC} & \frac{D'}{L} \\ -\frac{D'}{C} & 0 \end{bmatrix} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_g = -\frac{LC}{D'^2} \begin{bmatrix} -\frac{1}{RLC} \\ -\frac{D'}{LC} \end{bmatrix} V_g$$

$$\Rightarrow \quad X = \begin{bmatrix} I \\ V \end{bmatrix} = \begin{bmatrix} \frac{V_g}{RD'^2} \\ \frac{V_g}{D'} \end{bmatrix} \quad (15)$$

WHICH IS THE SAME RESULT AS THAT OBTAINED USING VOLT-SEC BALANCE ON THE INDUCTOR AND AMP-SEC BALANCE ON THE CAPACITOR.

THE ADVANTAGE OF THE SIMPLIFIED EXPRESSIONS, IS THAT WE HAVE ANALYTICAL (I.E. SYMBOLIC) EXPRESSIONS FOR THE STEADY STATE VECTOR X, (SUCH AS THAT OF (15) FOR THE BOOST CONVERTER), WHICH CONVEY MORE DESIGN RELATED INFORMATION THAN THAT GIVEN BY THE EXACT EXPRESSIONS (6) and (7).

EPILOGUE

IN ESSENSE WHAT STATE SPACE AVERAGING DOES IS TO REPLACE THE ACTUAL PIECEWISE LINEAR SYSTEM DESCRIBED BY

$$\begin{aligned} \dot{x} &= A_1 x + b_1 V_g, \quad kT_s \leq t \leq (k+d)T_s \\ \dot{x} &= A_2 x + b_2 V_g, \quad (k+d)T_s \leq t \leq (k+1)T_s \end{aligned} \tag{16}$$

WHERE k IS THE CYCLE NUMBER.

BY THE "AVERAGED" SYSTEM

$$\dot{x} = A x + b V_g \qquad \forall t \tag{17}$$

WHERE $A = dA_1 + d'A_2$

$b = db_1 + d'b_2$

THE STEADY STATE SOLUTION FOR THE AVERAGED SYSTEM IS GIVEN BY REALIZING THAT IN STEADY STATE

$$\dot{x} = 0$$

$$\Rightarrow \qquad 0 = AX + GV_g$$

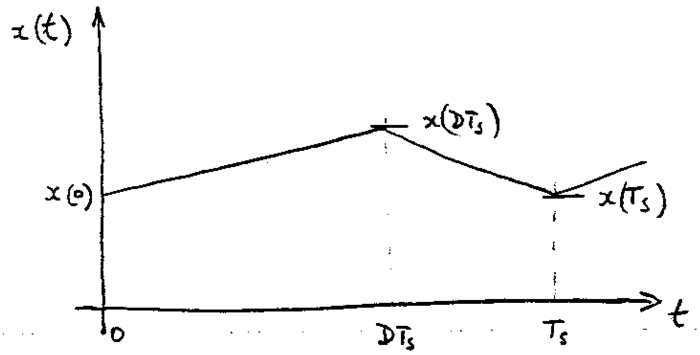
$$\Rightarrow \qquad X = -A^{-1}GV_g$$

WHICH IS THE SAME RESULT AS PREVIOUSLY GIVEN IN (14)

LECTURE: RIPPLE ANALYSIS

LINEAR RIPPLE EVALUATION USING STATE SPACE MATRICES

WITH THE LINEAR RIPPLE APPROXIMATION THE STATE EVOLUTION MAY BE SEEN AS BELOW



FOR WELL DESIGNED PWM CONVERTERS THE LINEAR RIPPLE APPROXIMATION IS QUITE GOOD.

FROM THE ABOVE FIGURE WE CAN SEE THAT THE STATE RIPPLE Δx IS GIVEN BY

$$\Delta x = x(DT) - x(0) \qquad (17)$$

WHICH BY (9) $\Rightarrow$

$$\Delta x \approx \left[A_1 x(0) + b_1 V_g\right] DT_s \qquad (18)$$

WE CAN APPRECIATE THE FORM OF (18) IN THAT THE SLOPE DURING $0 < t < DT_s$ IS

$\dot{x}(t) = Ax(t) + bV_g$. IN (18) WE SEE WE EVALUATE THIS EXPRESSION AT $t = 0$, THE START OF THE INTERVAL. WE EVALUATE $x(0)$ BY USE OF (16).

SUMMARIZING:

THE STATE RIPPLE Δx IS GIVEN BY

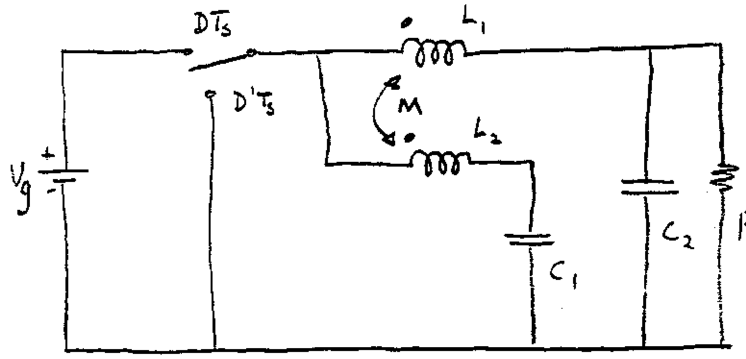
$$\Delta x = \left[A_1 x(0) + b_1 V_g\right] DT_s$$

WHERE $x(0) = -A^{-1} b V_g$

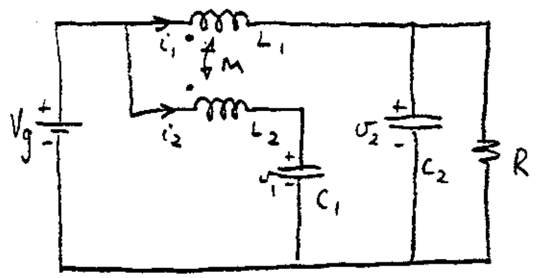
WHERE

$$A = DA_1 + D'A_2$$
$$b = Db_1 + D'b_2$$

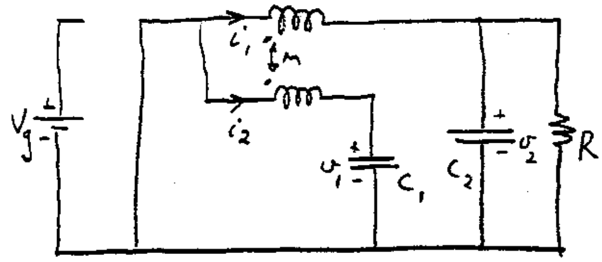
EXAMPLE : BUCK CONVERTER WITH COUPLED WINDING



DURING DT_s



DURING $D'T_s$



LET THE STATES BE INDUCTOR CURRENTS AND CAPACITOR VOLTAGES.

STATE EQUATIONS

$$L_1 \dot{i}_1 + M \dot{i}_2 = V_g - v_2 \qquad (1A)$$

$$M \dot{i}_1 + L_2 \dot{i}_2 = V_g - v_1 \qquad (1B)$$

$$i_2 = C_1 \dot{v}_1 \qquad (1C)$$

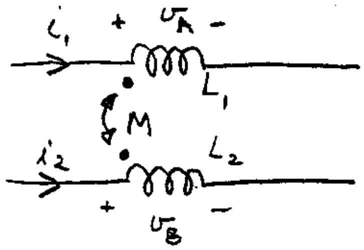
$$i_1 = C_2 \dot{v}_2 + \frac{v_2}{R} \qquad (1D)$$

STATE EQUATIONS

THE SAME EXCEPT $V_g = 0$

WHERE $\dot{i}_1 = \dfrac{di_1}{dt}$; $\dot{i}_2 = \dfrac{di_2}{dt}$; $\dot{v}_1 = \dfrac{dv_1}{dt}$; $\dot{v}_2 = \dfrac{dv_2}{dt}$

COUPLED INDUCTOR EQUATIONS



L_1 AND L_2 ARE SELF INDUCTANCES

M IS THE MUTUAL INDUCTANCE

$$v_A = L_1 \dot{i}_1 + M \dot{i}_2$$
$$v_B = M \dot{i}_1 + L_2 \dot{i}_2$$

LET $\quad x = \left[i_1, \ i_2, \ v_1, \ v_2 \right]^T$

WE NEED TO SOLVE FOR $\dot{i}_1$ AND $\dot{i}_2$ IN (1A) AND (1B) WHICH ARE REPEATED BELOW.

$$L_1 \dot{i}_1 + M \dot{i}_2 = V_g - v_2$$

$$M \dot{i}_1 + L_2 \dot{i}_2 = V_g - v_1$$ (11)

USE CRAMER'S RULE:

$$\dot{i}_1 = \frac{\begin{vmatrix} V_g - v_2 & M \\ V_g - v_1 & L_2 \end{vmatrix}}{\begin{vmatrix} L_1 & M \\ M & L_2 \end{vmatrix}} = \frac{(L_2 - M) V_g - v_2 L_2 + v_1 M}{\sigma^2}$$

WHERE $\sigma^2 = L_1 L_2 - M^2$

$$\dot{i}_2 = \frac{\begin{vmatrix} L_1 & V_g - v_2 \\ M & V_g - v_1 \end{vmatrix}}{\begin{vmatrix} L_1 & M \\ M & L_2 \end{vmatrix}} = \frac{(L_1 - M) V_g - L_1 v_1 + M v_2}{\sigma^2}$$

PUTING IN THE FORM $\dot{x} = Ax + BV_g \rightarrow$

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{M}{\sigma^2} & -\frac{L_2}{\sigma^2} \\ 0 & 0 & -\frac{L_1}{\sigma^2} & \frac{M}{\sigma^2} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{L_2 - M}{\sigma^2} \\ \frac{L_1 - M}{\sigma^2} \\ 0 \\ 0 \end{bmatrix} V_g$$

$\therefore \Rightarrow$

$$A_1 = A_2 = \begin{bmatrix} 0 & 0 & \frac{M}{\sigma^2} & \frac{-L_2}{\sigma^2} \\ 0 & 0 & -\frac{L_1}{\sigma^2} & \frac{M}{\sigma^2} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix}$$

$$b_1 = \begin{bmatrix} \frac{L_2 - M}{\sigma^2} \\ \frac{L_1 - M}{\sigma^2} \\ 0 \\ 0 \end{bmatrix} \qquad b_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$A \equiv DA_1 + D'A_2 = A_1 = A_2$$

$$b \equiv Db_1 + D'b_2 = \begin{bmatrix} D\left(\frac{L_2 - M}{\sigma^2}\right) \\ D\left(\frac{L_1 - M}{\sigma^2}\right) \\ 0 \\ 0 \end{bmatrix}$$

$$x(0) = -A^{-1} b\, V_g$$

A^{-1} MAY BE DETERMINED BY USING

$$A^{-1} = \frac{\text{ADJOINT } (A)}{\text{DET } A}$$

$\therefore$

$$x(0) = -\underbrace{\begin{bmatrix} -\frac{L_1}{R} & -\frac{M}{R} & 0 & C_2 \\ 0 & 0 & C_1 & 0 \\ -M & -L_2 & 0 & 0 \\ -L_1 & -M & 0 & 0 \end{bmatrix}}_{A^{-1}} \underbrace{\begin{bmatrix} \frac{D(L_2 - M)}{\sigma^2} \\ \frac{D(L_1 - M)}{\sigma^2} \\ 0 \\ 0 \end{bmatrix}}_{b} \; V_g$$

$$x(0) = -V_g \begin{bmatrix} \dfrac{D\left(-L_1L_2 + \cancel{L_1M} - \cancel{ML_1} + M^2\right)}{R\sigma^2} \\ 0 \\ \dfrac{D\left(-\cancel{ML_2} + M^2 - L_2L_1 + \cancel{L_2M}\right)}{\sigma^2} \\ \dfrac{D\left(-L_1L_2 + \cancel{L_1M} - \cancel{ML_1} + M^2\right)}{\sigma^2} \end{bmatrix}$$

WHERE

$$\sigma^2 = L_1L_2 - M^2$$

$$\Rightarrow$$

$$x(0) = \begin{bmatrix} I_1 \\ I_2 \\ V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \dfrac{DV_g}{R} \\ 0 \\ DV_g \\ DV_g \end{bmatrix}$$

$$\Delta x = \left[A_1 x(0) + b_1 V_g \right] DT_s$$

$$\Rightarrow \quad \Delta x = \left\{ \begin{bmatrix} 0 & 0 & \frac{M}{\sigma^2} & -\frac{L_2}{\sigma^2} \\ 0 & 0 & -\frac{L_1}{\sigma^2} & \frac{M}{\sigma^2} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} \frac{DV_g}{R} \\ 0 \\ DV_g \\ DV_g \end{bmatrix} + \begin{bmatrix} \frac{L_2 - M}{\sigma^2} \\ \frac{L_1 - M}{\sigma^2} \\ 0 \\ 0 \end{bmatrix} V_g \right\} DT_s$$

$$\Rightarrow \quad \Delta x = \begin{bmatrix} \Delta i_1 \\ \Delta i_2 \\ \Delta v_1 \\ \Delta v_2 \end{bmatrix} = \begin{bmatrix} \left(\frac{L_2 - M}{\sigma^2}\right) D' V_g \\ \left(\frac{L_1 - M}{\sigma^2}\right) D' V_g \\ 0 \\ 0 \end{bmatrix} DT_s$$

THE CURRENT RIPPLE FEEDING THE LOAD IS OF PARTICULAR INTEREST AND IS GIVEN BY

$$\Delta i_1 = \left(\frac{L_2 - M}{\sigma^2}\right) D' V_g \, DT_s \qquad \text{WHERE} \quad \sigma^2 = L_1 L_2 - M^2$$

<u>CASE 1</u>:

FOR <u>$M = 0$</u> (NO COUPLING) $\Rightarrow \quad \Delta i_1 = \dfrac{D' V_g \, DT_s}{L_1}$

WHICH CHECKS WITH PREVIOUSLY OBTAINED RESULTS

CASE 2:

For $\underline{M = L_2} \Rightarrow \Delta i_1 = 0$

THUS TO FIRST ORDER THE OUTPUT CURRENT RIPPLE IS ZERO $\Rightarrow$ OUTPUT VOLTAGE RIPPLE IS ZERO

NOTE THAT THE RIPPLE ON THE CAPACITORS, Δv_1 AND Δv_2, ARE ZERO REGARDLESS OF THE VALUE OF M. THIS IS A CONSEQUENCE OF USING A FIRST ORDER ANALYSIS; IT SHOWS THAT THERE IS NO FIRST ORDER TERMS IN THESE RIPPLE VOLTAGES.

RIPPLE EVALUATION : AN EXTENSION — SECOND ORDER TERMS

FROM THE PREVIOUS EXAMPLE WE SEE THAT THE GENERALLY DOMINANT FIRST ORDER TERMS MAY BE ZERO. WHEN THIS HAPPENS IT IS OF INTEREST TO LOOK AT THE SECOND ORDER TERMS.

THESE TERMS OBTAINED BY INCLUSION OF THE SECOND ORDER TERMS IN THE TAYLOR SERIES EXPANSION OF THE STATE TRANSITION MATRIX GIVEN IN (4) INTO EQUATION (7) ARE AS FOLLOWS

$$x^{(2)}(t) = \frac{A_i^2}{2}(t-t_j)^2\, x(t_j) + \frac{A_i}{2}(t-t_j)^2\, b_i V_g \qquad (19A)$$

$$= \frac{(t-t_j)^2 A_i}{2}\left[A_i\, x(t_j) + b_i V_g\right] \qquad (19B)$$

WHERE $x^{(2)}(t)$ REPRESENTS THE SECOND ORDER TERMS OF THE STATE VECTOR $x(t)$.

WITH THE ASSUMPTION THAT THE MAXIMUM AND MINIMUM VALUES OF THE SECOND ORDER TERMS OCCUR HALF WAY THROUGH EACH SUBINTERVAL, WE THEN ARE INTERESTED TO FIND $x^{(2)}\left(\frac{DT_s}{2}\right)$ AND $x^{(2)}\left(DT_s + \frac{D'T_s}{2}\right)$

USING (19B) WE HAVE

$$x^{(2)}\left(\frac{DT_s}{2}\right) = \frac{(DT_s)^2}{8} A_1 \left[A_1 x(0) + b_1 V_g \right] \qquad (20A)$$

AND

$$x^{(2)}\left(DT_s + \frac{D'T_s}{2}\right) = \frac{(D'T_s)^2}{8} A_2 \left[A_2 x(DT_s) + b_2 V_g \right] \qquad (20B)$$

NOW EQN (18) :

$$\Delta x \approx \left[A_1 x(0) + b_1 V_g \right] DT_s \qquad (18)$$

(18) AND (20A) $\Rightarrow$

$$x^{(2)}\left(\frac{DT_s}{2}\right) \approx \frac{DT_s}{8} A_1 \Delta x \qquad (21)$$

ALSO

$$\Delta x = x(DT_s) - x(0) \qquad (22A)$$
$$= x(DT_s) - x(T_s) \qquad (22B);$$ SINCE $x(0) = x(T_s)$ IN STEADY STATE

$x(T_s)$ IS GIVEN BY (9B)

$\therefore$ (9B) AND (22B) $\Rightarrow$

$$\Delta x = -\left[A_2 x(DT_s) + b_2 V_g \right] D'T_s \qquad (23)$$

$\therefore$ (20B) AND (23) $\Rightarrow$

$$x^{(2)}\left(DT_s + \frac{D'T_s}{2}\right) = -\frac{D'T_s}{8} A_2 \Delta x \qquad (24)$$

THE PEAK – TO – PEAK AMPLITUDE OF THE SECOND ORDER TERMS IS DEFINED AS FOLLOWS

$$\Delta^2 x = x^{(2)}\left(\frac{DT_s}{2}\right) - x^{(2)}\left(DT_s + \frac{D'T_s}{2}\right) \qquad (25)$$

(25), (21) AND (24) $\Rightarrow$

$$\Delta^2 x = \left(DA_1 + D'A_2\right) \Delta x \frac{T_s}{8}$$

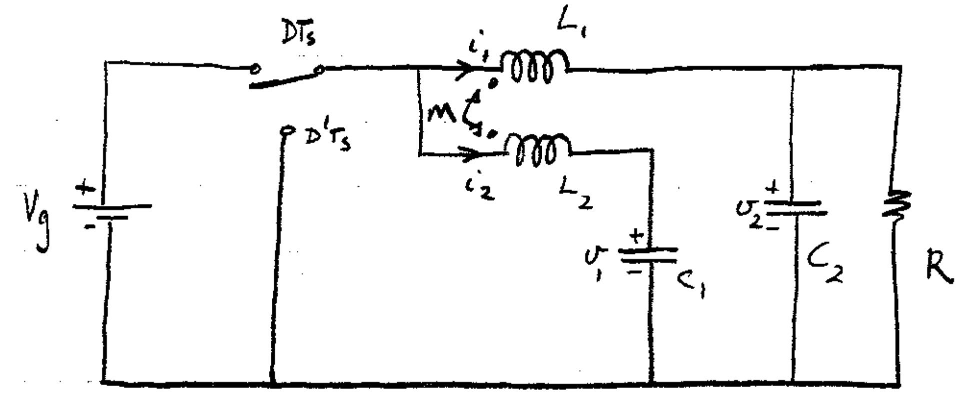
$$\Rightarrow \boxed{\Delta^2 x = A \, \Delta x \frac{T_s}{8}} \qquad (26)$$

WHERE A, THE AVERAGED STATE MATRIX WAS PREVIOUSLY DEFINED IN (13A) (REPEATED BELOW)

$$A = DA_1 + D'A_2 \qquad (13A)$$

EXAMPLE: BUCK CONVERTER WITH COUPLED WINDING

THIS IS THE SAME AS THE PREVIOUS EXAMPLE FOR WHICH WE NOW WILL FIND THE SECOND ORDER TERMS IN THE STATE RIPPLE



$$x = [i_1, i_2, v_1, v_2]^T$$

BEFORE WE FOUND

$$A_1 = A_2 = A = \begin{bmatrix} 0 & 0 & \frac{M}{\sigma^2} & -\frac{L_2}{\sigma^2} \\ 0 & 0 & -\frac{L_1}{\sigma^2} & \frac{M}{\sigma^2} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \quad \text{WHERE } \sigma^2 = L_1 L_2 - M^2$$

AND

$$\Delta x = \begin{bmatrix} \frac{L_2 - M}{\sigma^2} \\ \frac{L_1 - M}{\sigma^2} \\ 0 \\ 0 \end{bmatrix} D' V_g DT_s$$

THE SECOND ORDER RIPPLE IS GIVEN BY (26)

$$\Delta^2 x = A \, \Delta x \frac{T_s}{8}$$

$$= \begin{bmatrix} 0 & 0 & \frac{M}{\sigma^2} & -\frac{L_2}{\sigma^2} \\ 0 & 0 & -\frac{L_1}{\sigma^2} & \frac{M}{\sigma^2} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} \frac{L_2 - M}{\sigma^2} \\ \frac{L_1 - M}{\sigma^2} \\ 0 \\ 0 \end{bmatrix} D'V_g \frac{DT_s^2}{8}$$

$$\Delta^2(x) = \left[0, \quad 0, \quad \frac{L_1 - M}{C_1 \sigma^2} D'V_g \frac{DT_s^2}{8}, \quad \frac{L_2 - M}{C_2 \sigma^2} D'V_g \frac{DT_s^2}{8} \right]^T$$

CASE 1 : UNCOUPLED INDUCTORS : $M = 0$

$$\Rightarrow \quad \Delta^2 v_1 = \frac{D'V_g DT_s^2}{8 L_2 C_1}$$

AND

$$\Delta^2 v_2 = \frac{D'V_g DT_s^2}{8 L_1 C_2}$$

THESE RESULTS CORRESPOND TO THOSE PREVIOUSLY OBTAINED USING ANOTHER METHOD.

CASE 2 : $M = L_2 \Rightarrow \Delta i_1 = 0$

$$\Rightarrow \quad \Delta^2 v_1 = \frac{D' V_g D T_s^2}{8 L_2 C_1}$$

AND

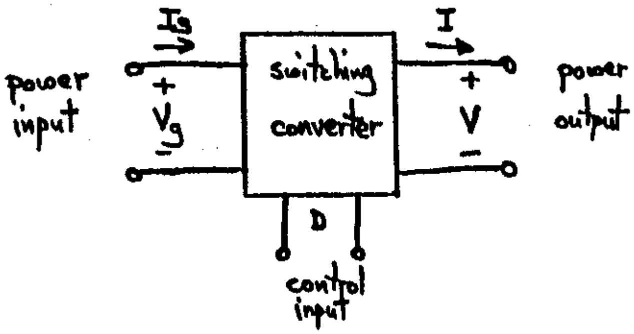
$$\Delta^2 v_2 = 0$$

$\therefore$ THE OUTPUT VOLTAGE RIPPLE IS NULLED FOR THE CONDITION $M = L_2$

Lecture : Losses, Conservation of Power, Dc converter model

1. Conservation of Power

Any switching converter contains three ports: a power input, a control input, and a power output.



The input power is processed as specified by the control input, and then it is output to the load.

Ideally, these functions are performed with 100% efficiency, and hence

$$P_{in} = P_{out}$$

$$\text{or,} \quad V_g I_g = V I$$

These relations are valid only under equilibrium (dc) conditions — during transients the converter inductors and capacitors may store or discharge energy.

In the previous lecture, we found that

$$V = M(D)\ V_g$$

where $M(D)$ = equilibrium conversion ratio

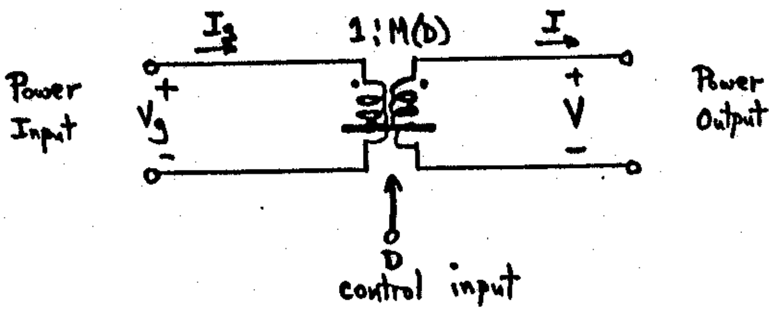
for ex, $M(D) = D$ for buck converter
$M(D) = 1/(1-D)$ for boost converter

Thus, we have

$$V_g I_g = V I$$
$$V = M(D) V_g$$
$$\Rightarrow I_g = M(D) I$$

These equations resemble the relations in the ideal transformer.

2. Ideal dc converter model



This models the first-order dc properties of the switched-mode converter: transformation of dc voltage and current levels, ideally with 100% efficiency, controllable by D.

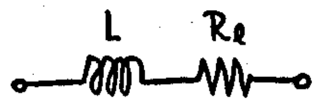
Second-order dc properties

3. Inductor core and copper losses

Practical inductors exhibit power loss, owing to

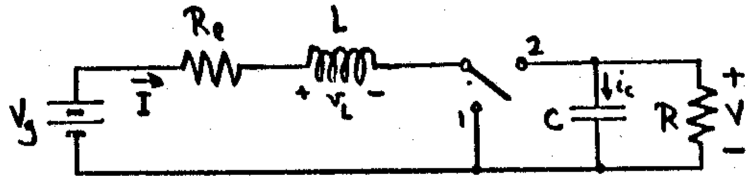
1) copper losses – resistance of the wire
2) core losses – hysteresis and eddy curre

A suitable model which describes these effects is

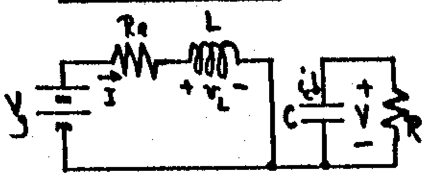


The effects of inductor losses on the overall converter properties may be found by use of the principle of inductor volt-sec balance.

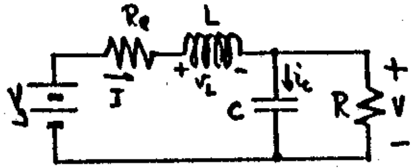
Boost Example with inductor losses



Switch in position 1
$0 \le t \le DT_s$



Switch in position 2
$DT_s \le t \le T_s$



$$v_L = V_g - IR_\ell \qquad\qquad v_L = V_g - IR_\ell - V$$
$$i_c = -V/R \qquad D + D' \triangleq 1 \qquad i_c = I - V/R$$

Volt-sec balance: $\langle v_L \rangle = 0 = D(V_g - IR_\ell) + D'(V_g - IR_\ell - V)$
$$\Rightarrow V_g - IR_\ell - D'V = 0$$

charge balance: $\langle i_c \rangle = 0 = D(-V/R) + D'(I - V/R)$
$$\Rightarrow D'I - V/R = 0$$

solution for I and V yields

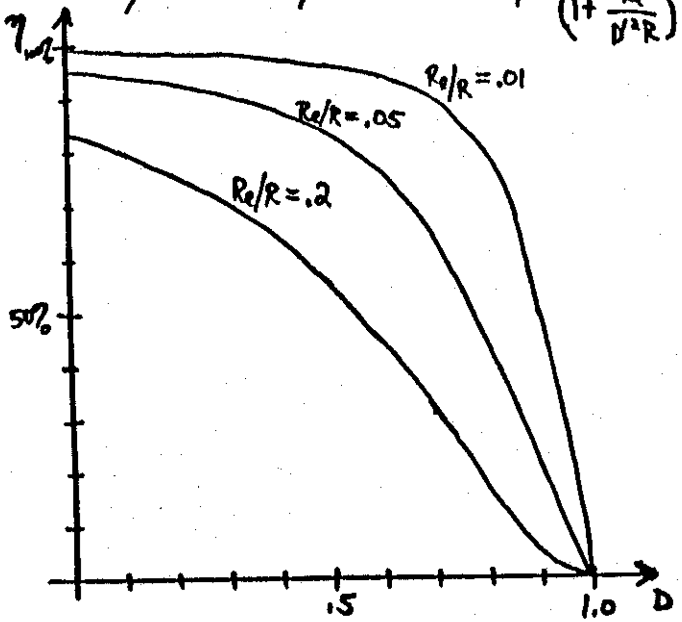
$$\frac{V}{V_g} = \underbrace{\frac{1}{D'}}_{M(D)} \cdot \underbrace{\frac{1}{\left(1 + \frac{R_\ell}{D'^2 R}\right)}}_{\eta(D,\, R_\ell/R)}, \quad I = \underbrace{\frac{1}{D'^2}}_{M^2(D)} \cdot \underbrace{\frac{1}{\left(1 + \frac{R_\ell}{D'^2 R}\right)}}_{\eta(D,\, R_\ell/R)} \frac{V_g}{R}$$

or, $V = M \eta V_g \qquad I = M^2 \eta \frac{V_g}{R} = M \frac{V}{R}$

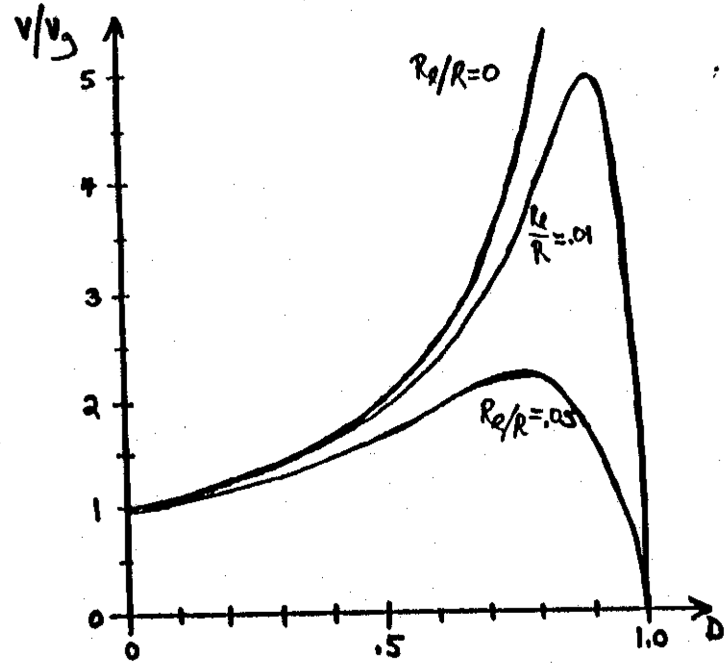
where $M =$ ideal $(R_\ell = 0)$ conversion ratio
$\eta =$ efficiency $= 1/\left(1 + \frac{R_\ell}{D'^2 R}\right)$

note that $P_{in} = V_g I = \eta \frac{(MV_g)^2}{R}$
$P_{out} = V^2/R = \eta^2 \frac{(MV_g)^2}{R} = \eta P_{in}$ ✓

efficiency vs. duty ratio $\quad \eta = \dfrac{1}{\left(1 + \dfrac{R_\ell}{D'^2 R}\right)}$



Output voltage vs. duty ratio



$$\frac{V}{V_g} = M(D)\,\eta(D, R_\ell/R) = \frac{1}{D'}\,\frac{1}{\left(1 + \dfrac{R_\ell}{D'^2 R}\right)}$$

4. Steady-State Converter Model, with Losses Accounted For

For this boost converter example, we found that

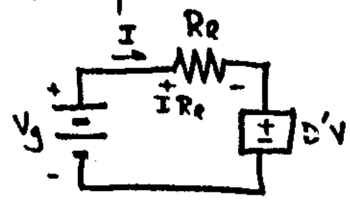
$V_g - I R_e - D'V = 0$ (by use of inductor volt-sec balance)

$D'I - V/R = 0$ (by use of capacitor charge balance)

One may easily reconstruct a ciruit model from these equations which describes the dc behavior of the boost converter with inductor losses. This is done by constructing a circuit whose Kirchoff loop and node equations are identical to the two equations above.

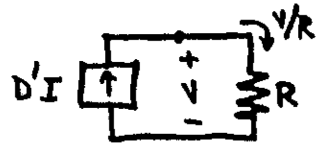
1. $V_g - I R_e - D'V = 0$

This is a loop equation since it involves voltages. Voltage source V_g, resistor R_e (with voltage drop $I R_e$), and another voltage source with value $D'V$ are connected in a loop:

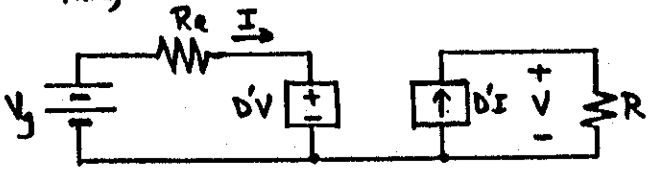


2. $D'I - V/R = 0$

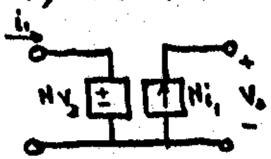
This is a node equation since it involves currents. A current source of value $D'I$ and resistor R (with current V/R) come together at a node:



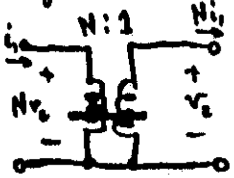
Thus, we have:



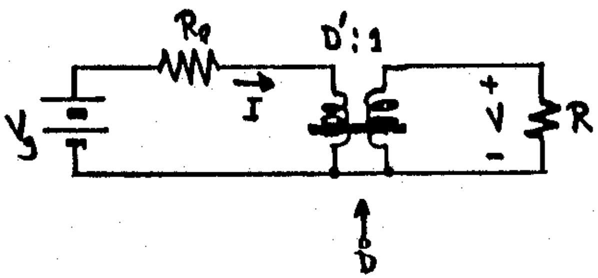
Next, note that



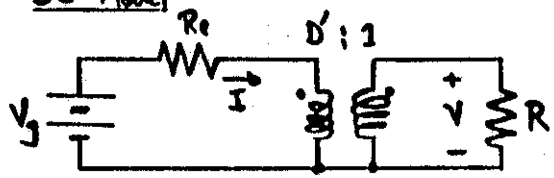
is equivalent to



⇒ the dc model becomes



DC Model



Model describes basic properties of converter:

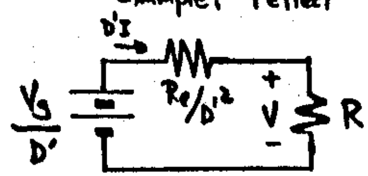
a) transformation of dc voltage and current levels

b) second order effects – power losses

c) dc conversion ratio V/V_g

Can perform circuit manipulations on model –

Example: reflect V_g & R_e through transformer



solve for V/V_g, $I/(V_g/R)$ by inspection

$$V = \frac{V_g}{D'} \frac{R}{R + \frac{R_e}{D'^2}} = \frac{V_g}{D'} \frac{1}{1 + R_e/D'^2 R}$$

$$D'I = \left(\frac{V_g}{D'}\right) \Big/ \left(\frac{R_e}{D'^2} + R\right)$$

$$\Rightarrow I = \frac{V_g}{D'^2 R} \frac{1}{\left(1 + \frac{R_e}{D'^2 R}\right)}$$

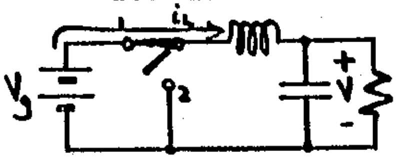
Other Sources of Power Loss

5. Semiconductor Conduction Losses

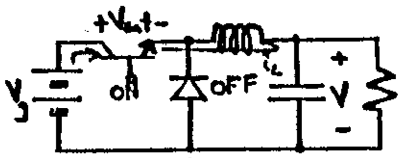
The voltage drop across a practical switch is never really zero.

Example: Realization of switch using transistor and diode in buck converter

Ideal circuit

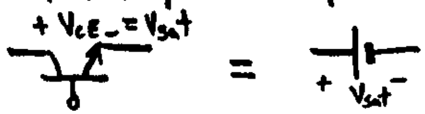


Practical circuit



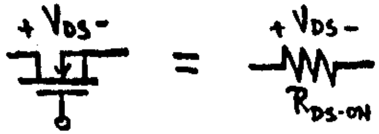
Switch in position 1 - place transistor in saturated state

BJT



Typically, $V_{sat} \approx 0.5 - 1.0\,V$

MOSFET



$V_{DS} \approx 0.5 - 5.0\,V$

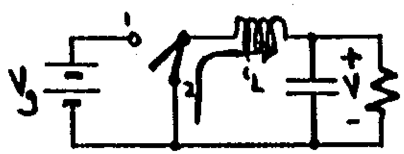
Other Sources of Power Loss

5. Semiconductor Conduction Losses

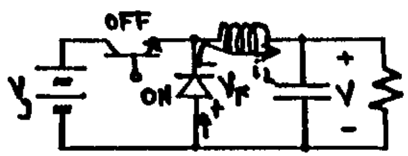
The voltage drop across a practical switch is never really zero.

Example: Realization of switch using transistor and diode in buck converter

Ideal circuit



Practical circuit



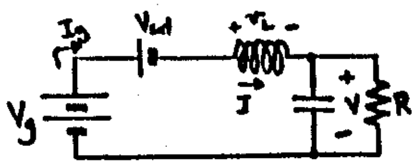
Switch in position 2 - transistor OFF, diode conducts

Typically, $V_F = \begin{cases} .8 - 1.2\,V & \text{for fast recovery diodes} \\ .3 - .6\,V & \text{for Schottky diodes} \end{cases}$

The same steady-state analysis techniques (volt-second balance, charge balance, small ripple) can be used to determine the effects of these voltage drops.

<u>Buck converter example</u>

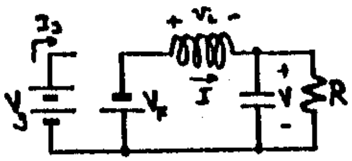
<u>Transistor conducts</u>



$v_L = V_g - V_{sat} - V$

$I_g = I$

<u>Diode conducts</u>



$v_L = -V - V_F$

$I_g = 0$

Inductor volt-second balance:

$$D(V_g - V_{sat} - V) + D'(-V - V_F) = 0$$

$$\Rightarrow D(V_g - V_{sat}) = (V + D'V_F)$$

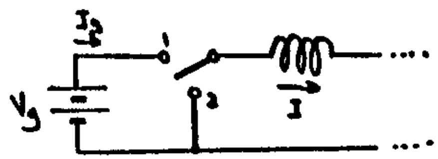
can solve for $\frac{V}{V_g}$ now if desired.

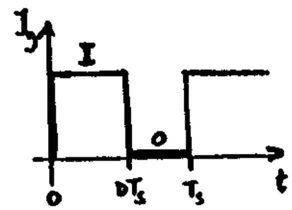
$$\frac{1}{D} = \frac{(V_g - V_{sat})}{(V + D'V_F)}$$

Find efficiency η vs. V_{sat}, V_F :

$\eta = \dfrac{P_{out}}{P_{in}}$, so must first find P_{out} and P_{in}

<u>input power</u>



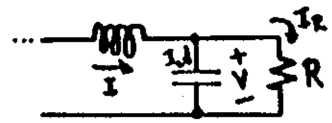


Input power during 1^{st} interval $= I_g V_g = I V_g$

Input power during 2^{nd} interval $= I_g V_g = 0 \cdot V_g = 0$

Average input power $= P_{in} = D(I V_g) + D'(0) = D I V_g$

<u>output power</u>



In steady state, $\langle I_C \rangle = 0$

$\Rightarrow \langle I_R \rangle = \langle I \rangle$

Average output power $= P_{out} = V I_R = V I$

so

$$\eta = \frac{P_{out}}{P_{in}} = \frac{VI}{DV_g I} = \frac{1}{D}\frac{V}{V_g} \quad \text{for Buck example}$$

but we found that

$$\frac{1}{D} = \frac{(V_g - V_{sat})}{(V + D'V_F)}$$

so

$$\boxed{\eta = \frac{(V_g - V_{sat})}{V_g} \cdot \frac{V}{(V + D'V_F)}}$$

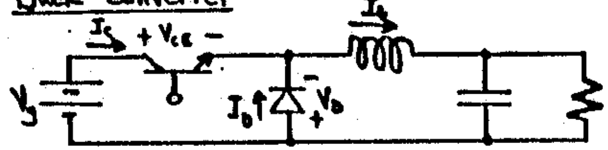
$\frac{(V_g - V_{sat})}{V_g}$ describes effect of the transistor saturation voltage

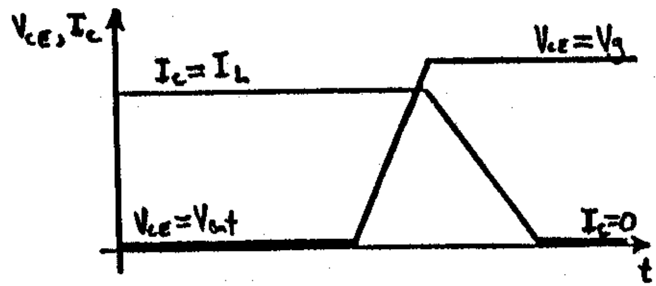
$\frac{V}{(V + D'V_F)}$ describes effect of the diode forward voltage drop

6. Semiconductor Switching Losses

Switching transitions (between switch positions 1 and 2) are never instantaneous - a certain amount of time is required to turn a semiconductor switch on or off. During this switching time, the transistor typically passes through a period of high instantaneous power dissipation.

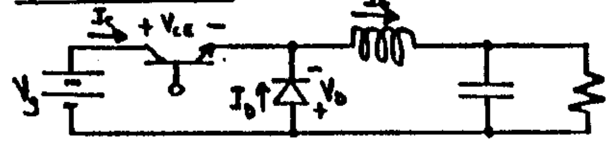
Buck converter

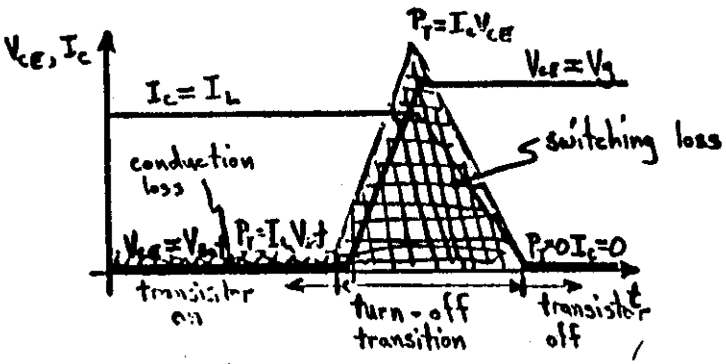




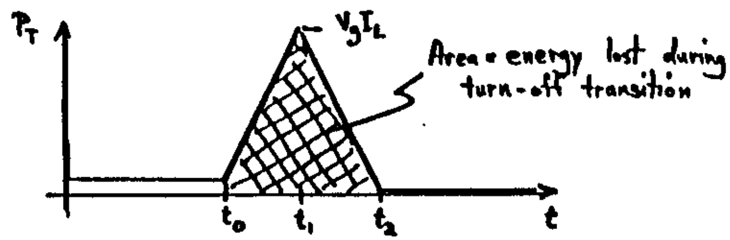
Switching transitions (between switch positions 1 and 2) are never instantaneous – a certain amount of time is required to turn a semiconductor switch on or off. During this switching time, the transistor typically passes through a period of high instantaneous power dissipation.

Buck converter





Estimation of switching loss – turn off calculations



Energy lost during one turn-off transition

$$= \text{area} = \tfrac{1}{2} V_g I_L (t_2 - t_0) = E_T$$

This much energy is lost once each switching cycle. Power loss = energy lost per second

$$= E_T f_s \qquad \text{where } f_s = \text{switching frequency}$$

$$= E_T / T_s \qquad T_s = 1/f_s$$

so turn-off transition switching loss

$$= \tfrac{1}{2} V_g I_L \frac{(t_2 - t_0)}{T_s} \quad (\text{watts})$$

Efficiency may now be calculated by use of

$$\eta = \frac{P_{out}}{P_{in}}, \text{ with } P_{out} + P_{loss} = P_{in}$$

Summary

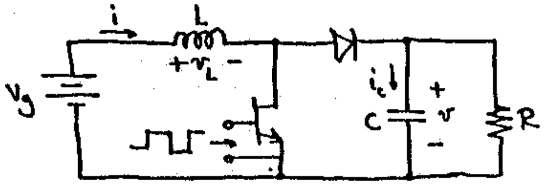
1. Dc "transformer" model - describes principal functions of converter in lucid, circuit-oriented way

2. Effects of losses may be determined by use of the same analysis techniques - inductor volt-sec balance, etc.

3. Principal sources of converter inefficiency:
   - magnetics core & copper losses
   - semiconductor conduction losses
   - semiconductor switching losses

Semiconductor Conduction Losses

Boost Converter Example:



Switch in position 1: transistor on, diode off

can model transistor conduction losses as:

||

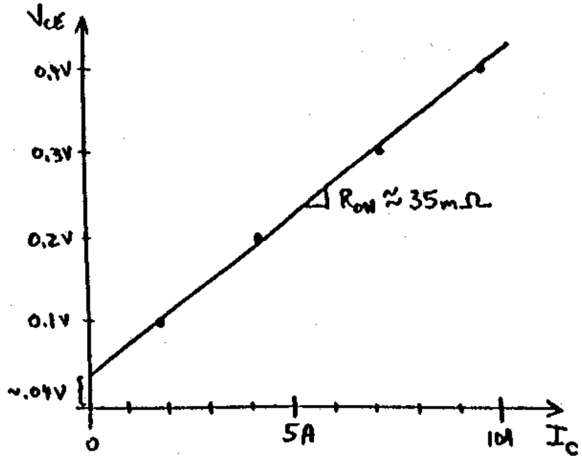
or,

R_{ON} more accurate for power transistors than V_{SAT}.

Use R_{ON} in this example.

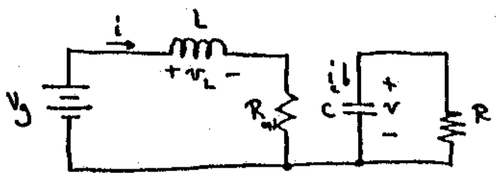
Example D44H10 NPN transistor 10A, 80V

V_{CE} vs. I_C, for $I_B \geq I_C/10$



• experimental data

So we have



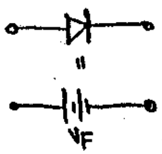
$v_L = V_g - i R_{ON} \approx V_g - I R_{ON}$

Linear Ripple Approx.

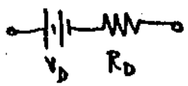
$i_c = -v/R \approx -V/R$

<u>switch in position 2:</u> transistor off, diode on

can model diode as

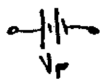


or

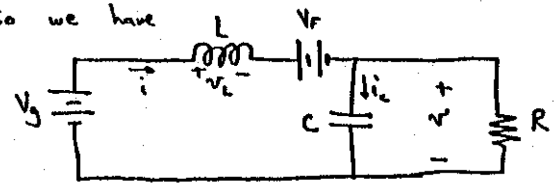


(more accurate)

for this example, use



So we have



$v_L = V_g - V_F - v \cong V_g - V_F - V$

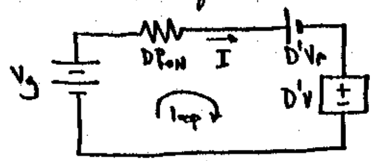
$i_c = i - v/R \cong I - V/R$

<u>inductor volt-sec balance:</u> (steady-state)

$\langle v_L \rangle = D(V_g - I R_{ON}) + D'(V_g - V_F - V) = 0$

$\Rightarrow V_g - D'V - D I R_{ON} - D'V_F = 0$

– a loop equation



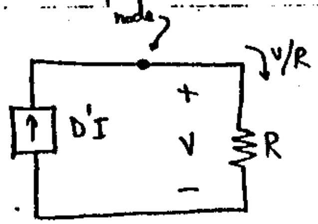
<u>capacitor charge balance:</u>

$\langle i_c \rangle = D(-V/R) + D'(I - V/R) = 0$

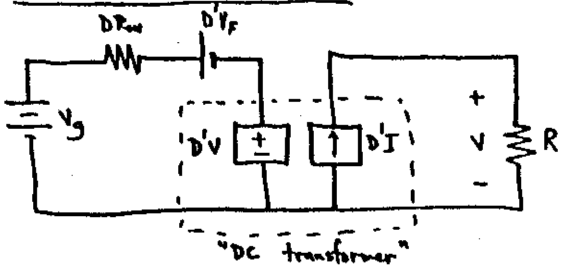
$\Rightarrow D'I - V/R = 0$

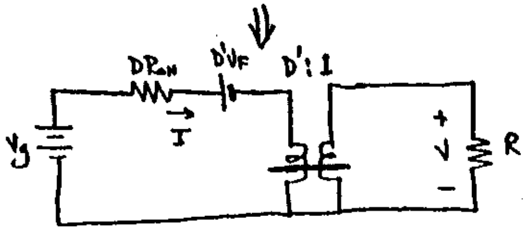
– a node equation

SCL-4

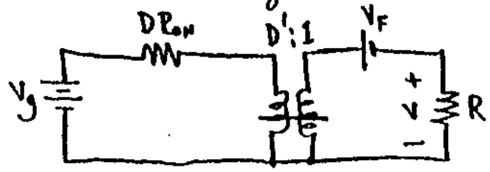


combine the two circuits:



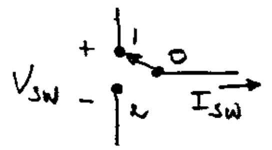


Reflect $D'V_F$ through transformer:



Lecture : Implementation of switches using transistor and diodes
Discontinuous conduction mode

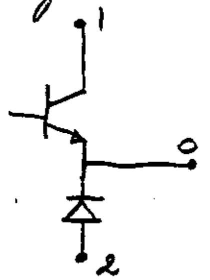
How to realize a switch using semiconductors :

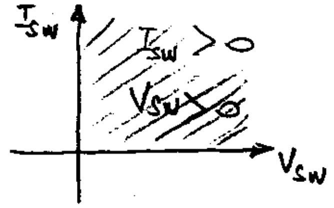


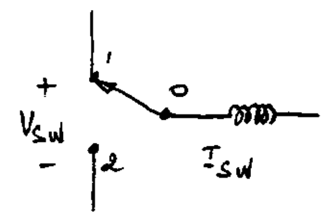
(*)

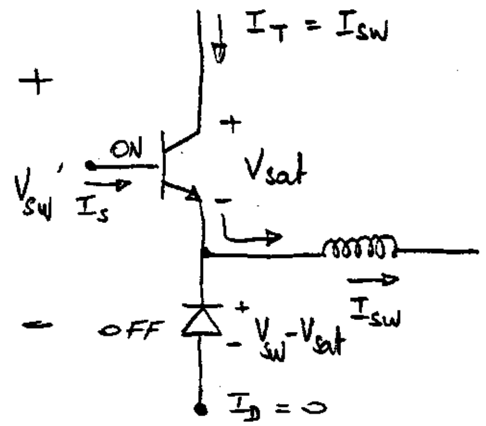
1. Single quadrant switch

If $V_{SW} > 0$ and $I_{SW} > 0$ under all conditions then (*) may be realized by









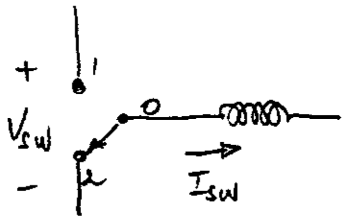
Switch in position 1

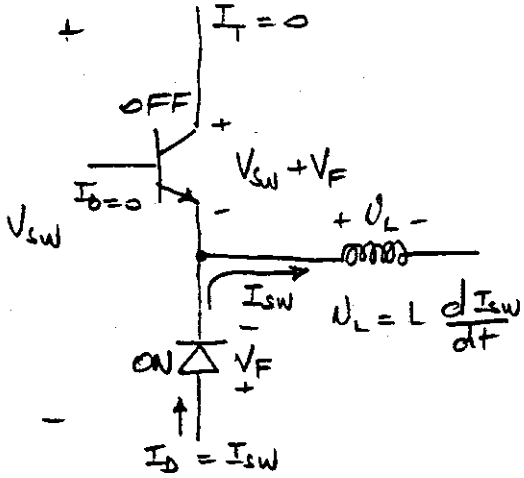
- Diode reverse-biased by voltage $V_{SW} - V_{sat} \cong V_{SW} \Rightarrow I_D = 0$
- Transistor forward biased (by application of base current)

  transistor current $I_T = I_{SW}$

  where V_{sat} = transistor saturation (ON) voltage drop $\cong$ .5-1 Volt

Note that if $V_{SW} < 0$ then diode become forward biased shorting out V_{SW}.





Switch in position 2

Transistor reverse-biased (by removal of base current)

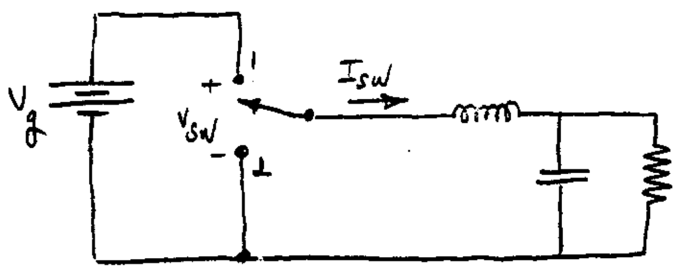
$\Rightarrow I_T = 0 , \quad V_T = V_{SW} + V_F \cong V_{SW}$

Diode must be conduct to provide path for inductor current I_{SW} $\Rightarrow I_D = I_{SW} , \quad V_D = V_F$

where V_F = diode forward Voltage drop $\approx .7$ Volts

Note that if $I_{SW} < 0$, then diode cannot conduct.

Example: Buck converter



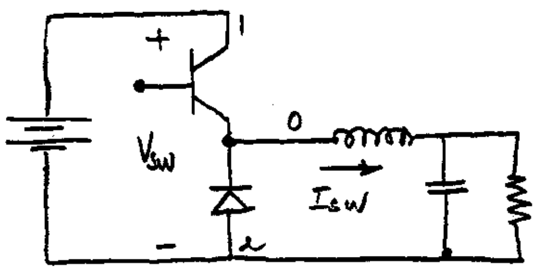
Note that

$V_{SW} = V_g > \phi$

and

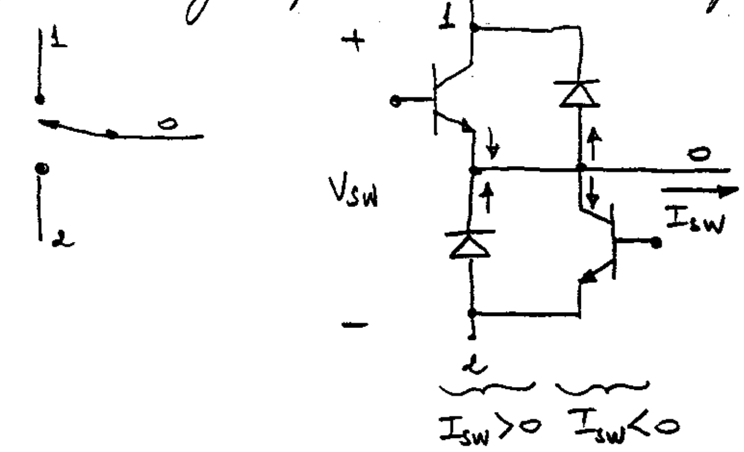
$I_{SW} = I_L$

hence require $I_L > \phi$



2) Two quadrant switch

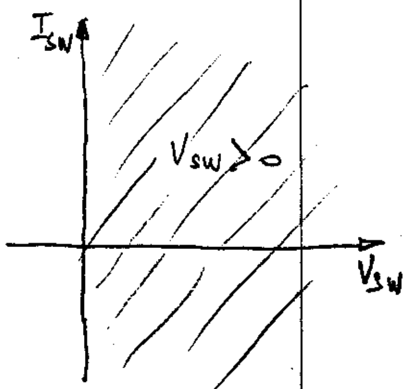
If $V_{sw} > 0$ but I_{sw} of either polarity, the (*) may be realized by two single quadrant switches in parallel:



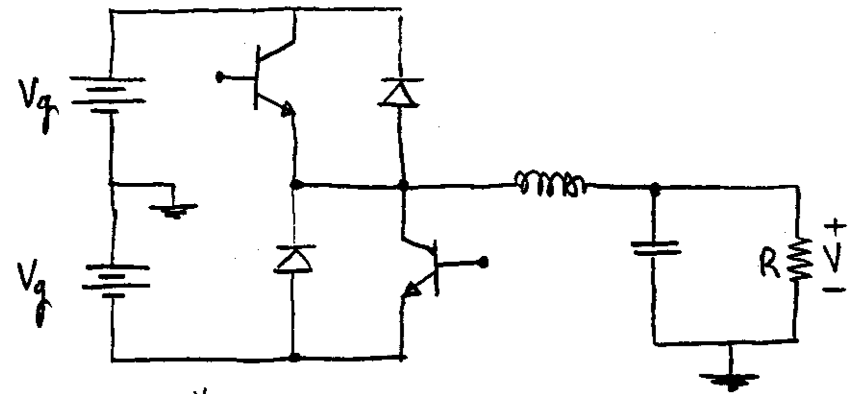
Use first transistor and diode for $I_{sw} > 0$

Second ——————— $I_{sw} < 0$

We must still have $V_{sw} > 0$; otherwise, both diodes conduct simultaneously.

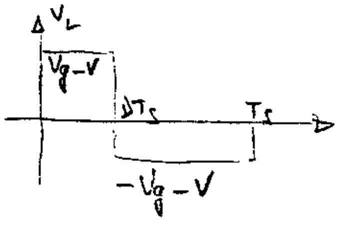


Example: Buck Amplifier



$V_{sw} = \text{Avg} > 0$

$I_{sw} = \frac{V}{R} = \frac{(2D-1)V_g}{R}$



$$D(V_g - V) + D'(-V_g - V) = 0$$
$$-DV + DV_g - D'V_g - D'V = 0$$
$$-V(\underbrace{D + D'}_{1}) + V_g(D - D') = 0$$
$$V = V_g(D - (1-D)) = V_g(2D-1)$$

$$I = \frac{V}{R} = \frac{V_g(2D-1)}{R}$$

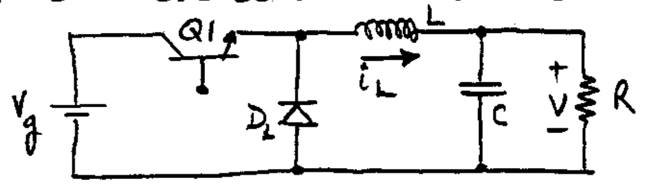
Discontinuous Conduction mode

Often, a converter must work for a wide range of load R. If the load current is decreased (ie, R is increased) to the point where $\Delta i_L > I_o$, then the discontinuous conduction mode occurs, where the inductor current attempts to reverse polarity during one portion of each cycle.

If single quadrant switches are used, then the inductor current is not allowed to become negative. Instead, the diode reverse biases and turn off prematurely. Three intervals then occur during each switching period T_s :

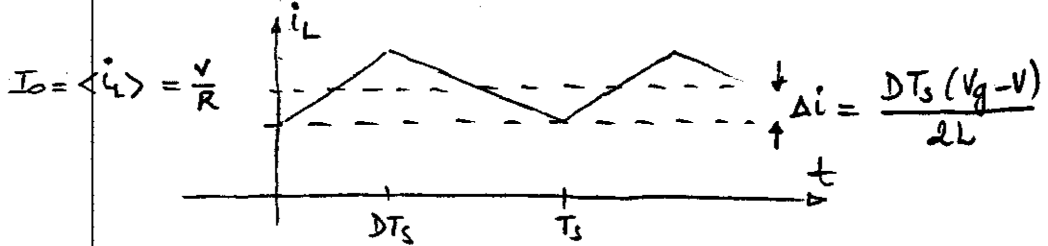
$0 \le t \le D_1 T_s$	Transistor ON	diode OFF
$D_1 T_s \le t \le (D_1 + D_2) T_s$	——— OFF	——— ON
$(D_1 + D_2) T_s \le t \le T_s$	——— OFF	——— OFF

Discontinuous conduction mode – Buck converter example



1. $I_o \gg \Delta i$

Continuous conduction mode



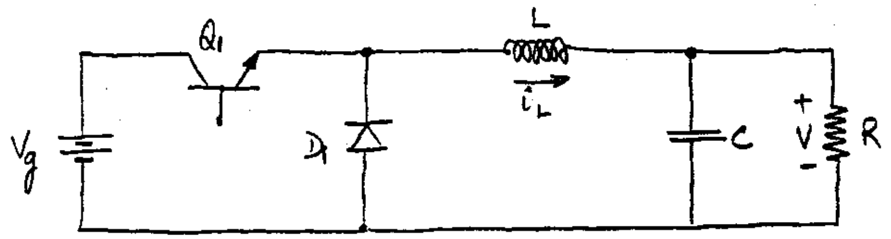
$I_o = \frac{V}{R}$ = dc component of inductor current

Note: I_o Varies with load R

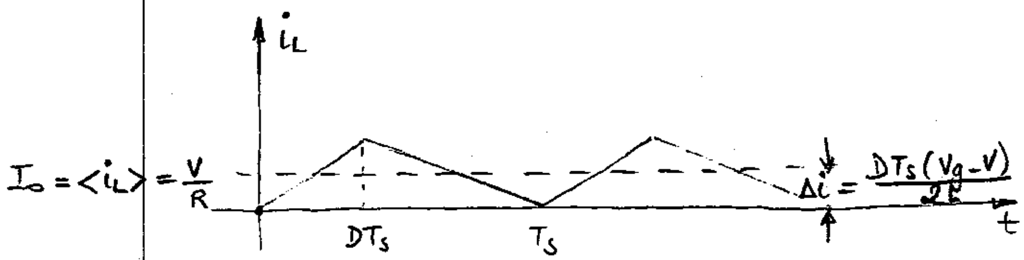
$\Delta i = DT_s (V_g - V)/2L$ = peak current ripple

Δi independent of load R

Discontinuous conduction mode - Buck converter example



a. $I_o = \Delta i$ boundary between modes



$I_o = \frac{V}{R}$ = dc component of inductor current

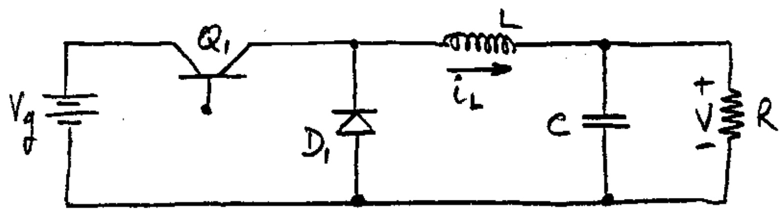
Note: I_o Varies with load R

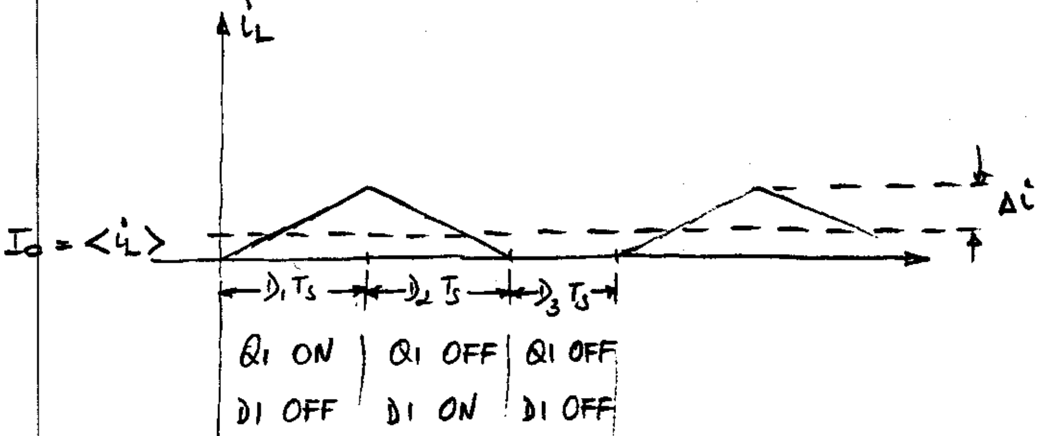
$\Delta i = DT_s(V_g - V)/2L$ = peak current ripple

Δi : independent of load R

Discontinuous conduction mode - Buck converter example

B. $I_o < \Delta i$ discontinuous conduction mode





<u>Conditions for operation in discontinuous mode</u>

If $I_o > \Delta i$ then continuous conduction mode

$I_o < \Delta i$ then discontinuous ______

where I_o : average (dc) inductor current

Δi : inductor current ripple (peak to average)

For the buck converter, we know that

$$I_o = \frac{V}{R} = \frac{DV_g}{R}$$

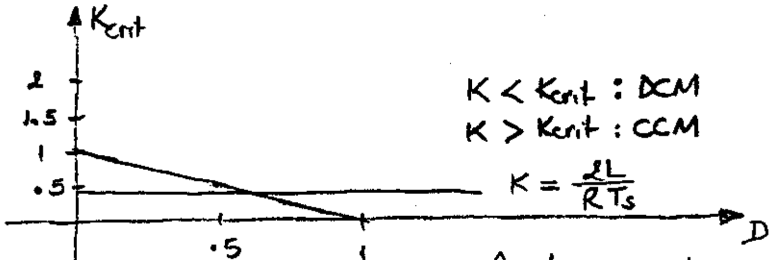
$$\Delta i = \frac{DT_s(V_g - V)}{2L} = \frac{DD'T_sV_g}{2L} \quad \text{where } D' \simeq 1-D$$

So discontinuous mode occurs when $I_o < \Delta i$

$$\Rightarrow \frac{DV_g}{R} < \frac{DD'T_sV_g}{2L} \Rightarrow \frac{2L}{RT_s} < D'$$

or, $K < K_{crit}$ with $K = \frac{2L}{RT_s}$, a dimensionless parameter

$K_{crit} = D'$



Buck converter : $K_{crit} = D' = 1-D$

Note that since $K_{crit} = D' \leq 1$, then if we choose $K > \max(K_{crit})$ or $K > 1$, the converter operates in continuous conduction mode for any possible value of D.

Also note that the boundary between modes depends not only on D, but also on R (which affects the average inductor current), L (which affects the ripple Δi), and T_s (which also affects the ripple).

It is also desired to determine how the change of load R affects the operating mode. The previous expressions can also be written

$R < R_{crit}$ Continuous conduction mode

$R > R_{crit}$ Discontinuous ——————

where $R_{crit} = \frac{2L}{D' T_s}$

Note that $\min(R_{crit}) = \frac{2L}{T_s}$, and hence if $R < \frac{2L}{T_s}$, then the converter operates in continuous conduction mode for all allowed values of D

A similiar analysis may be performed for the boost and buck converters:

$K = \frac{2L}{R T_s}$ in all cases

Converter	$K_{crit}(D)$	$\max_D(K_{crit})$	$R_{crit}(D)$	$\min_D(R_{crit})$
Buck	$1-D$	1	$\frac{2L}{(1-D)T_s}$	$\frac{2L}{T_s}$
Boost	$D(1-D)^2$	$4/27$	$\frac{2L}{D(1-D)^2 T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck-Boost	$(1-D)^2$	1	$\frac{2L}{(1-D)^2 T_s}$	$\frac{2L}{T_s}$

And in general,

$K > K_{crit}(D)$ or $R < R_{crit}(D) \Rightarrow$ Continuous Mode

$K < K_{crit}(D)$ or $R > R_{crit}(D) \Rightarrow$ discontinuous Mode.

Analysis of dc conversion ratio V/V_g

With a few modifications, the same technique and approximations used in the steady-state analysis of the continuous conduction mode may be applied to the discontinuous conduction mode:

1- Inductor Volt-second balance: average (dc) inductor voltage must be zero

$$0 = \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt \Rightarrow i_L(0) = i_L(T_s)$$

2- Capacitor charge balance: average (dc) capacitor current must be zero:

$$0 = \frac{1}{T_s}\int_0^{T_s} i_c(t)\,dt \Rightarrow q_c(0) = q_c(T_s)$$

3- Linear ripple approximation: we must be careful here.

a) Output capacitor voltage ripple.

It is still required that the output voltage ripple be small, and hence in any well-designed converter

$$\Delta v \ll V_o \Rightarrow v(t) \simeq V_o \quad (\text{as before})$$

where V_o : average (dc) output voltage

Δv : peak voltage ripple

$v(t)$: actual output voltage waveform

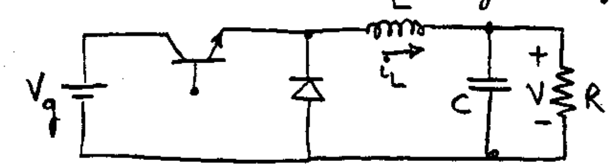
b) Inductor current ripple: The inductor current ripple is not small, since the discontinuous mode occurs only when $\Delta i > I_o \Rightarrow i(t) \not\simeq I_o$

where I_o : average (dc) inductor current

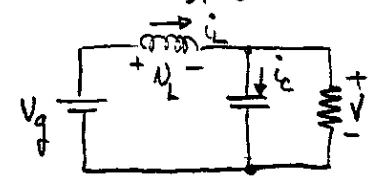
Δi : peak current ripple

$i(t)$: actual inductor current waveform

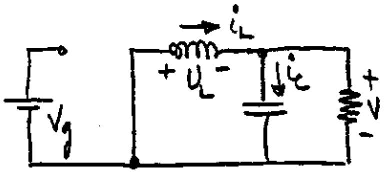
Buck converter example : $\frac{V}{V_g}$ analysis



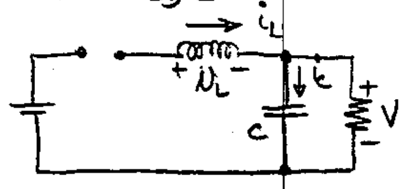
Interval D_1T_s



Interval D_2T_s



Interval D_3T_s



$$L\frac{di_L}{dt} = v_L = V_g - V$$

$$C\frac{dv_c}{dt} = i_c = i_L - \frac{V}{R}$$

$$v_L = -V$$

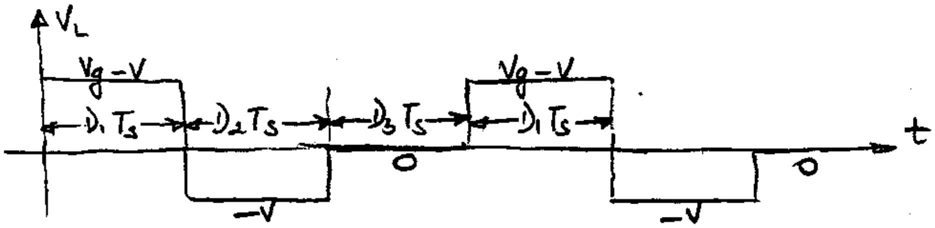
$$i_c = i_L - V/R$$

$$i_L = 0\ ,\ V_L = 0$$

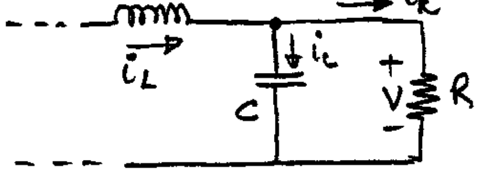
$$i_c = i_L - \frac{V}{R} = -\frac{V}{R}$$

Inductor Volt-sec balance: $\langle v_L \rangle = 0$.

$$D_1(V_g - V) + D_2(-V) + D_3(0) = 0\ ; \Rightarrow \boxed{V = V_g \frac{D_1}{D_1 + D_2}}$$



Next, use capacitor charge balance :



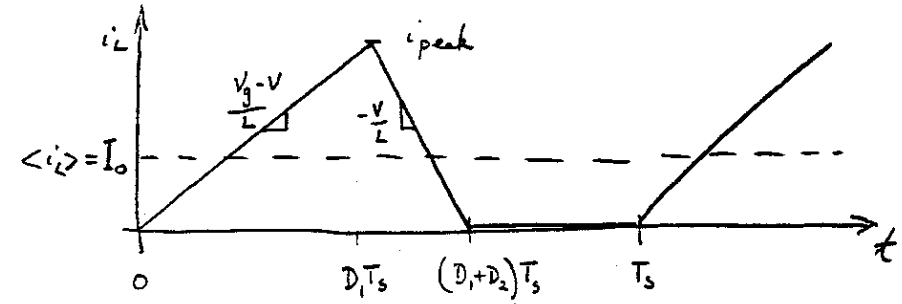
$$i_L = i_c + i_R = i_c + \frac{V}{R}$$

Charge balance : $\langle i_C \rangle = 0$

$\Rightarrow \langle i_L \rangle = 0 + \langle \frac{V}{R} \rangle$ or $\langle i_L \rangle = \frac{V}{R}$

DC component of inductor current = Load current

FIND AVERAGE INDUCTOR CURRENT:



$$i_{peak} = \frac{V_g - V}{L} D_1 T_s$$

$$\langle i_L \rangle = \frac{1}{T_s} \int_0^{T_s} i_L(t)\, dt = \frac{1}{T_s}\left[\frac{1}{2} i_{peak} (D_1 + D_2) T_s \right]$$

$$= \frac{1}{2} i_{peak} (D_1 + D_2)$$

$$= (V_g - V) \frac{D_1 T_s}{2L} (D_1 + D_2)$$

So $\langle i_L \rangle = \frac{V}{R} \Rightarrow$

$$\boxed{\frac{V}{R} = \frac{D_1 T_s}{2L} (D_1 + D_2)(V_g - V)}$$

Thus, we have two unknowns (V and D_2), and two equations:

$$V = V_g \frac{D_1}{D_1 + D_2} \quad \text{(from inductor volt-sec. balance)}$$

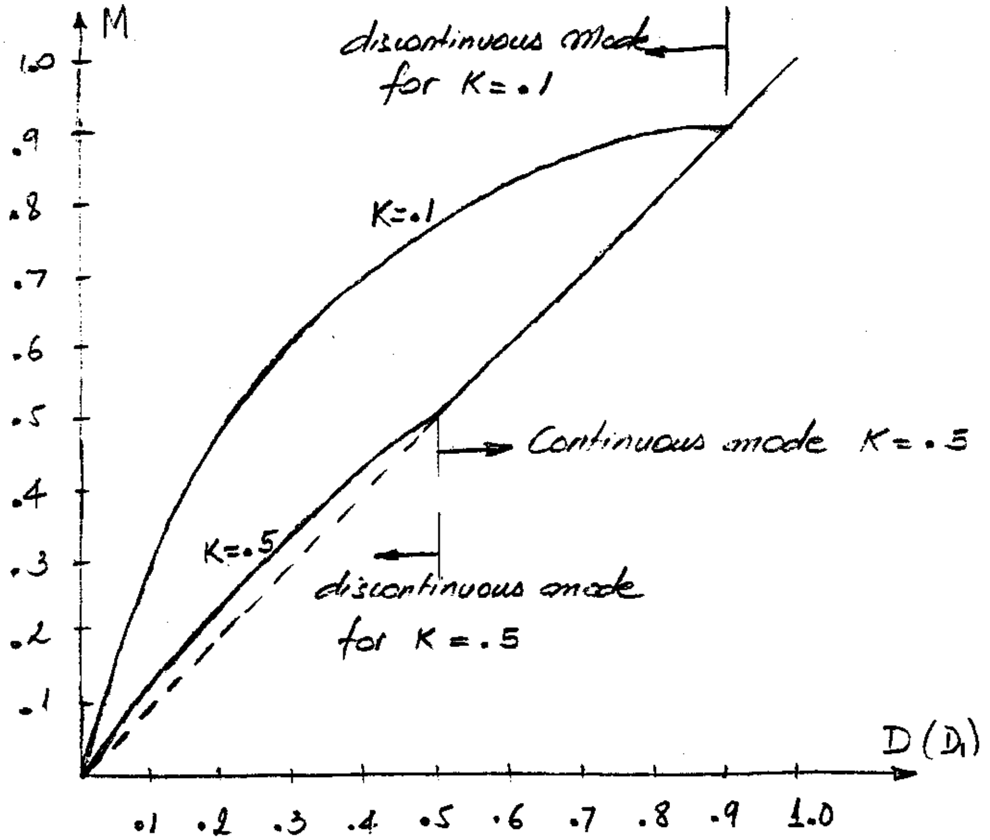
$$\frac{V}{R} = \frac{D_1 T_s}{2L} (D_1 + D_2)(V_g - V) \quad \text{(capacitor charge balance)}$$

Elimination of D_2 and solution for $\frac{V}{V_g}$ yields

$$\boxed{\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + 4K/D_1^2}} = M(D_1, K)}$$

where $K = \frac{2L}{R T_s}$ as before,

valid for $K < K_{crit}$



Voltage gain $= \frac{V}{V_g}$

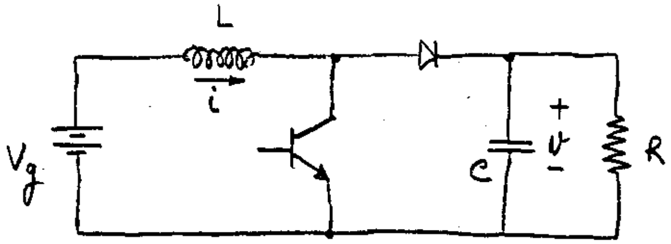
Buck converter

$$K = \frac{2L}{RT_s}, \quad K_{crit} = D' \simeq 1-D \; ; \; M = \begin{cases} D & \text{for } K > K_{crit} \\ \dfrac{2}{1+\sqrt{1+4K/D_1^2}} & \text{for } K < K_{crit} \end{cases}$$

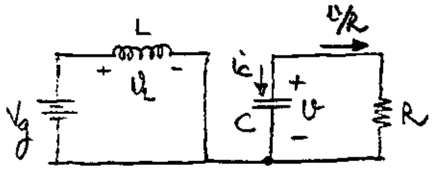
for $K = .1$, $K < K_{crit}$ when $.1 < 1-D \Rightarrow D < .9$

$K = .5$, $K < K_{crit}$ when $.5 < 1-D \Rightarrow D < .5$

Example : Discontinuous Conduction Mode in the boost Converter

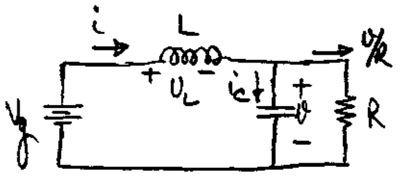


Interval 1 $D_1 T_s$ (neglect losses) Transistor on, diode off



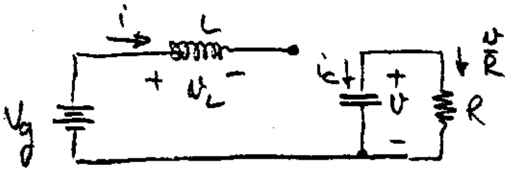
$$L\frac{di}{dt} = v_L = V_g$$
$$C\frac{dv}{dt} = i_c = -\frac{v}{R} \cong -\frac{V}{R}$$

Interval 2 $D_2 T_s$ Transistor off, diode on



$$v_L = V_g - v \cong V_g - V$$
$$i_c = i - \frac{v}{R} \cong I - \frac{V}{R}$$

Interval 3 $D_3 T_s$ transistor off, diode off



$$i = 0 \quad , \quad v_L = 0$$
$$i_c = -\frac{v}{R} \cong -\frac{V}{R}$$

Determine boundary between modes:

In continuous conduction mode, we found that inductor current ripple $\Delta i = \frac{D T_s V_g}{2L}$

and average inductor current $I_o = \frac{V}{D'R}$

The boundary between modes is found as follows:

$I_o > \Delta i$ for CCM

$I_o < \Delta i$ for DCM

$$\Rightarrow \frac{V}{D'R} > \frac{DT_sV_g}{2L} \quad \text{for CCM}$$

but

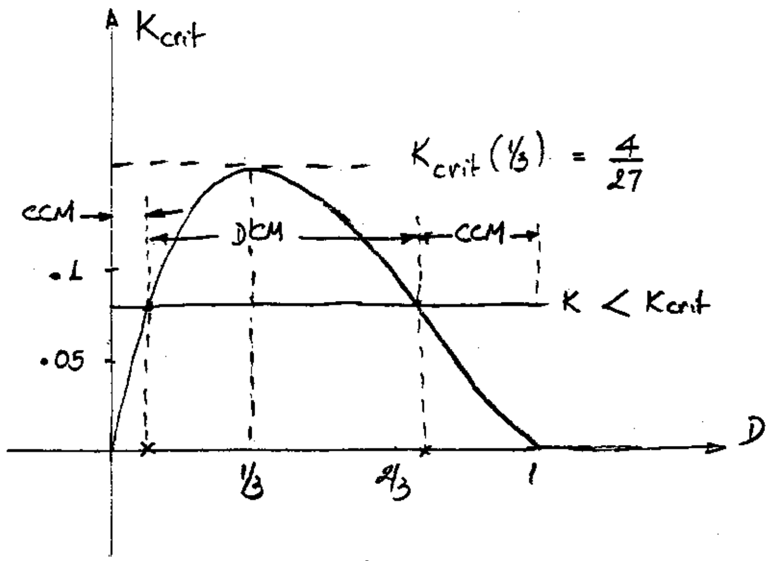
$$V = \frac{V_g}{D'} \quad \text{in CCM}$$

$$\Rightarrow \frac{V_g}{D'^2R} > \frac{DT_sV_g}{2L}$$

or $\frac{2L}{RT_s} > DD'^2$

$K > K_{crit}(D)$ for CCM

where $K = \frac{2L}{RT_s}$, $K_{crit}(D) = DD'^2$ for boost DCM occurs when $K < K_{crit}$



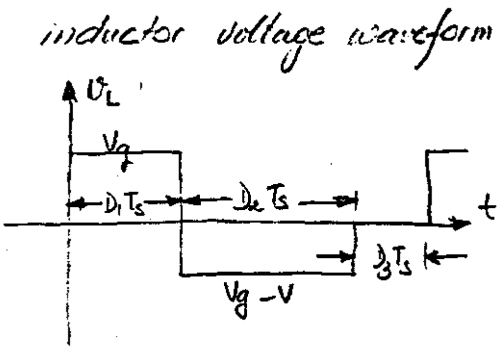
max occurs at $D = 1/3$

$\Rightarrow$ if $K > 4/27$, the converter operates in continuous mode for all D

if $K < \frac{4}{27}$, then converter operates in DCM for some middle values of D, but in CCM near $D = 0$ and $D = 1$

Determine voltage conversion ratio $\frac{V}{V_g}$

inductor voltage waveform

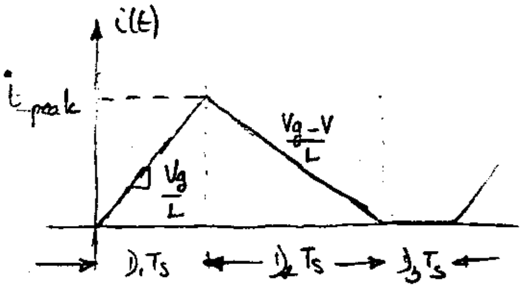


Volt-sec balance:

$$D_1 V_g + D_2 (V_g - V) + 0 = 0$$

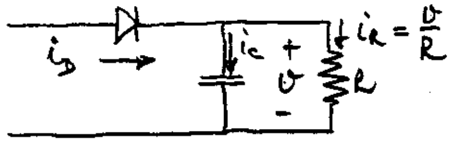
$$V = \frac{D_1 + D_2}{D_2} V_g$$

Inductor current waveform:



$$i_{peak} = \frac{V_g}{L} D_1 T_s$$

Capacitor charge balance:



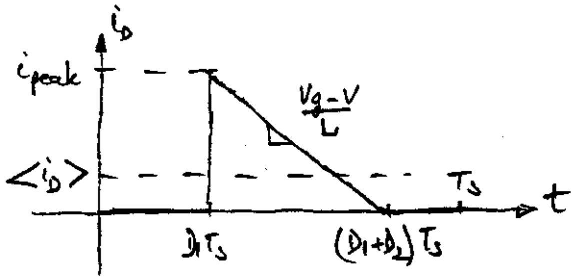
$$i_D = i_c + i_R$$

$$\langle i_c \rangle = 0$$

$$\langle i_D \rangle = \langle i_R \rangle$$

No dc current flows through C, Hence dc load current is equal to dc (average) component of diode current.

$\Rightarrow$ need to find diode current $\quad i_D = \begin{cases} 0 & 1^{st} \text{ interval} \\ i & 2^{nd} \text{ ——} \\ 0 & 3^{rd} \text{ ——} \end{cases}$



$$\langle i_D \rangle = \frac{1}{T_s}\int_0^{T_s} i_D(\tau)\,d\tau = \frac{\text{area under curve}}{T_s} = \frac{1}{T_s}\left(\frac{1}{2} i_{peak} D_2 T_s\right)$$

$$= \frac{V_g D_1 D_2 T_s}{2L}$$

Also, $\langle i_R \rangle = \frac{V}{R} \Rightarrow \langle i_D \rangle = \langle i_R \rangle$ becomes

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R}$$

We now have two unknowns and two equations:

① $V = \frac{D_1 + D_2}{D_2} V_g$ (from Volt-sec balance)

② $V = \frac{R T_s}{2L} V_g D_1 D_2$ (from charge balance)

use ① to eliminate D_2:

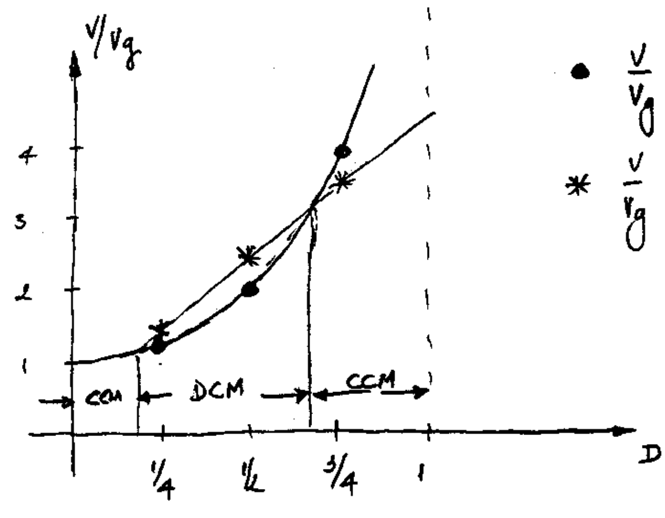
$$D_2 V = (D_1 + D_2) V_g \Rightarrow D_2 = D_1 \frac{V_g}{V - V_g} \quad \text{plug into ②}$$

$$V = \frac{V_g}{K} D_1^2 \frac{V_g}{1 - V_g} \quad \text{with } K = \frac{2L}{R T_s}$$

$$\Rightarrow V^2 - V V_g - \frac{V_g^2 D_1^2}{K} = 0 \Rightarrow V = \frac{V_g}{2} \pm \sqrt{\left(\frac{V_g}{2}\right)^2 + \frac{V_g^2 D_1^2}{K}}$$

note: from ① that $V > V_g$. take plus sign

$$\frac{V}{V_g} = M = \frac{1 + \sqrt{1 + 4D_1^2/K}}{2}$$



• $\frac{V}{V_g} = \frac{1}{D'}$

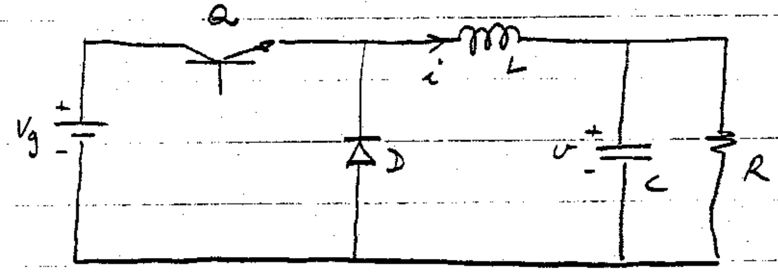
* $\frac{V}{V_g} = \frac{1 + \sqrt{1 + 4D_1^2/K}}{2}$

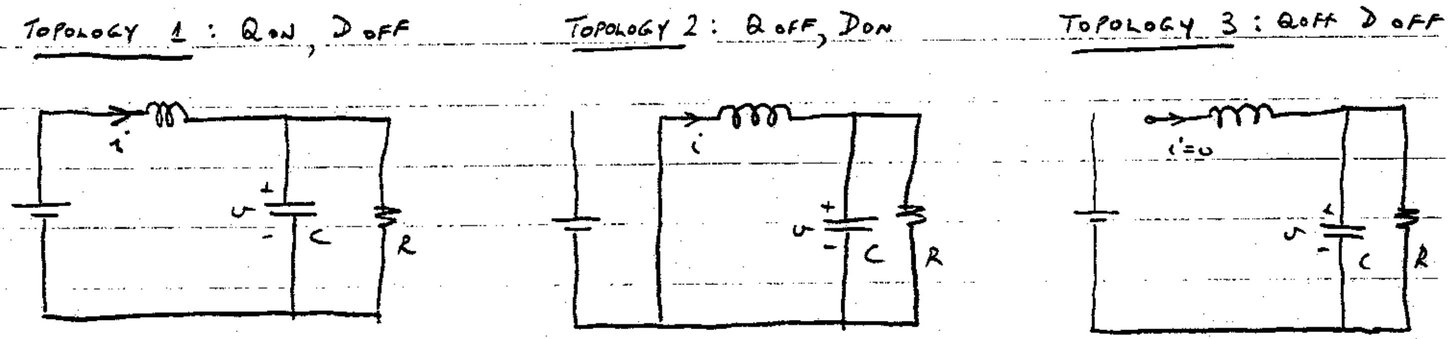
Actual gain is the larger of $1/D'$ and $\frac{1 + \sqrt{1 + 4D_1^2/K}}{2}$

R. TYMERSKI

ACCURATE DETERMINATION OF THE SWITCHING TIME FOR DCM OPERATION IN PWM CONVERTERS

A PWM CONVERTER OPERATING IN DCM CYCLES THROUGH THREE TOPOLOGIES DURING A SWITCHING PERIOD. LET US CONSIDER THE BUCK CONVERTER, WHOSE THREE TOPOLOGIES ARE SHOWN BELOW





THE CHANGE OF TOPOLOGY FROM 1 TO 2 IS DICTATED BY THE CONTROL SIGNAL TO THE TRANSISTOR, AND THEREFORE THE SWITCHING TIME IS A KNOWN QUANTITY. SIMILARLY THE CHANGE OF TOPOLOGY FROM 3 TO 1 IS ALSO DICTATED BY THE CONTROL AND IT DEFINES THE SWITCHING PERIOD. IN CONTRAST, THE CHANGE OF TOPOLOGY FROM 2 TO 3, IS DICTATED BY THE CONDITION THAT THE INDUCTOR

CURRENT REACHES ZERO. THE TIME AT WHICH THIS HAPPENS IS AN UNKNOWN QUANTITY AND NEEDS TO BE DETERMINED. THIS MAY BE DONE WITH GOOD ACCURACY BY USING THE NEWTON—RAPHSON ALGORITHM FOR THE SOLUTION OF A SET OF NONLINEAR EQUATIONS. THE DERIVATION OF THIS ALGORITHM FOR THE SINGLE VARIABLE AND MULTIVARIABLE CASES IS GIVEN IN THE APPENDIX.

NEWTON – RAPHSON ALGORITHM

THE SOLUTION TO THE (POSSIBLY MULTIVARIABLE) EQUATION

$$y(t) = 0 \tag{1}$$

CAN BE FOUND BY ITERATING THE FOLLOWING FORMULA

$$t^{(j+1)} = t^{(j)} - \left[\frac{d\,y(t)}{dt} \bigg|_{t=t^{(j)}} \right]^{-1} y\left(t^{(j)}\right) \tag{2}$$

WHERE $t^{(j)}$ REFERS TO THE jth GUESS

APPLICATION OF ALGORITHM TO SWITCHING CONVERTERS

THE DIODE (INDUCTOR) CURRENT DURING TOPOLOGY 2 CAN BE DESCRIBED BY THE OUTPUT EQUATION

$$i(t) = c_2 x(t) + d_2 V_g$$

WE WISH TO FIND THE SOLUTION OF

$$i(t) = 0 = c_2 x(t) + d_2 V_g$$

THE ALGORITHM REQUIRES FINDING THE DERIVATIVE

$$\frac{d\,i(t)}{dt} = c_2 \dot{x}(t)$$

$$= c_2 \left(A_2 x(t) + b_2 V_g \right)$$

THEREFORE, USING (2) WE CAN FIND THE SOLUTION OF THE SWITCHING TIME TO A DESIRED ACCURACY BY ITERATING THE FOLLOWING FORMULA

$$\boxed{t^{(j+1)} = t^{(j)} - \frac{c_2 x(t^{(j)}) + d_2 V_g}{c_2 \left[A_2 x(t^{(j)}) + b_2 V_g \right]}}$$

APPENDIX :

5-4-1 Newton–Raphson Algorithm for One Equation in One Unknown

Consider the equation

$$f(x) = 0 \tag{5-33}$$

and let $x = x^{(j)}$ be the jth guess.[3] We can safely assume that $x^{(j)}$ is *not* a solution, for if it were a solution, we are done.[4] Hence, $f(x^{(j)}) \neq 0$. Suppose that we obtain the Taylor expansion for $f(x)$ about the point $x = x^{(j)}$:

$$f(x) = f(x^{(j)}) + \frac{df(x)}{dx}\bigg|_{x=x^{(j)}}(x - x^{(j)}) + \frac{1}{2!}\frac{d^2f(x)}{dx^2}\bigg|_{x=x^{(j)}}(x - x^{(j)})^2 + \ldots \tag{5-34}$$

[3]Throughout this section, the jth guess is denoted by a *superscript* (j) rather than by a *subscript* as in the preceding section. The change of notation is necessary here to avoid possible confusion with the jth component of a vector, which we shall denote with a subscript.

[4]It follows from Appendix 5A that if the derivative $F'(x) = [f(x)f''(x)]/[f'(x)]^2$ of $F(x) \triangleq x - [f'(x)]^{-1}f(x)$ never vanishes for all values of x, then the Newton–Raphson algorithm $x^{(j+1)} = F(x^{(j)})$ *cannot terminate in a finite number of steps* unless the initial guess $x^{(0)} = x^*$. (This assertion does not apply to linear equations since $F'(x) = 0$ in this case. See also Problem 5-23.) Of course, it will generally take only a *finite* number of iterations to come close to the exact solution x^*. Otherwise, the algorithm would be useless!

If we let $x = x^{(j+1)}$ be the next guess, Eq. (5-34) becomes

$$f(x^{(j+1)}) = f(x^{(j)}) + \frac{df(x)}{dx}\bigg|_{x=x^{(j)}}(x^{(j+1)} - x^{(j)}) + \frac{1}{2!}\frac{d^2f(x)}{dx^2}\bigg|_{x=x^{(j)}} \times (x^{(j+1)} - x^{(j)})^2 + \ldots \tag{5-35}$$

Now suppose that we make the *not necessarily valid* assumption that the initial guess is quite *good* in the first place so that $x^{(j+1)} - x^{(j)}$ is a small number. If this assumption is indeed true, we can neglect the higher-order terms in Eq. (5-35), since the nth power of a small number is a much smaller number, for $n \geq 2$. In this case, Eq. (5-35) can be approximated by

$$f(x^{(j+1)}) \approx f(x^{(j)}) + \frac{df(x)}{dx}\bigg|_{x=x^{(j)}}(x^{(j+1)} - x^{(j)}) \tag{5-36}$$

Our objective is to choose $x^{(j+1)}$ so that it is a solution of Eq. (5-33). Hence, if our preceding assumption is valid, $x^{(j+1)}$ should obviously be chosen so that $f(x^{(j+1)}) = 0$. Equating Eq. (5-36) to zero and solving for $x^{(j+1)}$, we obtain the desired "recipe":

$$\boxed{x^{(j+1)} = x^{(j)} - [J(x^{(j)})]^{-1}f(x^{(j)})} \tag{5-37}$$

where

$$[J(x^{(j)})]^{-1} \triangleq \left[\frac{df(x)}{dx}\bigg|_{x=x^{(j)}}\right]^{-1} \tag{5-38}$$

Equation (5-37) can now be identified as the *Newton–Raphson equation* derived earlier in (5-29). If our earlier assumption, which led to the derivation of Eq. (5-37) is valid, this algorithm will converge. It is proved in Appendix 5A that, if the initial guess $x^{(0)}$ is sufficiently close to *a correct* solution x^* of Eq. (5-33), then the Newton–Raphson algorithm will *always* converge to x^*. Before proceeding, it will be instructive to present a *geometrical interpretation* of this algorithm. A typical curve representing $y = f(x)$ is shown in Fig. 5-6(a). If we let $P^{(j)}$ represent the point on the curve corresponding to $f(x^{(j)})$, the slope of the tangent drawn through this point is equal to

$$J(x^{(j)}) = \frac{df(x)}{dx}\bigg|_{x=x^{(j)}} \tag{5-39}$$

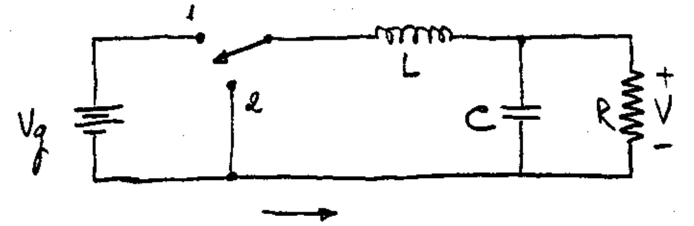
Hence, the next guess $x^{(j+1)}$ is simply the distance from the origin to the point of intersection between the x-axis and the tangent from $P^{(j)}$. The next point $P^{(j+1)}$ is therefore the intersection of this curve and the vertical line drawn through $x = x^{(j+1)}$, as shown in Fig. 5-6(a). By repeating this procedure, we find the iteration rapidly approaches point Q, which is the correct solution. To show that the Newton–Raphson algorithm may not converge, consider the curve shown in Fig. 5-6(b). There are two solutions in this case corresponding to points Q_a and Q_b. An initial guess corresponding to point P_a will eventually converge to point Q_a, and an initial guess corresponding to point P_b will eventually converge to point Q_b. However, an initial guess at point P_c will cause the iteration to simply oscillate around the loop without ever

Lecture : Switched-Mode Converter Topologies.

We have already analyzed the operation of a number of different types of converters: Buck, boost, buck-boost and Ćuk. With these converters, a number of different functions can be performed: Step down of Voltage, step up or inversion of polarity while stepping down or up.

Where do these converters come from? What other converters occur, and what other functions can be obtained? What are the basic relations between converters?

The simplest and most basic converter is the buck:



Switch in position 1 during $0 \le t \le DT_s$

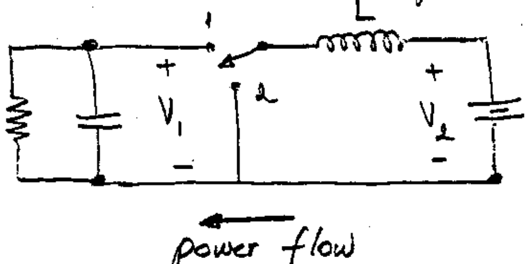
—— " —— 2 during $DT_s \le t \le T_s$

$$\frac{V}{V_g} = D$$

Inversion of Source and load

Reverse position of load R (bypassed by capacitor) with the Source V_g. Also, realize ideal switch with transistors and diodes such that power can flow in opposite direction.

Result: A new converter whose conversion ratio V/V_g is the reciprocal of the original case.



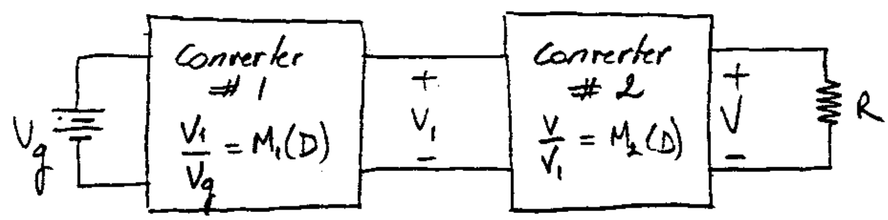
$V_2 = D V_1$ (position 1)

$V_1 = \frac{1}{D} V_2$ (position 2)

Inversion of buck converter yields boost converter

Cascade connection of converters

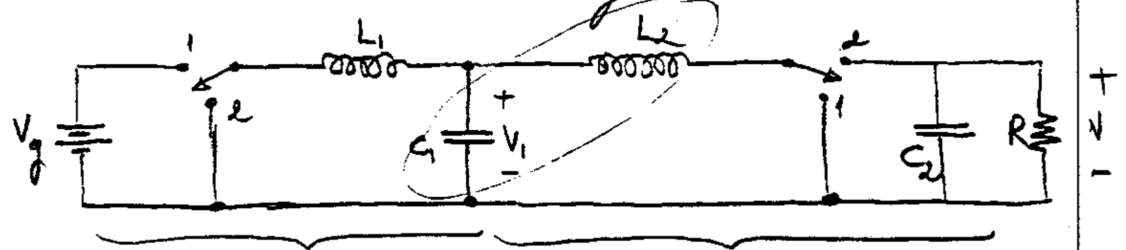
Connect two converters in series.



Result: conversion ratio $M(D) = \frac{V}{V_g}$ of composite converter is product of individual conversion ratios:

$$M(D) = M_1(D)\, M_2(D)$$

Example 1: Buck cascaded by boost



Buck Converter

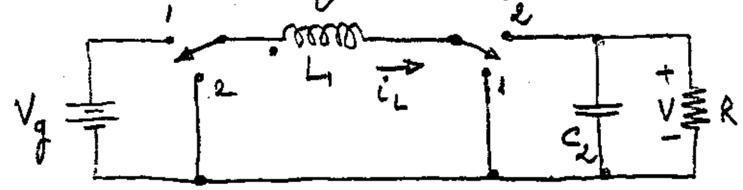
$$\frac{V_1}{V_g} = D$$

Boost Converter

$$\frac{V}{V_1} = \frac{1}{D'} = \frac{1}{1-D}$$

$$\Rightarrow \frac{V}{V_g} = \frac{D}{D'}$$

Note that C_1 and L_2 are not necessary: the three-section filter may be reduced to a single-section filter containing L_1 only:



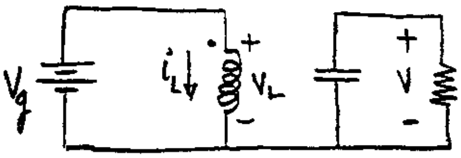
$$\frac{V}{V_g} = \frac{D}{D'}$$ Noninverting buck-boost

$\langle v_L \rangle = 0$

$DT_sV_g + D'(-V) = 0$

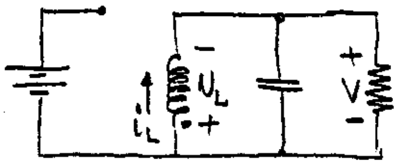
$$\frac{V}{V_g} = \frac{D}{D'}$$

Switch in position 1



$V_L = V_g$

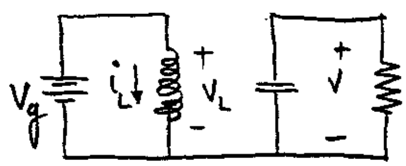
position 2



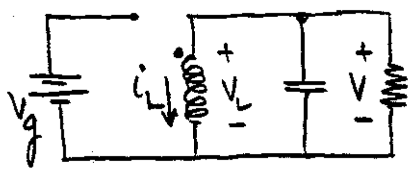
$V_L = -V$

To obtain a negative output, reverse polarity of inductor during second interval (switches in position 2). This also reduces the number of switches necessary:

Position 1

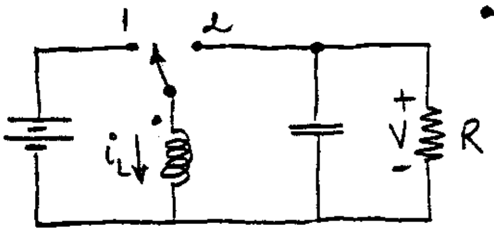


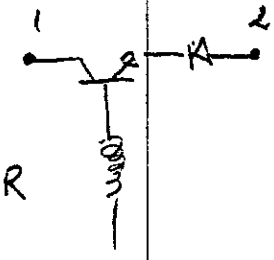
position 2



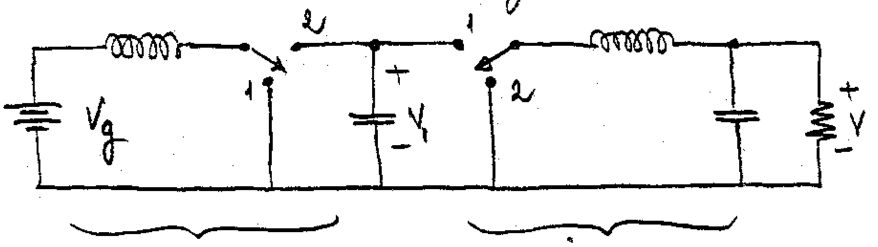
Buck-boost converter

$$\frac{V}{V_g} = -\frac{D}{D'}$$





Example 2 Boost cascaded by buck



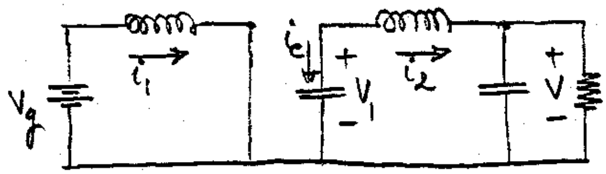
boost converter buck converter

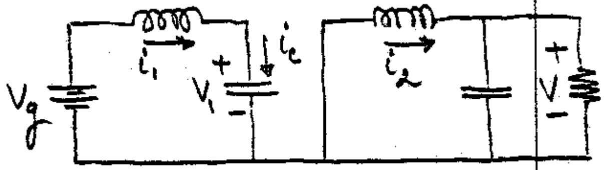
$$\frac{V_1}{V_g} = \frac{1}{D'} \qquad \frac{V}{V_1} = D$$

Noninverting Cuk converter

Composite dc conversion ratio $\frac{V}{V_g} = \frac{D}{D'}$

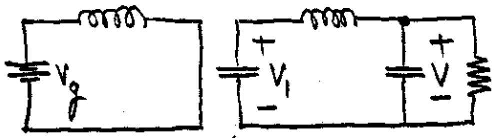
position 1 position 2

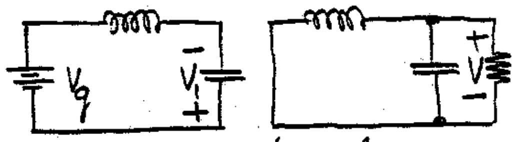




$$i_c = -i_2 \qquad i_c = i_1$$

By analogy with the buck-boost derivation, a negative output can be obtained by reversal of the capacitor polarity (V_1) during the second interval (position 2). Again, this also reduces the number of switches:

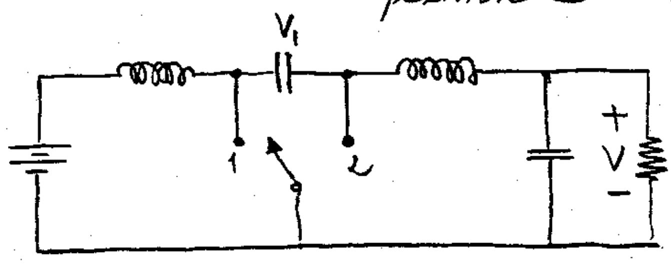




position 1 position 2

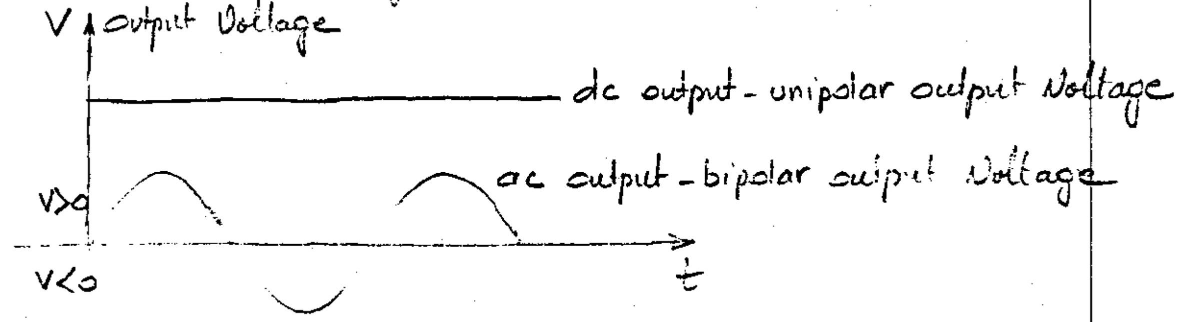
Cuk Converter

$$\frac{V}{V_g} = -\frac{D}{D'}$$



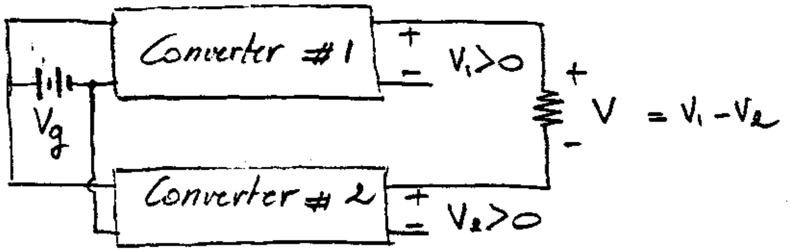
AC output - Differential Connection of load

In many applications an ac output is required, and hence a converter is needed which is capable of producing an output voltage of either polarity.



Of the converters we have studied so far, the buck and boost can produce only a positive unipolar output voltage, while the buck-boost and Cuk produce a negative unipolar output. How can we obtain a bipolar output?

One widely-used technique for obtaining a bipolar output is the differential connection of the load across the output of two known converters:



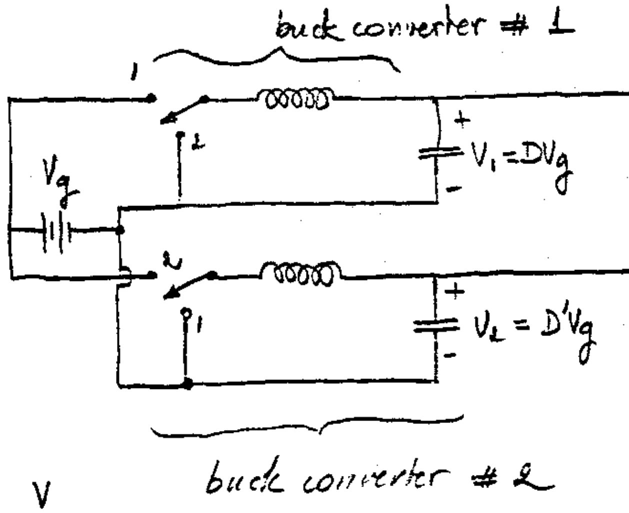
Output voltage $V = V_1 - V_2$

note V is bipolar:

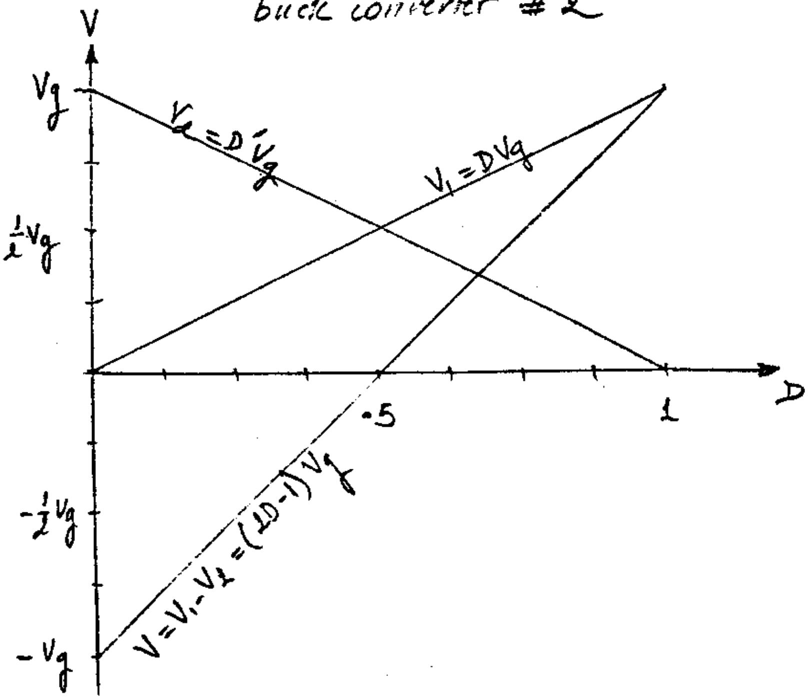
$V > 0$ if $V_1 > V_2$

$V < 0$ if $V_1 < V_2$

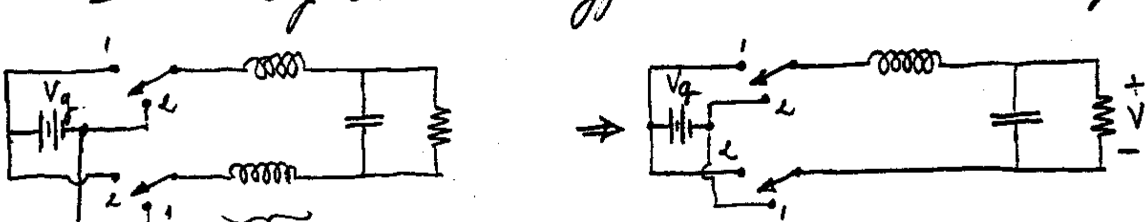
Example 8: Differential connection of load across output of two buck converters



$$V = V_1 - V_2$$
$$= DV_g - D'V_g$$
$$= (2D-1)\,V_g$$



It is usually desired to bypass the load with a capacitor:

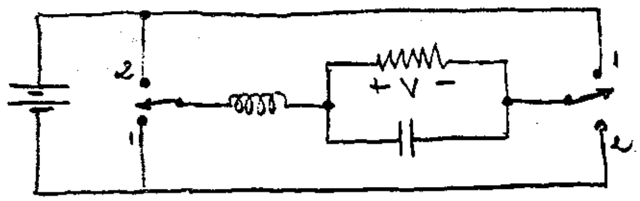


The two inductors are now redundant

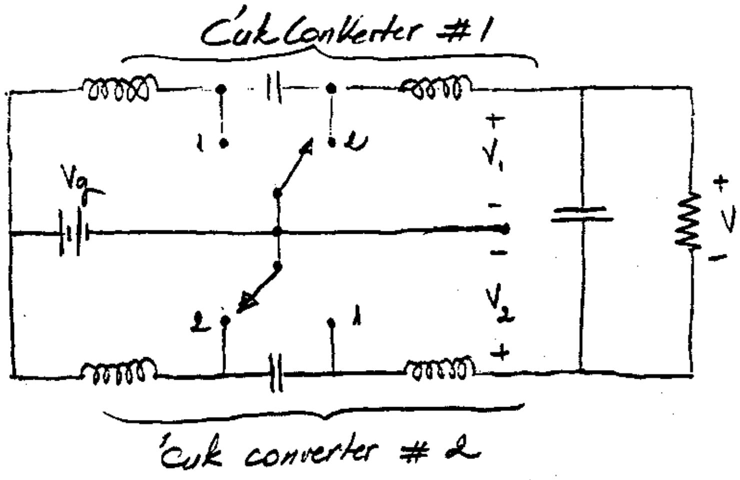
Re-draw for clarity:

Bridge converter

$$\frac{V}{V_g} = 2D - 1$$



Example 4 Differential connection of load across outputs of two Ćuk converters



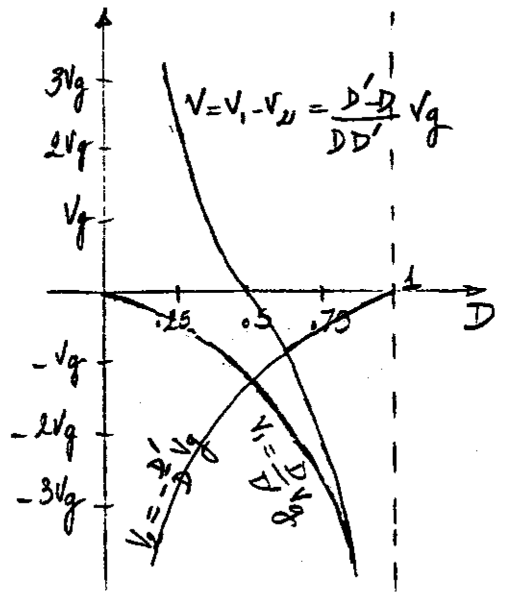
Ćuk Amplifier

$$V_1 = -\frac{D}{D'} V_g$$

$$V_2 = -\frac{D'}{D} V_g$$

$$V = V_1 - V_2 = \left[-\frac{D}{D'} + \frac{D'}{D}\right] V_g$$

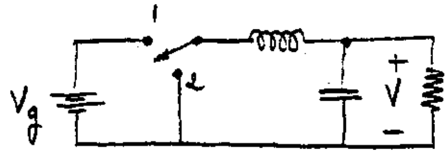
$$V = \frac{D' - D}{D D'} V_g$$

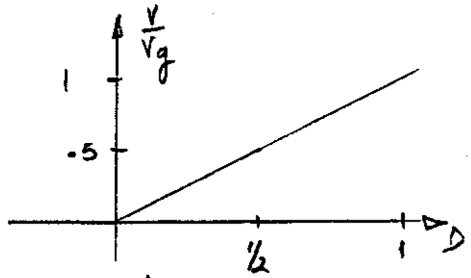


The Class of Single-inductor, Single output converters

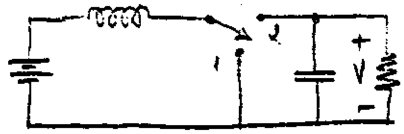
Converters well-suited for dc-dc applications.

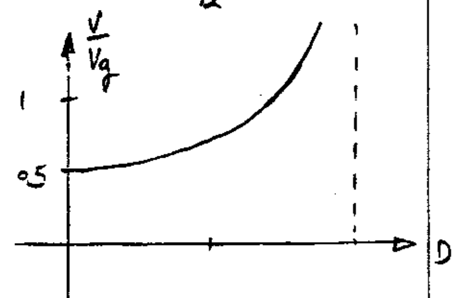
1- Buck $V/V_g = D$



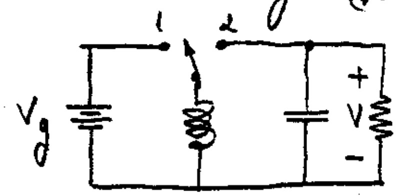


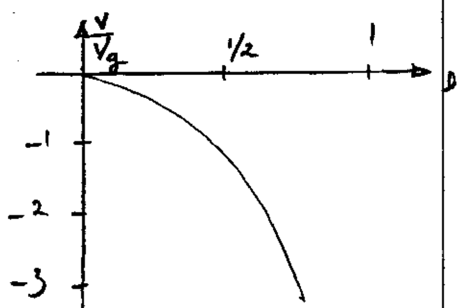
2- Boost $V/V_g = \frac{1}{1-D}$





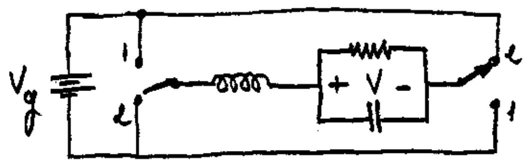
3- Buck-boost $\frac{V}{V_g} = \frac{-D}{(1-D)}$

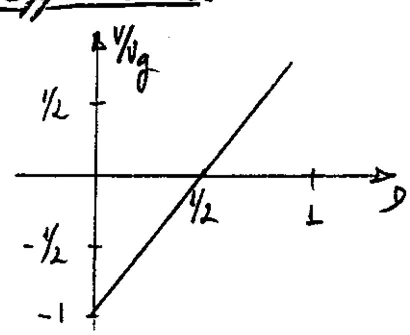




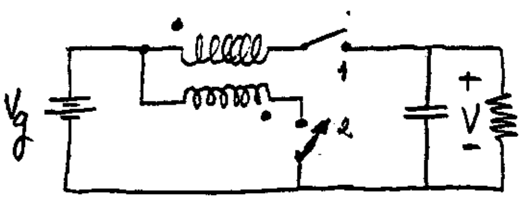
Converters well-suited for dc-ac applications

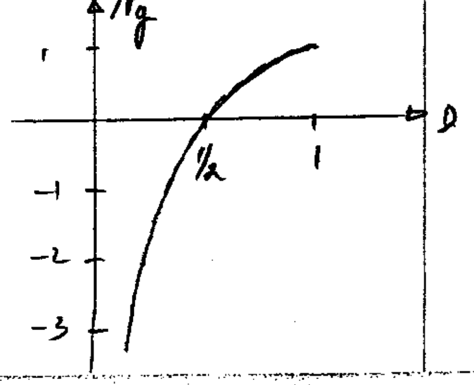
4- Bridge $\frac{V}{V_g} = 2D-1$





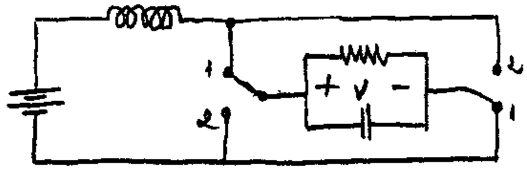
5- Watkins-Johnson $\frac{V}{V_g} = \frac{2D-1}{D}$

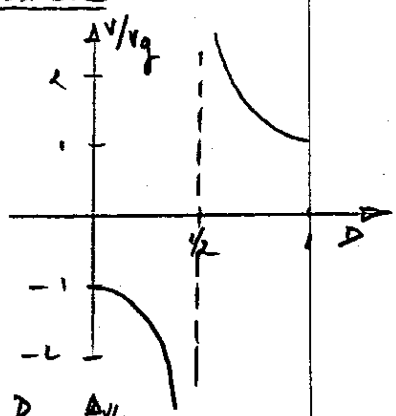




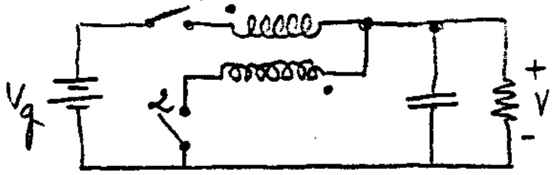
Converters well-suited for dc-dc applications

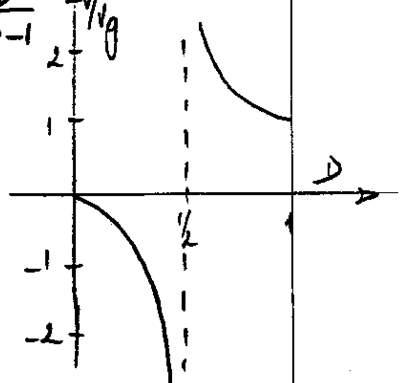
6- Current-fed bridge $\frac{V}{V_g} = \frac{1}{2D-1}$





7- Inversion of Watkins-Johnson $\frac{V}{V_g} = \frac{D}{2D-1}$

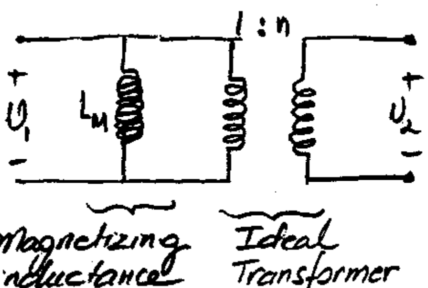




Isolation Transformers

In a large number of applications, it is desired to incorporate a transformer into a switching converter, to obtain dc isolation and a turn ratio. The same analysis techniques can be applied to these isolated converters, but one must model the transformer:

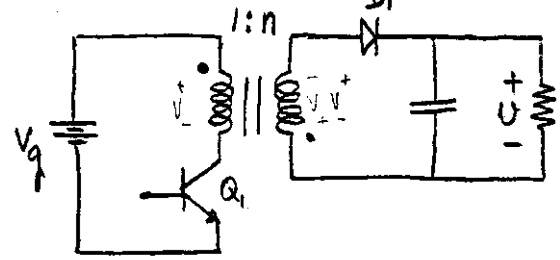
A suitable 1st order model:



- L_M models flux inside core of transformer
- Can apply Volt-second balance to L_M

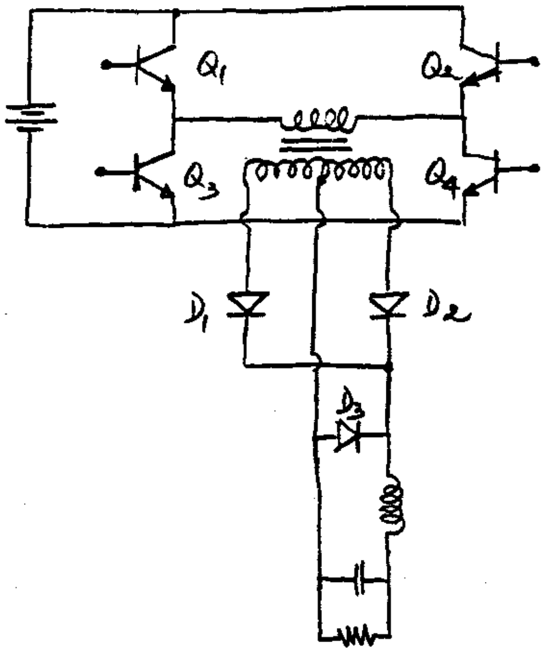
Some converters which incorporate isolation transformers:

1 - Flyback converter based on buck-boost converter



Interval	Q_1	D_1
DT_s	ON	OFF
$D'T_s$	OFF	ON

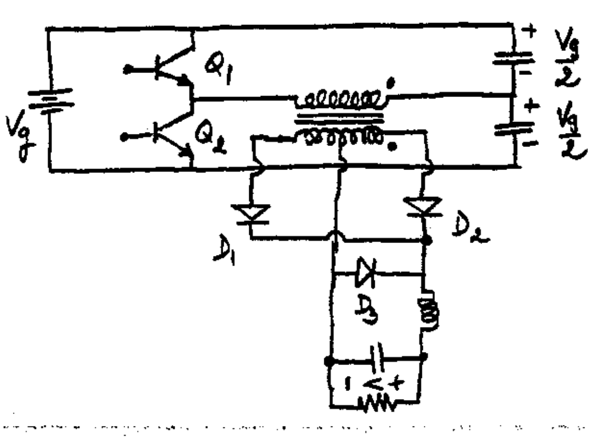
2 - Full Bridge converter: based on buck converter
(not the same as the bridge converter derived on p. 8)



Interval	Conducting devices
DT_s	Q_1, Q_4, D_1
$D'T_s$	D_3
DT_s	Q_2, Q_3, D_2
$D'T_s$	D_3

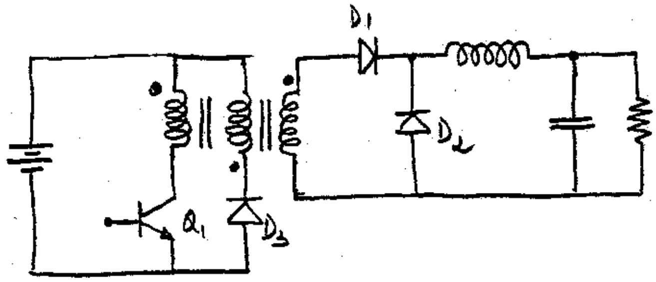
D_3 may be omitted then D_1 and D_2 conduct simultaneous during interval $D'T_s$

3. Half - Bridge Converter (based on buck converter)



Interval	Conducting devices
DT_s	Q_1, D_1
$D'T_s$	D_3
DT_s	Q_2, D_2
$D'T_s$	D_3

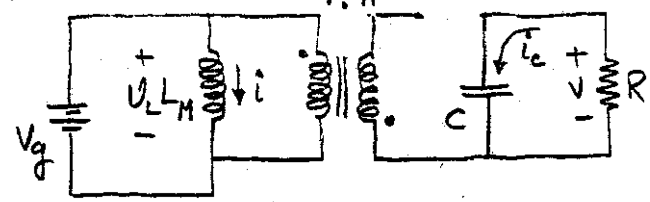
4. forward Converter (based on buck converter)



Interval	Conducting Devices
DT_s	Q_1, D_1
$D'T_s$: $D_2 T_s$	D_2, D_3
$D'T_s$: $D_3 T_s$	D_2

<u>Example</u> - Flyback converter in continuous conduction mode

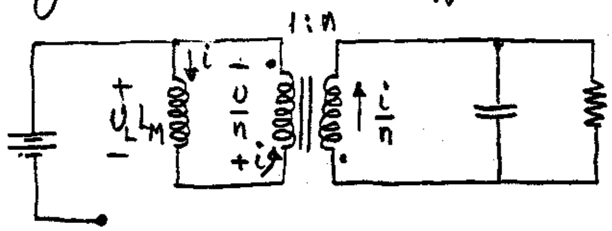
During DT_s transistor on, diode off



$$v_L = L\frac{di}{dt} = v_g$$

$$i_c = C\frac{dv}{dt} = -\frac{v}{R} \simeq -\frac{V}{R}$$

During $D'T_s$ transistor off, diode on



$$v_L = -\frac{v}{n} \simeq -\frac{V}{n}$$

$$i_c = \frac{i}{n} - \frac{v}{R} \simeq \frac{I}{n} - \frac{V}{R}$$

Volt-Sec balance on L_M :

$$D(V_g) + D'\left(-\frac{V}{n}\right) = 0$$

$$\Rightarrow \boxed{\frac{V}{V_g} = n\frac{D}{D'}}$$

Charge balance on C :

$$D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0$$

$$\Rightarrow \boxed{I = \frac{nV}{D'R}}$$

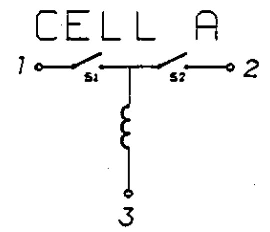
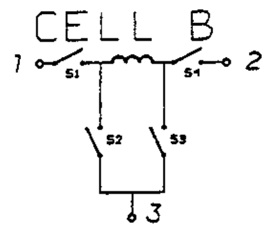
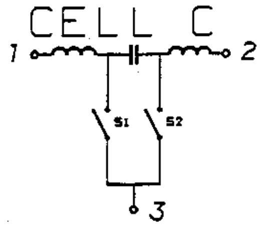
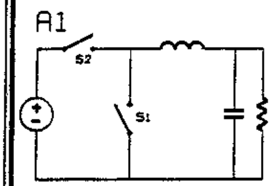
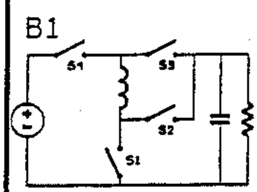
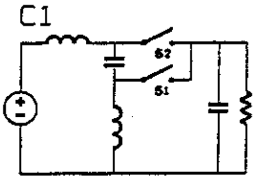
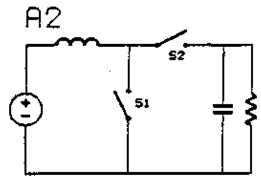
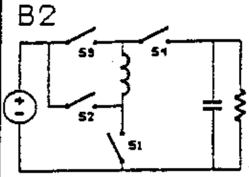
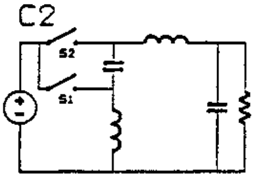
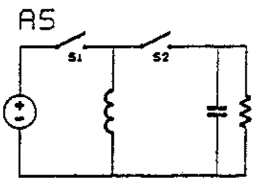
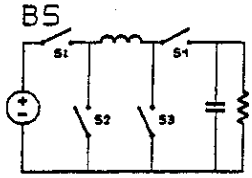
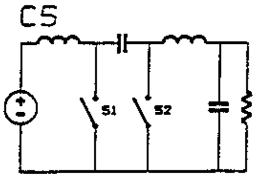
CONFIG.	CELL A	CELL B	CELL C
			
1	 S2 : $M = D$	 1) S2,S4(D < 0.5) $M = \frac{D}{2D - 1}$ 2) S1,S3(D < 0.5) $M = \frac{D'}{1 - 2D}$	 S2 : $M = D$
2	 S1 : $M = \frac{1}{D'}$	 1) S2,S4(D > 0.5) $M = \frac{2D - 1}{D}$ 2) S1,S3(D > 0.5) $M = \frac{1 - 2D}{D'}$	 S1 : $M = \frac{1}{D'}$
3	*THE SAME AS 1 ABOVE*	*THE SAME AS 1 ABOVE*	*THE SAME AS 1 ABOVE*
4	*THE SAME AS 2 ABOVE*	*THE SAME AS 2 ABOVE*	*THE SAME AS 2 ABOVE*
5	 S1 : $M = -\frac{D}{D'}$	 S1, S3 : $M = \frac{D}{D'}$	 S1 : $M = -\frac{D}{D'}$
6	*THE SAME AS 5 ABOVE*	*THE SAME AS 5 ABOVE*	*THE SAME AS 5 ABOVE*

Table 2. *The converter-cell generated families of converters. See the text for an explanation of the active switch/conversion gain (M) entries in the table.*

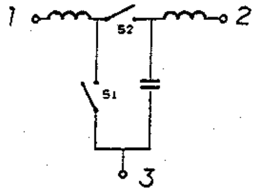
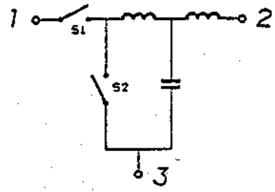
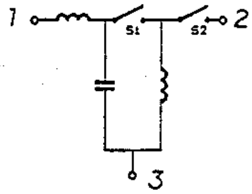
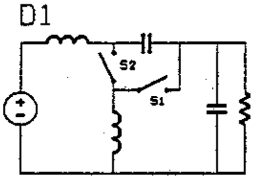
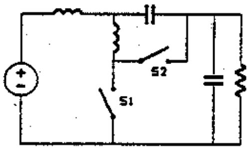
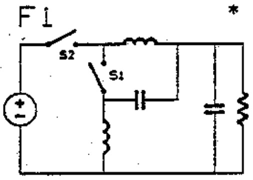
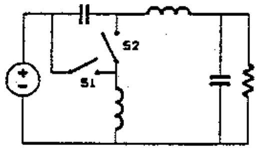
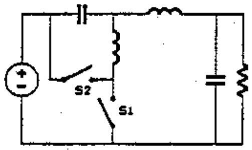
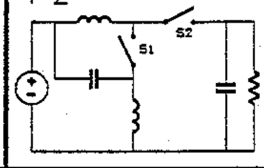
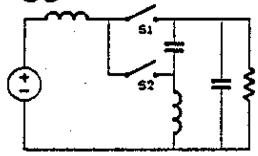
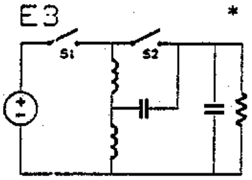
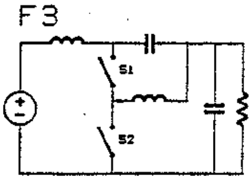
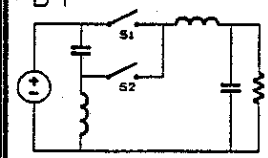
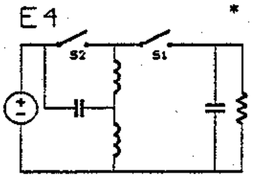
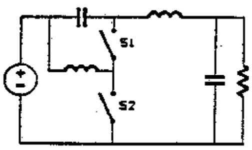
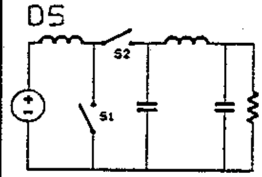
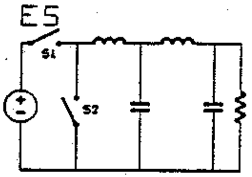
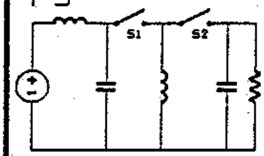
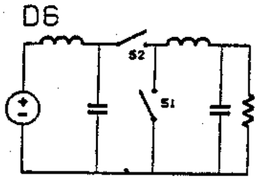
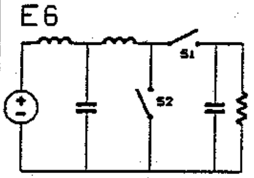
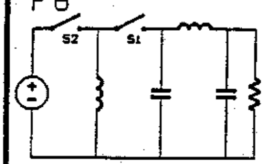
CONFIG.	CELL D	CELL E	CELL F
			
1	D1  S2 : $M = -\frac{D}{D'}$	E1  S1 : $M = \frac{1}{D'}$	F1 *  S2 : $M = D$
2	D2  S1 : $M = -\frac{D}{D'}$	E2  S2 : $M = D$	F2 *  S1 : $M = \frac{1}{D'}$
3	D3  S2 : $M = \frac{1}{D'}$	E3 *  S1 : $M = -\frac{D}{D'}$	F3  S1 : $M = D$
4	D4  S1 : $M = D$	E4 *  S2 : $M = -\frac{D}{D'}$	F4  S2 : $M = \frac{1}{D'}$
5	D5  S1 : $M = \frac{1}{D'}$	E5  S1 : $M = D$	F5  S1 : $M = -\frac{D}{D'}$
6	D6  S2 : $M = D$	E6  S2 : $M = \frac{1}{D'}$	F6  S2 : $M = -\frac{D}{D'}$

Table 2 (cont'd).

* *The LC branch connected from source to ground or from sink to ground is redundant in these converters.*

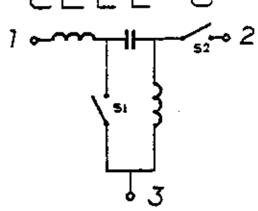
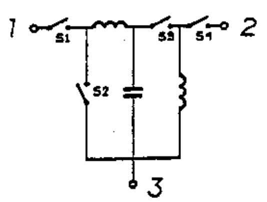
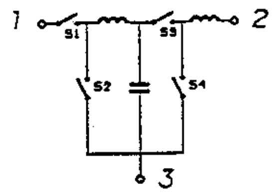
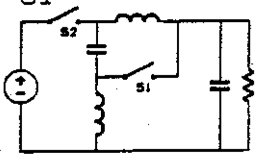
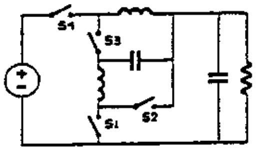
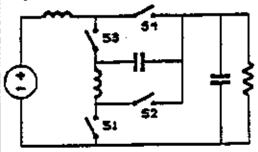
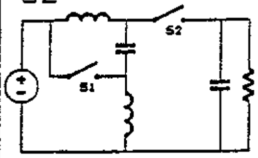
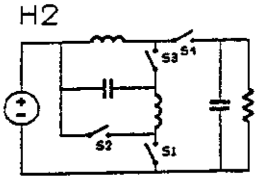
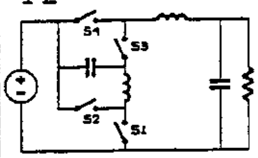
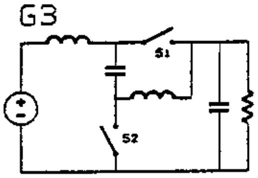
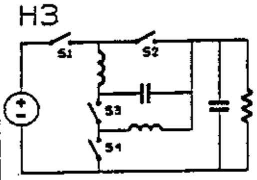
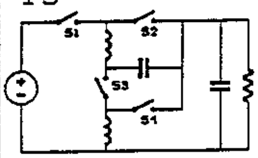
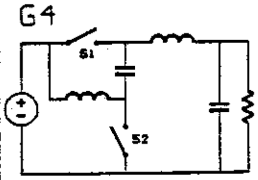
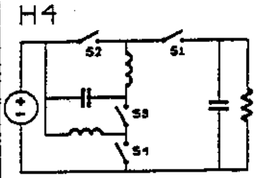
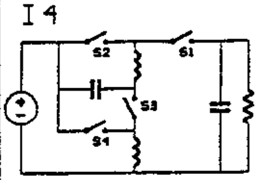
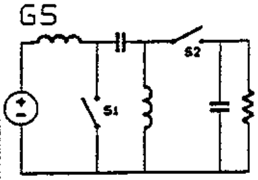
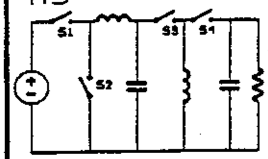
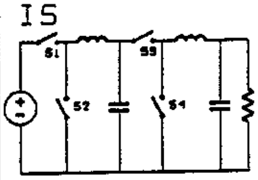
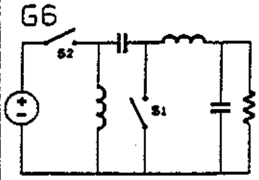
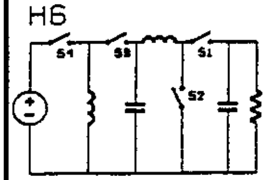
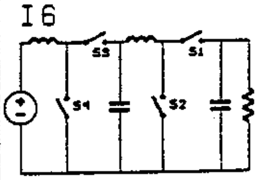
CONFIG.	CELL G	CELL H	CELL I
			
1	G1  1) S2 ($D < 0.5$): $M = \frac{D}{2D-1}$ 2) S1 ($D < 0.5$): $M = \frac{D'}{1-2D}$	H1  1) S2,S4 : $M = \frac{D}{D + D'^2}$ 2) S1,S4 : $M = \frac{1}{1 + D'}$	I1  1) S1,S3 : $M = \frac{1}{1 - D^2}$ 2) S1,S4 : $M = \frac{1}{1 - DD'}$
2	G2  1) S1 ($D > 0.5$): $M = \frac{1-2D}{D'}$ 2) S2 ($D > 0.5$): $M = \frac{2D-1}{D}$	H2  1) S1,S3 : $M = \frac{D' + D^2}{D'}$ 2) S2,S3 : $M = 1 + D$	I2  1) S2,S4 : $M = 1 - D'^2$ 2) S1,S4 : $M = 1 - DD'$
3	G3  1) S1 ($D < 0.5$): $M = \frac{D}{2D-1}$ 2) S2 ($D < 0.5$): $M = \frac{D'}{1-2D}$	H3  1) S1,S3 : $M = \frac{D^2}{D' + D^2}$ 2) S1,S4 : $M = \frac{D'}{1 + D'}$	I3  1) S1,S3 : $M = \frac{D^2}{D^2 - 1}$ 2) S1,S4 : $M = \frac{DD'}{DD' - 1}$
4	G4  1) S2 ($D > 0.5$): $M = \frac{1-2D}{D'}$ 2) S1 ($D > 0.5$): $M = \frac{2D-1}{D}$	H4  1) S2,S4 : $M = \frac{D + D'^2}{D'^2}$ 2) S1,S4 : $M = \frac{1 + D'}{D'}$	I4  1) S2,S4 : $M = \frac{D'^2 - 1}{D'^2}$ 2) S1,S4 : $M = \frac{DD' - 1}{DD'}$
5	G5  S1 : $M = \frac{D}{D'}$	H5  1) S1,S3 : $M = -\frac{D^2}{D'}$ 2) S1,S4 : $M = -D'$	I5  1) S1,S3 : $M = D^2$ 2) S1,S4 : $M = DD'$
6	G6  S2 : $M = \frac{D}{D'}$	H6  1) S2,S4 : $M = -\frac{D}{D'^2}$ 2) S1,S4 : $M = -\frac{1}{D'}$	I6  1) S2,S4 : $M = \frac{1}{D'^2}$ 2) S1,S4 : $M = \frac{1}{DD'}$

Table 2 (cont'd).

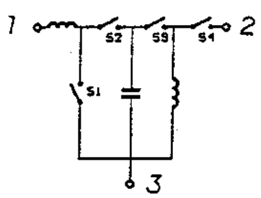
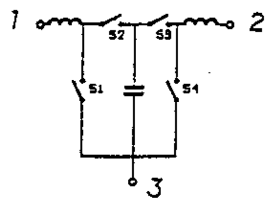
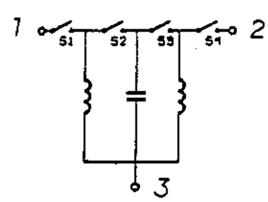
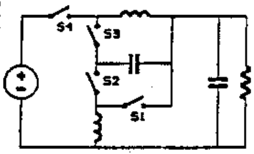
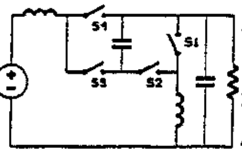
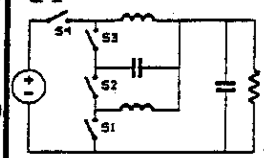
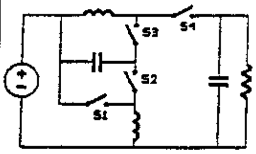
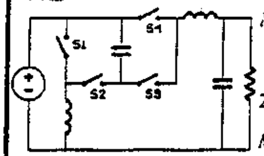
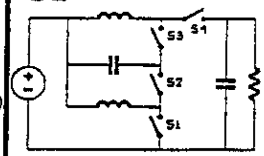
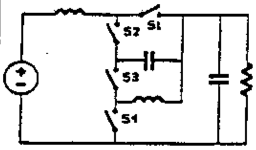
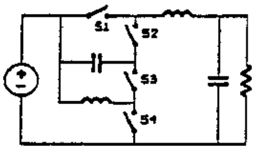
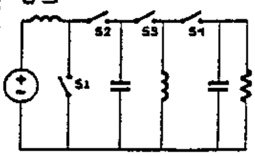
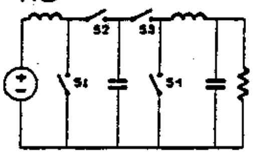
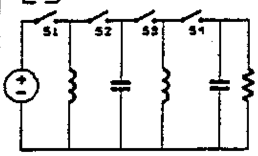
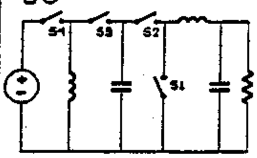
CONFIG.	CELL J	CELL K	CELL L
			
1	J1  S2,S4 : $M = \frac{D^2}{D' + D^2}$	K1  1) S1,S3(D < 0.5) $M = \frac{D'}{1 - 2D}$ 2) S2,S4(D < 0.5) $M = \frac{D}{2D - 1}$	L1  1) S2,S4(D < 0.5) $M = \frac{D^2}{2D - 1}$ 2) S1,S3(D < 0.5) $M = \frac{D'^2}{1 - 2D}$
2	J2  S1,S3 : $M = \frac{D + D'^2}{D'^2}$	K2  1) S1,S3(D > 0.5) $M = \frac{1 - 2D}{D'}$ 2) S2,S4(D > 0.5) $M = \frac{2D - 1}{D}$	L2  1) S1,S3(D > 0.5) $M = \frac{1 - 2D}{D'^2}$ 2) S2,S4(D > 0.5) $M = \frac{2D - 1}{D^2}$
3	J3  S1,S3 : $M = \frac{D}{D + D'^2}$	*THE SAME AS 1 ABOVE*	*THE SAME AS 1 ABOVE*
4	J4  S2,S4 : $M = \frac{D' + D^2}{D'}$	*THE SAME AS 2 ABOVE*	*THE SAME AS 2 ABOVE*
5	J5  S1,S3 : $M = -\frac{D}{D'^2}$	K5  S1,S3 : $M = \frac{D}{D'}$	L5  S1,S3 : $M = \left(\frac{D}{D'}\right)^2$
6	J6  S2,S4 : $M = -\frac{D^2}{D'}$	*THE SAME AS 5 ABOVE*	*THE SAME AS 5 ABOVE*

Table 2 (cont'd).

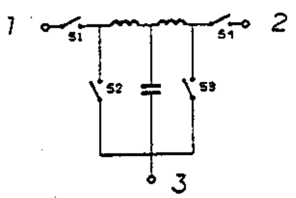
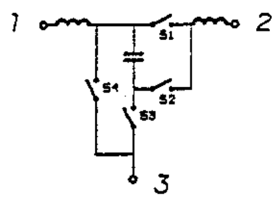
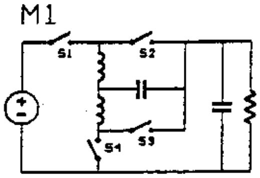
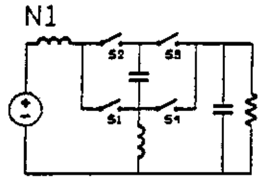
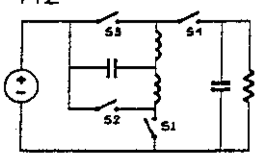
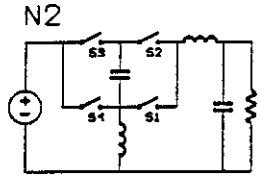
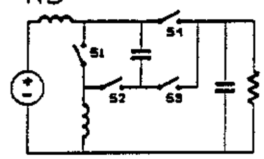
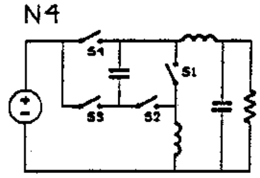
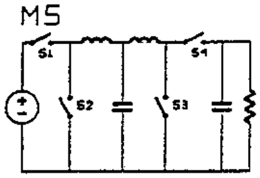
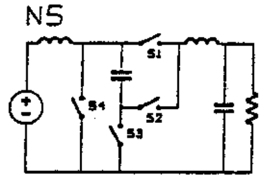
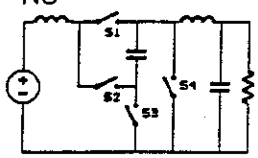
CONFIG.	CELL M 	CELL N 
1	M1  1) S1,S3(D < 0.5) $M = \frac{D}{2D - 1}$ 2) S2,S4(D < 0.5) $M = \frac{D'}{1 - 2D}$	N1  S1,S3 (D < 0.5): $M = \frac{D}{D'}$
2	M2  1) S2,S4(D > 0.5) $M = \frac{2D - 1}{D}$ 2) S1,S3(D > 0.5) $M = \frac{1 - 2D}{D'}$	N2  S2,S4 (D > 0.5): $M = \frac{D}{D'}$
3	*THE SAME AS 1 ABOVE*	N3  S2,S4 (D > 0.5): $M = \frac{2D - 1}{D}$
4	*THE SAME AS 2 ABOVE*	N4  S1,S3 (D < 0.5): $M = \frac{D'}{1 - 2D}$
5	M5  S1,S3 : $M = \frac{D}{D'}$	N5  S2,S4 (D > 0.5): $M = \frac{1 - 2D}{D'}$
6	*THE SAME AS 5 ABOVE*	N6  S1,S3 (D < 0.5): $M = \frac{D}{2D - 1}$

Table 2 (cont'd).

17

BASICS OF SWITCHED-MODE POWER CONVERSION: TOPOLOGIES, MAGNETICS, AND CONTROL

ABSTRACT

Switched-mode power conversion emerged recently as an interdisciplinary field which requires a fundamental knowledge in three areas: power circuit configurations, control systems, and magnetic circuits. A tutorial review of basic switched-mode power conversion topologies, properties, and simple analysis methods is given first. Principles of magnetic circuit analysis treated next, provide better understanding of power inductor and power transformer design requirements. Closing the feedback loop in pulse-width modulated (pwm) systems requires basic understanding of dc-to-dc converter dynamics, and so the accompanying transfer functions and frequency response methods are also reviewed. With these basic building blocks well understood, the sophisticated and complex structures of modern electronic power processing systems may be more easily and reliably designed.

1. INTRODUCTION

The practicing engineers in the Power Electronics field today are faced with an unusual challenge. Their everyday job requires expertise in three fundamental areas of electrical engineering: classical power conversion methods, magnetic circuit designs, and control system techniques. Traditionally, each of those areas might be considered as a specialty in its own right, requiring considerable effort to master it. Thus, this review paper is an attempt to ease these difficulties for novices to the field by introducing them to the fundamentals in each of the three key areas: topologies, magnetics and control. For the reader of this two volume book, the purpose of this paper is to build the bridge toward better understanding of the advanced concepts presented in follow-up scientific papers [1 - 16, 18 - 30] which constitute this two volume book.

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In Section 2, the fundamental reasoning for changing to switching conversion technology from the classical linear (dissipative) power conversion control is presented.

Fundamental conversion topologies reviewed by Section 3 include buck, boost, buck-boost and Ćuk converters. Along the converter topology development many topics are introduced at appropriate places where they can be easily understood: dc analysis through volt-sec balance on inductors, two modes of operation (continuous and discontinuous conduction), efficiency evaluation in presence of component nonidealities, dc isolation and multiple output extensions, two-quadrant (battery charger/discharger) and four-quadrant (switched-mode amplifier and ac uninterruptible power supplies) converter classification.

The Section 4 on magnetics fundamentals reviews the key results pertinent to the understanding and design of inductors and transformers for switching power conversion applications: analogy of magnetic circuits with electric circuits and reluctance concept, effect of the airgap on the inductor flux-current characteristic, inductors with dc bias, transformer operation and modelling, transformer design with no dc bias and some simplified design procedure for inductor and transformer core selection using area product or core geometry [43] approach.

Modelling of switching-mode regulator and its control transfer properties (loop gain) are reviewed in Section 5 on a very fundamental level, which demonstrates very simple models of the nonlinear converter power stage and separately linear modulator transfer properties.

2. POWER CONVERSION ALTERNATIVES

Two alternatives for delivery of electric power from a dc source to a load in a controllable manner are linear and switched-mode power conversion. They are illustrated in Fig. 1, reduced to their simplest forms.

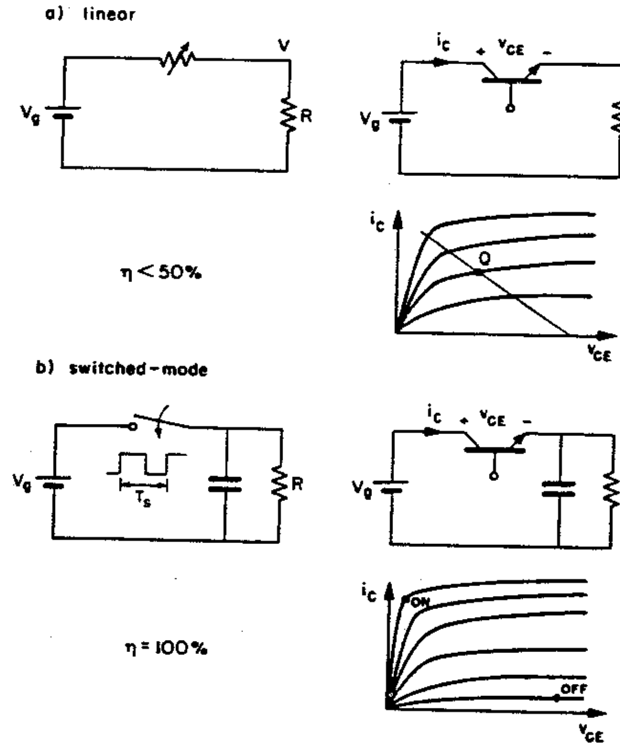

Fig. 1. *Comparison of linear (dissipative) (a) and switched-mode (nondissipative) (b) power conversion.*

Linear power conversion (Fig. 1a) relies on the presence of a series linear element, either a resistor (mechanical control), or a transistor used in the linear mode, (electronic control) such that the total load current is passed through the series linear element. Therefore, the greater the difference between the input and output voltages (the higher the controlling power range) the more power is lost in the controlling device. Thus, linear power conversion even in its ideal form is dissipative and inefficient, typically in the 30-60% efficiency range.

In switched-mode power conversion, (Fig. 1b) however, the controlling device is an ideal switch, which is either closed or open. Then by controlling the ratio of the time intervals spent in the closed and open position (often defined as duty ratio), the power flow to the load can be controlled in a very efficient way. Namely, ideally it is 100% efficient even for a wide range of power being controlled. However, in practice it is reduced somewhat owing to nonideal realization of the switch. Nevertheless the semiconductor device (bipolar transistor, for example) is clearly used in a much more efficient way. When the device is fully ON it has only a small saturation voltage drop across it (typically 0.3V to 1V). In the OFF condition, the reverse leakage current is usually negligible, so that the power loss is negligible despite the fact that the blocking voltage across it may be high. However, the output voltage is far from being dc as in the linear example, and pulsed power is applied. Although this may be acceptable for some applications such as oven heating, in many other uses a constant dc output voltage is desired. The power flow to the load may be easily smoothed out by the addition of a low-pass LC filter.

We therefore reach two important conclusions: *Efficient electric power conversion and control requires the use of switches as its basic components. The need to generate dc output voltage introduces ideally lossless storage components, inductors, and capacitors whose role is to smooth out the inherent pulsating behavior originating from the switching action.*

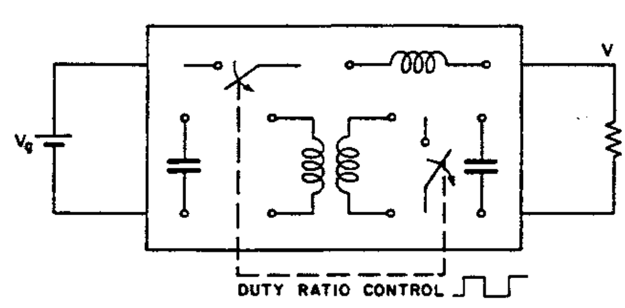

Fig. 2. *General switched-mode power conversion consists of storage components and switches arranged in a topology which has effective low-pass filter nature.*

Thus, in general, efficient switched-mode power conversion may be postulated as in Fig. 2. Note the addition of the transformer as a component which provides an often very important practical requirement, dc isolation between input and output grounds. In Fig. 2, the storage components and switches are purposely shown disconnected to emphasize a great variety of possible converter topologies, of which only the very few basic ones will be reviewed here.

Converter topology, however, is not random but has to form effectively a low-pass filter in order to achieve the basic dc-to-dc conversion function.

Although the conversion would be 100% efficient in the ideal case of lossless components such as in Fig. 2, in practice each of the components in Fig. 2 is lossy, thus leading to reduced efficiency. For example, a switch implemented by semiconductor devices is lossy, as in the real physical inductor, when its windings resistance and core losses are taken into account. Transformers and capacitors similarly further degrade the efficiency. Therefore, the prime objective in switched-mode power conversion becomes to realize the given conversion function, (such as dc-to-dc conversion) with the least number of components to improve its overall efficiency and reliability.

Let us therefore now take a closer look at some of the simplest ways that dc voltage conversion may be accomplished. In parallel with introduction of the basic switching dc-to-dc converter configurations, some rudimentary methods for their analysis will be explained.

3. DC-TO-DC CONVERTER TOPOLOGY FUNDAMENTALS

The simplest dc-to-dc converter topologies consist of a single switch (single-pole, double-throw ideal switch S in Fig. 3), a single inductor, and a single capacitor. Let us now see how by different arrangement of this limited number of components (Fig. 3) a number of useful and different dc-to-dc conversion functions can be realized.

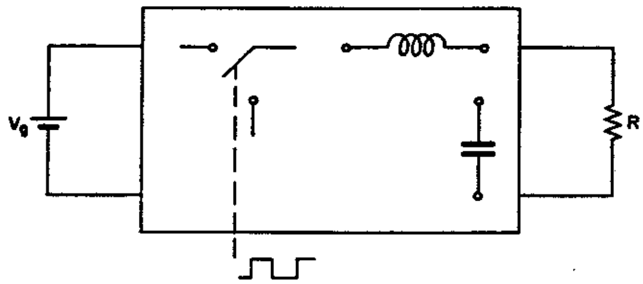

Fig. 3. All three simple dc-to-dc converter topologies: the buck, the boost and the buck-boost can be obtained by simple rearrangement of the three components: ideal switch, inductor and capacitor.

3.1 Buck (Step-Down) Dc-to-Dc Converter

The simplest configuration to understand is the basic buck converter shown conceptually in block diagram form in Fig. 4. The input dc voltage V_g is chopped by the switch S (hence the widely used name "chopper" for this converter type) resulting in an intermediate pulsed waveform v_i. Low-pass filtering of this waveform passes only the average DV_g to form the output dc voltage $V = DV_g$. Here the duty ratio D is defined as the ratio of the on-time interval (switch S in supply V_g position) to the total switching interval T_s. As seen in Fig. 4, by controlling the duty ratio of the switch (dotted line), the output dc voltage is controlled (dotted line).

Frequency Viewpoint (Fourier Analysis)

The output voltage is not ideal as seen in Fig. 4, but in addition to a dc component it consists of a small ripple voltage component at the switching frequency $f_s \triangleq 1/T_s$, as seen in Fig. 5. A frequency viewpoint customary to engineers, becomes very useful here. Namely, the pulse-width-modulated (pwm) voltage waveform at the input of the low-pass LC filter (in Fig. 5, $D = 0.5$ is illustrated) may be broken down into its dc component

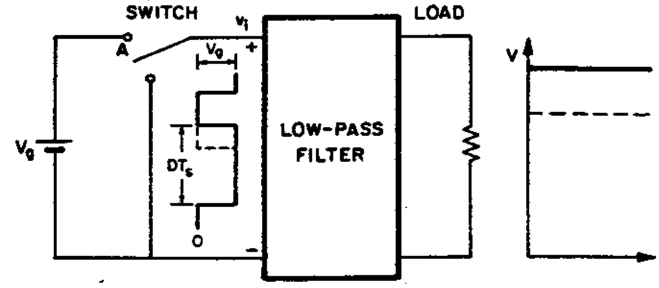

Fig. 4. Controlled dc-to-dc power conversion in a basic buck converter through pulse width modulation.

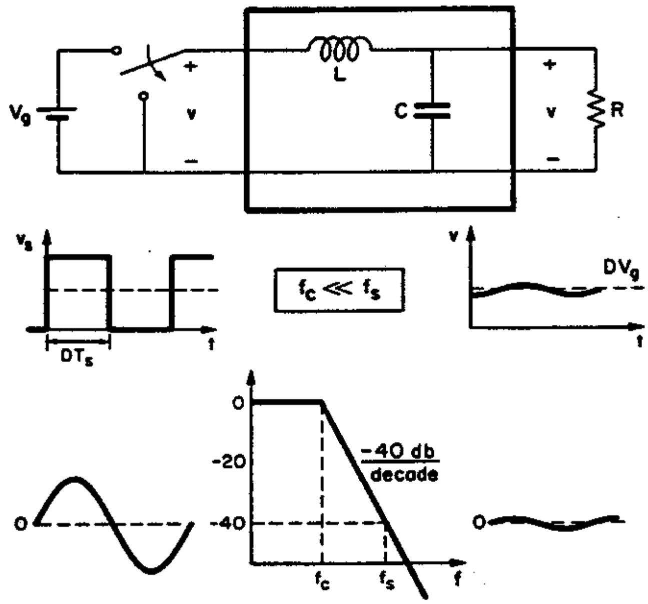

Fig. 5. Frequency viewpoint reveals that for low output switching ripple filter corner frequencies must be well below switching frequency.

and harmonics at the switching frequency f_s and its integer multiples by use of the Fourier series. The dc component passes unattenuated through the filter to generate its primary desirable dc output $V = DV_g$.

Provided that the filter corner frequency $f_c = 1/2\pi\sqrt{LC}$ is significantly lower than the switching frequency (typically at least a decade below f_s), the first and higher order harmonics are substantially attenuated by passing through the LC filter, resulting in an acceptably low switching ripple voltage at the output. A quantitative expression for the switching ripple can be obtained easily by examination of the characteristic waveforms in the switching converter.

Characteristic Waveforms in Switching Converters and Evaluation of Switching Ripple

The small switching ripple of the converter (typically specified to be less than 1%) directly translates into the idealized rectangular voltage waveform and triangular current waveform on the inductors seen in Fig. 6. The rising and falling slopes of the inductor current ripple are easily deduced from the corresponding linear switched network to be $(V_g - V)/L$ (for interval DT_s), and V/L (for interval $D'T_s$), since voltage ripple is being neglected.

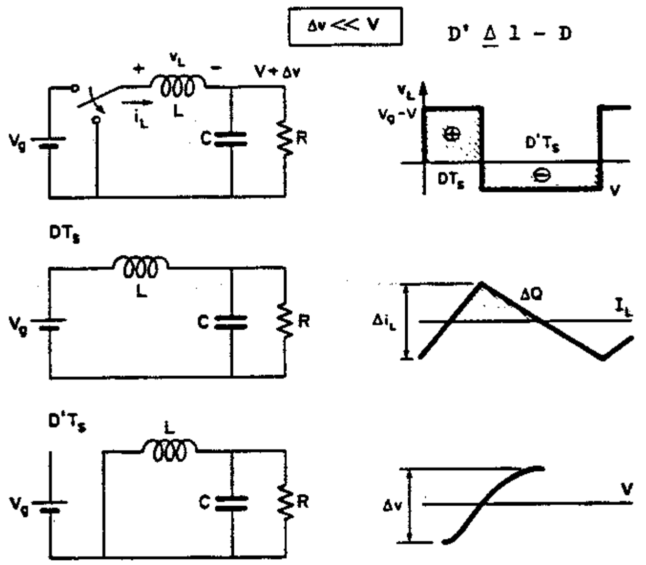

Fig. 6. Quantitative evaluation of the output voltage switching ripple through characteristic waveforms in switching converters.

To calculate the switching output voltage ripple Δv, it is assumed that the average inductor current I flows into the load resistance R to generate the dc voltage $V = IR$, while the inductor current ripple Δi_L flows into the output capacitor to generate the output voltage ripple Δv. This is very good approximation for small switching ripple. Since the capacitance voltage is the integral of its current, $v = \int i dt$, and since the capacitor ripple current is triangular in shape, the voltage ripple typically consists of segments of two parabolas. The total voltage ripple Δv is easily obtained from the stored charge ΔQ, which corresponds to the area under inductor current ripple. Hence

$$\Delta Q = \frac{1}{2}\left(\frac{DT_s}{2} + \frac{D'T_s}{2}\right)\frac{\Delta i_L}{2} = \frac{1}{8} T_s \Delta i_L \tag{1}$$

From the falling slope of the inductor current V/L,

$$\Delta i_L = \frac{V}{L} D'T_s \tag{2}$$

Thus the absolute output voltage ripple is

$$\Delta v = \frac{\Delta Q}{C} = \frac{1}{8}\frac{T_s \Delta i_L}{C} = \frac{1}{8}\frac{D'T_s^2}{LC} V \tag{3}$$

and the relative voltage ripple $\Delta v/V$ is

$$\frac{\Delta v}{V} = \frac{1}{8}\frac{D'T_s^2}{LC} \tag{4}$$

Restated in terms of the corner frequencies,

$$\frac{\Delta v}{V} = \frac{\pi^2 D'}{2}\left(\frac{f_c}{f_s}\right)^2 \text{ where } f_c \triangleq \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

For example, for $D = 0.5$, $f_c = 500\text{Hz}$, $f_s = 20\text{kHz}$, the output voltage ripple is 0.154%.

This result for the buck converter can be generalized for other switching converters:

$$\text{small switching ripple} \Rightarrow \text{natural frequencies} \ll \text{switching frequency} \tag{6}$$

As a consequence of this basic requirement for small switching ripple, the voltage waveforms on the inductors in many converters have the typical rectangular shape. This then serves as a basis for an alternative way of finding steady-state (dc) voltage and current relationships in switching converters.

Steady-State (Dc) Analysis and Volt-Sec Balance on Inductors

In the buck converter, the switching function and filtering function are clearly delineated (cascade connection of the two) such that application of Fourier transform analysis was possible. However, in many more complex switching converters, and even in some simple ones such as the boost and buck-boost, the switching action is buried within the low-pass filter network, and an alternative more general method for finding the dc conditions must be found.

From Faradey's law for the inductor voltage,

$$v_L = L\frac{di_L}{dt} \tag{7}$$

and by integration over the full period T_s, we get

$$\frac{1}{L}\int_0^{T_s} v_L dt = \int_0^{T_s} di_L = i_L(T_s) - i_L(0) = 0 \tag{8}$$

since in the steady state, the initial and final values of the inductor current must be equal. Removal of the finite (nonzero) proportionality constant L in (8) results in a general criterion for the steady-state, the so-called volt-second balance on the inductor, as:

$$\int_0^{T_s} v_L dt = 0 \qquad \text{volt-sec balance on inductors} \qquad (9)$$

or, for the two switched intervals,

$$\underbrace{\int_0^{DT_s} v_L dt}_{\text{volt-second stored}} = \underbrace{- \int_{DT_s}^{T_s} v_L dt}_{\text{volt-second released}} \qquad (10)$$

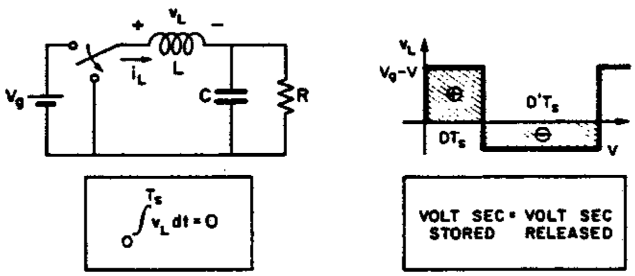

Fig. 7. General method for finding the steady-state conditions in switching converters: Volt second balance on inductors.

The basic requirement for low ouput voltage ripple (6) directly translates into the rectangular voltage waveform on the inductor, since the ripple is neglected as illustrated for the buck converter in Fig. 7. This further simplifies the calculations and reduces them to a simple product of voltages and time intervals. For example, for the buck converter in Fig. 7, the volt-second balance becomes

$$(V_g - V)\, DT_s = VD'T_s \qquad (11)$$

and, after simplification, the stepped-down conversion ratio of the buck converter is obtained as

$$\frac{V}{V_g} = D \qquad (12)$$

Since the converter is ideally 100% efficient (no second-order parasitic elements taken into account), the ratio of the output dc current and average input current is the inverse of (12):

$$\frac{I}{I_g} = \frac{1}{D} \qquad (13)$$

Thus, the buck converter dc conversion function can be modeled by a simple dc-to-dc transformer whose turns ratio is equal to duty ratio D, as shown in Fig. 8. Note, however, that the current conversion ratio (13) is referred to the *average* and *not instantaneous* input and output currents, which as seen from Fig. 8 substantially deviate from the ideal constant (dc) currents. In particular, the input current consists of large pulses, which often cause the so-called *conducted* electromagnetic interference (EMI) on the source lines. This *pulsating* input current causes substantially higher EMI problems than the *nonpulsating* output inductor current (the double-pole inductive filter of Fig. 5 is assumed here).

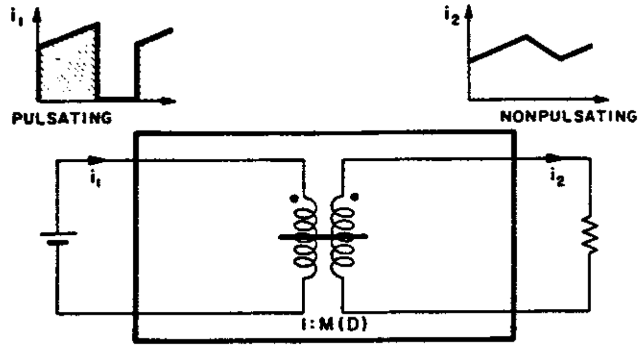

Fig. 8. Input and output currents in the buck converter of Fig. 7 and the definition of pulsating and nonpulsating currents.

Semiconductor Implementation of the Switching Action

To fully gain electronic control of the converter, a semiconductor implementation of the single-pole, double-throw switch is desired. Two alternative implentations, using a diode and a bipolar transistor (either npn or pnp type), are shown in Fig. 9. In either case the diode works in synchronism with the transistor, which is the only controlled device. When the transistor is turned ON, the input dc voltage reverse-biases the diode and turns the diode OFF for interval DT_s. Then, when the transistor turns OFF, the inductor voltage reversal forward biases the diode and turns it ON (inductor current flow cannot be interrupted instantaneously). Note, however, that this semiconductor

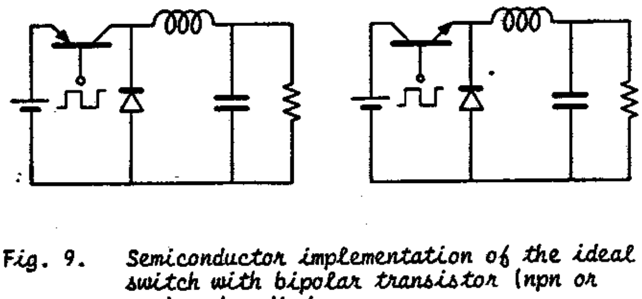

Fig. 9. Semiconductor implementation of the ideal switch with bipolar transistor (npn or pnp) and a diode.

implementation simulates the original ideal switch only in a limited fashion. Namely, while the ideal switch conducts current in either direction and can block voltage of either polarity (hence, it could be termed a *four-quadrant* switch), the shown semiconductor version limits the current flow to only one direction and blocks voltage of only one polarity (hence it could be designated a *single-quadrant* switch). Thus, this implementation by its nature limits the whole converter to *single-quadrant* operation, that is, only one voltage and one current polarity are available at the output. In a later section, it will be shown how the removal of the limitations imposed by the switch implementation may lead to a two-quadrant converter and eventually to a four-quadrant converter.

3.2 How to Create Step-Up (Boost) Function

The simple buck converter of Fig. 5 achieves dc voltage conversion very efficiently compared to its linear regulator counterpart, but still retains some of its limitations: it is capable of only reducing (stepping-down) the input dc voltage.

However, only a very simple step is needed to create a step-up (boost) converter from the original buck converter, as shown in Fig. 10. The buck converter pulsating input current (Fig. 8), often requires an input filter to smooth out large current variations. Hence the buck converter of Fig. 10a has an input capacitance to reduce current ripple returned to the source.

A simple interchange of the source and load (bilateral inversion) generates a boost converter from the original buck converter.

The dc gain of the new boost configuration, due to the nature of source and load interchange, is equal to the reciprocal of the buck converter gain (12), that is, the boost converter gain becomes:

$$\frac{V}{V_g} = \frac{1}{D} \geq 1 \quad \text{for} \quad D \; [0,1] \tag{14}$$

Practical boost converter implementation by use of an npn bipolar transistor as a controlling device and a diode is shown in Fig. 11, in which the input capacitance is also omitted as nonessential for basic operation of the converter. Hence, again, conversion is realized by the least number of components: a single switch, inductor, and capacitor put together into a different topology. However, this time the low-pass LC filter is "broken" by the switching action, thus mixing the chopping and filtering functions which were easily differentiated in the buck converter. Thus, the volt-sec balance on the inductor as a general criterion, and the boost converter waveforms of Fig. 11, lead to the steady-state (dc) voltage gain as:

$$\frac{V}{V_g} = \frac{1}{1 - D} \tag{15}$$

Note that here the duty cycle D determines interval DT_s during which the transistor is turned ON as is customary in all converters, while expression (14) actually referred to the switch closed during its complementary interval D', and hence the D⇒D' conversion.

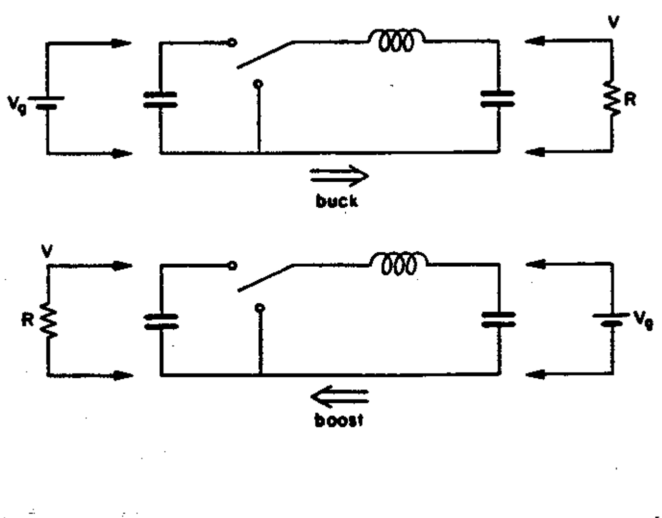

Fig. 10. How to create a step-up (boost) converter from a step-down (buck) converter by a process of bilateral inversion.

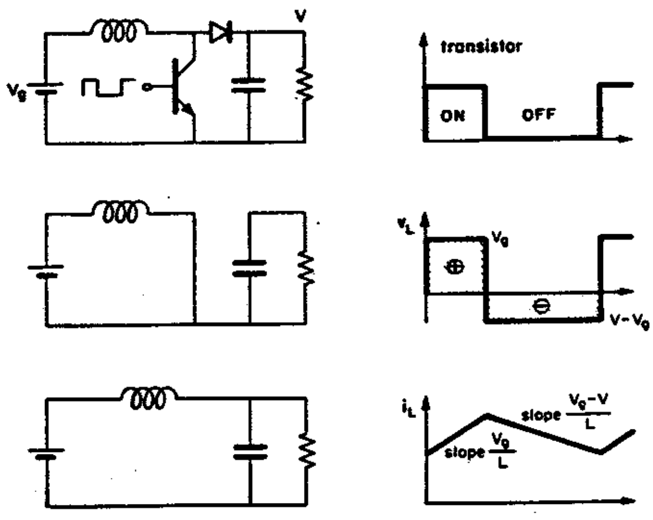

Fig. 11. Analysis and characteristic waveforms in the boost converter.

Effect of Parasitics on Voltage Gain and Efficiency

The importance of including some lossy elements in the converter analysis now becomes quite obvious, since otherwise the obtained results may even be qualitatively misleading. For example, the dc voltage gain of the boost converter (15) becomes infinitely large when the duty ratio D approaches 1, clearly a physically incorrect result. However, the inclusion of some lossy elements, such as the parasitic resistance R_ℓ of the inductor, corrects this problem. The efficiency of course, is now reduced from the original 100%, because of the $I_\ell{}^2 R_\ell$ loss on the inductor resistance, to:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{V^2/R}{V^2/R + I_\ell{}^2 R_\ell} \qquad (16)$$

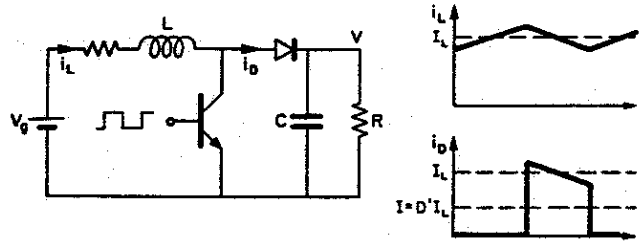

Fig. 12. Pulsating output (diode) current is a source of boost converter inefficiency at high duty ratios.

From the inductor and diode current waveforms in Fig. 12, the ratio of the average inductor I_L and the load current I becomes

$$\frac{I_\ell}{I} = \frac{1}{D'} \qquad (17)$$

and the efficiency becomes

$$\eta = \frac{1}{1 + \alpha/(1-D)^2} \quad \text{where } \alpha \triangleq \frac{R_\ell}{R} \qquad (18)$$

By use of this result, and since efficiency is alternatively $\eta = VI/V_g I_L$, the voltage gain becomes:

$$\frac{V}{V_g} = \frac{I_L}{I}\eta = \frac{1}{1-D} \; \frac{1}{1 + \alpha/(1-D)^2} = \frac{1-D}{(1-D)^2 + \alpha} \qquad (19)$$

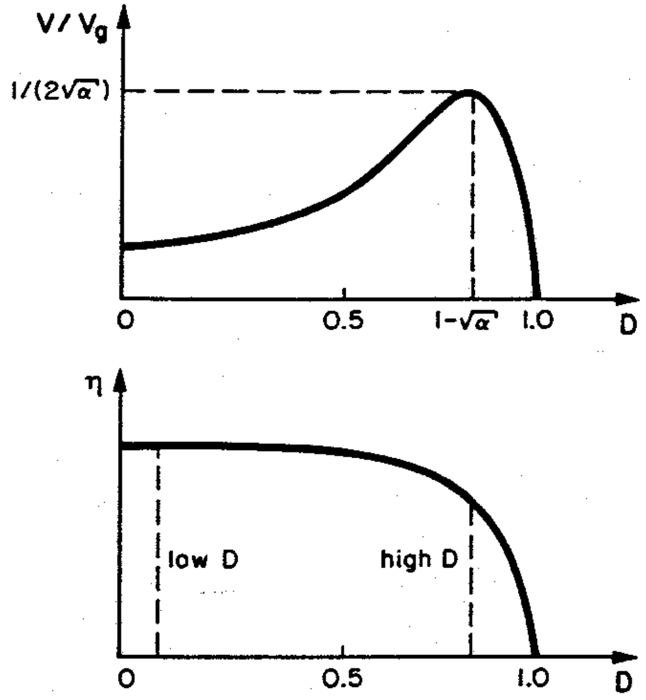

Fig. 13. Voltage gain and efficiency of the boost converter deteriorate significantly at high duty ratios.

As seen in Fig. 13, the voltage dc gain now correctly exhibits a maximum value over the duty ratio D range. Also, the efficiency is seen to decrease significantly for higher duty ratios. Comparison of the inductor and diode current waveforms at low and high duty ratios reveals the source of gross differences in efficiencies at the two extremes (low and high duty cycle), as illustrated in Fig. 14.

For low duty ratio, the average diode current I_D (equal to dc load current I), is almost equal to the average inductor current I_L. Thus, the resistive inductor loss $P_{loss} = I_L{}^2 R_\ell$ and power delivered to the load I^2R are roughly in the ratio R_ℓ/R. Hence for $R_\ell/R = 1/100$, the efficiency loss is very good, around 1%. However, for the same amount of power delivered to the load at high duty ratio D, the diode current has to be a narrow pulse of high magnitude (Fig. 14), such that its average value over the full cycle is unchanged. But, the height (magnitude) of this pulse also determines the average inductor current, which now becomes several times, or even an order of magnitude, higher than the delivered dc load current. The final consequence is that on the *same* inductor resistance it generates a considerably higher loss. For example for D = 0.8, and $R_\ell/R = 0.01$ as before, the efficiency loss becomes $I_\ell{}^2 R_\ell/I^2R = 25\%$, or 25 times higher.

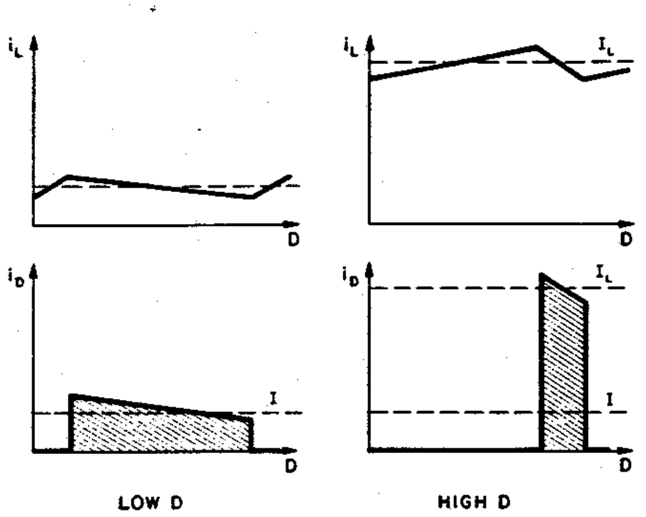

Fig. 14. Inefficiency of boost converter at high duty ratio is attributed to the narrow pulse, high magnitude output diode current.

This example clearly demonstrates the two important facts associated in general with switching converters:

1. The presence of even minute parasitic elements can signficantly alter even the qualitative behavior of switching converters (infinite dc gain vs. finite dc voltage gain, infinite Q factors vs. finite damping factors for dynamic considerations).

2. Pulsating currents in general lead to inefficient use of nonideal physical components (resistive losses in inductors and capacitors etc.), and should be minimized as much as possible.

This last point is further reinforced by consideration of the input current in the buck converter (Fig. 8). Owing to its pulsating nature, discharge of the input dc battery will cause, in its internal source resistance, considerably higher loss than for a smooth (nonpulsating) current. The difference will be higher, the lower the duty ratio of the switch, for the same reason as before — narrow pulse of high magnitude. Thus, pulsating current at either input or output is undesirable for inefficiency as well as high conducted noise reasons. Later (Section 3.4), a converter which meets this criterion will be presented.

The buck converter can only step-down input dc voltage, the boost converter can only step-up dc voltage. Let us now synthesize a converter which can perform either of these two functions.

3.3 How to Create the General Step-Down or Step-Up Function

The previous two converters can now be viewed as emanating from switching the single inductor (inductive energy transfer) between the input (dc source) and the output port (dc load with capacitance across it), as illustrated in Fig. 15a and b. The remaining third possibility, in which the inductor is grounded, results in the buck-boost converter of Fig. 15c.

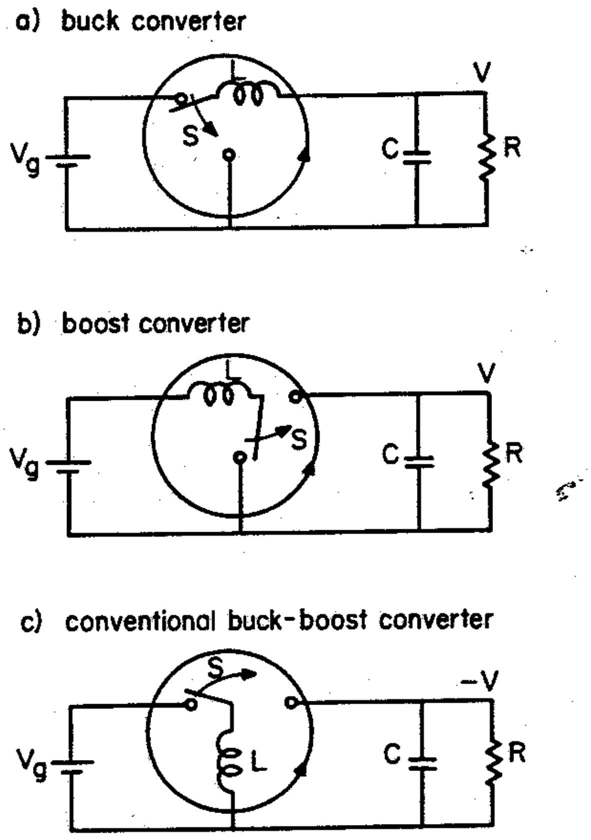

Fig. 15. Generation of three basic inductive energy transfer converters by cyclic rotation of the inductance in series with a switch.

From the usual volt-sec balance in steady-state, the dc voltage gain is

$$\frac{V}{V_g} = \frac{D}{1 - D} \tag{20}$$

Thus either a step-up ($D > 0.5$) or a step-down ($D < 0.5$) function can be achieved in the same converter. As before in the boost converter, inclusion of inductor parasitic resistance results in a finite voltage gain instead of the infinite gain given by (20) for $D = 1.0$.

So far the switch has been considered ideal. However, the semiconductor implementation as shown in Fig. 16 results in additional efficiency loss.

Effect of Switch Nonidealities on Efficiency

The semiconductor switch may well be approximated by two batteries (Fig. 16): one modelling the saturation voltage drop of transistor V_s, and the other the forward voltage drop of the diode V_F. Leakage currents in both devices when they are off can safely be neglected. To simplify derivations and observations, we now assume that the inductors are *ideal* and consider only efficiency loss due to switch nonidealities. From the input and output pulsed current waveforms, the average currents are calculated, and so the efficiency η is

$$\eta = \frac{VD'I_L}{V_g DI_L} = \frac{V/V_g}{D/D'} = \frac{\text{real voltage gain}}{\text{ideal voltage gain}} \tag{21}$$

However in steady-state the volt-sec balance still applies, and results in

$$(V_g - V_s)DT_s = (V + V_F)D'T_s \tag{22}$$

$$\frac{D}{D'} = \frac{V + V_F}{V_g - V_s} \tag{23}$$

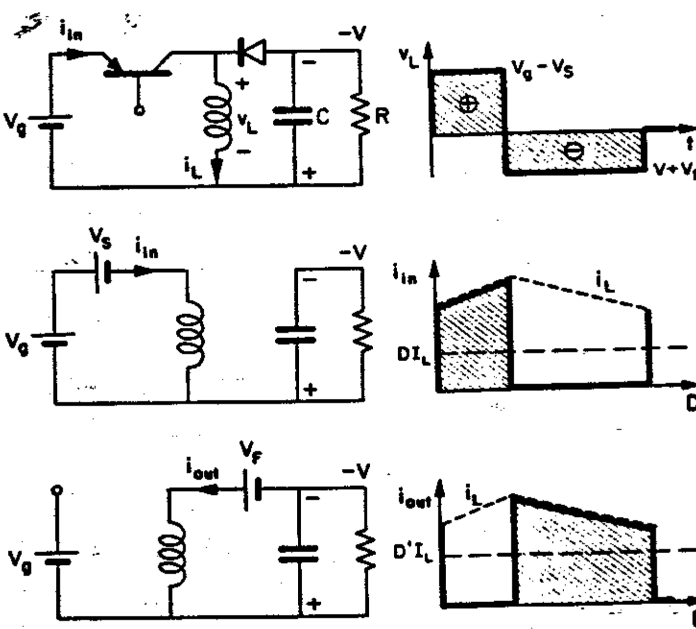

Fig. 16. Converter efficiency in presence of switch nonidealities (nonzero transistor and diode voltage drops).

Substitution of (23) in (21) finally gives

$$\eta = \frac{V_g - V_s}{V_g}\,\frac{V}{V + V_F} \tag{24}$$

In the special case of the buck-boost converter, this result could have been obtained from consideration of "input" and "output" circuit efficiency η_I and η_O, respectively

$$\eta_I = \frac{(V_g - V_s)I_{in}}{V_g I_{in}} = \frac{V_g - V_s}{V_g}$$

$$\eta_O = \frac{VI_{out}}{(V + V_F)I_{out}} = \frac{V}{V + V_F} \tag{25}$$

$$\eta = \eta_I \eta_O$$

The form of the result (24) is very illuminating and leads to a general conclusion:

High efficiency is difficult to obtain even with switching converters when either input or output voltages are low and comparable to transistor and diode drops.

For example, for 3V output, efficiency degradation is 25% due solely to the inclusion of the diode drop $V_F = 1V$. A diode with a lower voltage drop (such as a Schottky diode) would improve efficiency. A transistor with a high saturation voltage causes similar efficiency degradation on the input side for low input voltages. Simultaneous low input and low output voltage conversion is apparently even more inefficient.

However, these dc losses are not the only semiconductor losses since, in addition, switching losses are generated in the semiconductors as well. Namely, during the switching between its ON and OFF states which does not happen instantaneously, the transistor travels through its linear high dissipation region as illustrated in Fig. 17. Integration of the instantaneous power (product of transistor voltage and current) over the transition interval and its averaging over the switching period results in switching losses. New MOSFET power transistors have much shorter switching times (rise and fall times) than comparably rated bipolar transistors, hence reduced switching losses, but their dc losses are higher due to still substantial ON resistance of the device. Note that a power FET is appropriately modelled by its ON resistance (typically 0.3Ω – 3Ω range) rather than the battery V_s as in the bipolar transistor case. Thus, the inclusion of all losses (semiconductor losses, parasitic resistance losses, core losses in magnetic components etc.) may lead to substantial deviation from the ideal 100% efficiency.

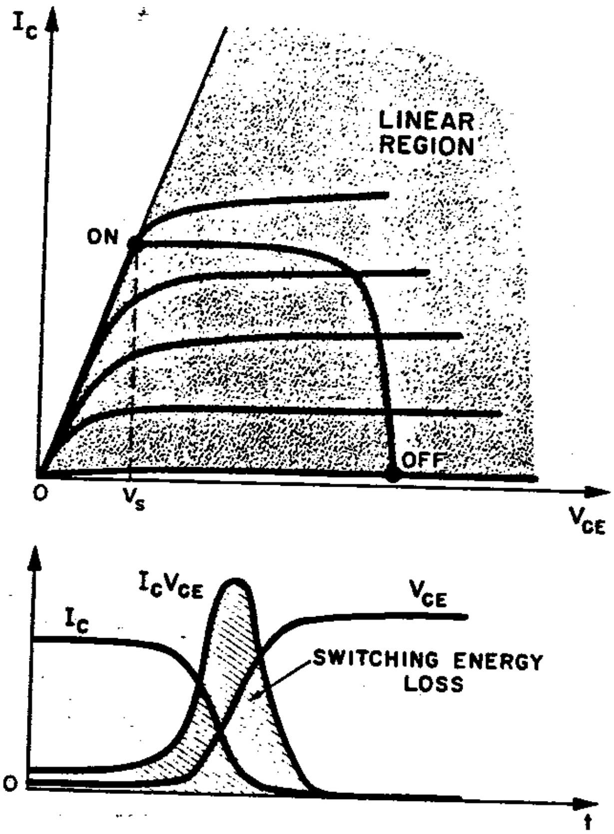

Fig. 17. Finite semiconductor switching times lead to switching losses during transition between the ON and OFF states.

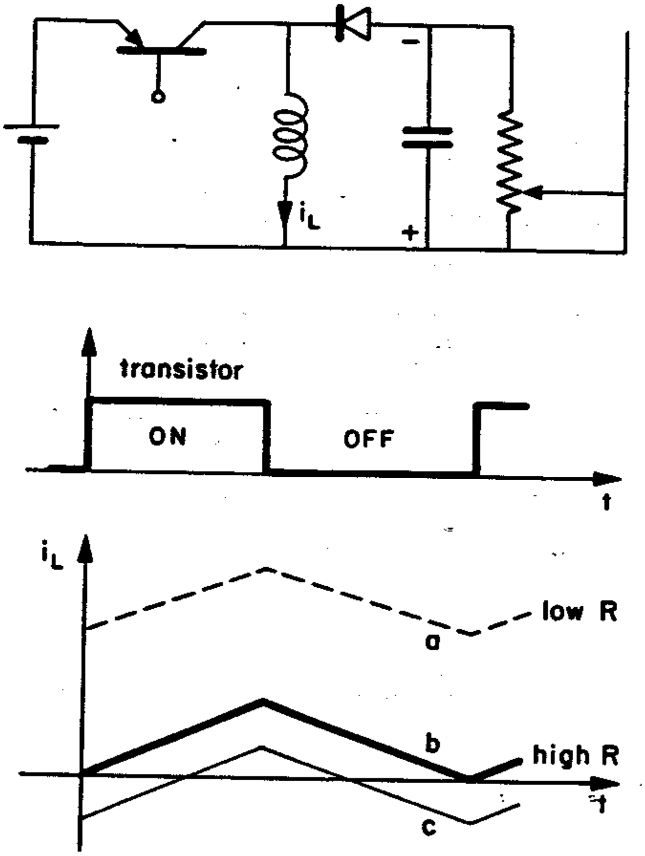

Fig. 18. Decrease of the load current below some critical value (waveform b) leads to a new mode of operation: discontinuous conduction mode.

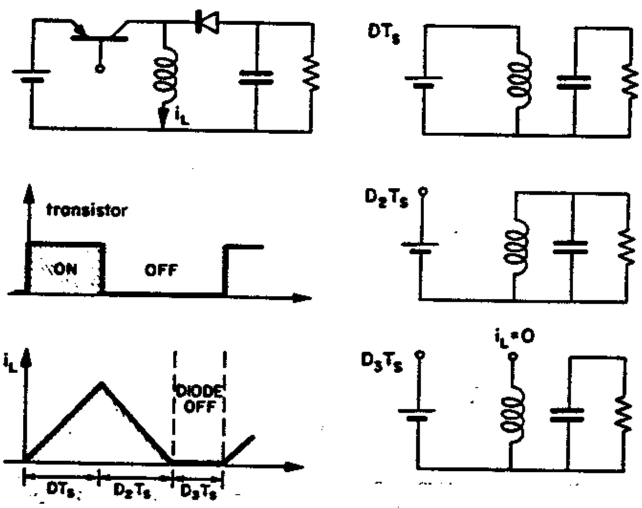

Fig. 19. Salient features of the discontinuous conduction mode illustrated on the buck-boost converter.

Discontinuous Conduction Mode

In practice load current may change over a wide range, from no load to full load, and it is desirable that converter operation not be significantly affected. However, this is not so as illustrated in Fig. 18. Namely, increase of load resistance leads to a decrease of load current, hence the average inductor current is continuously reduced from waveform a in Fig. 18 to waveform b. Nevertheless, further decrease of the load current *does not* produce waveform c. The waveform c would require that the inductor current falls to zero and *reverses its direction during* the transistor OFF time. However, the diode is a current unidirectional element and does not conduct current in the opposite direction. Hence at the instant defined by waveform b in Fig. 18, a new mode of converter operation is encountered termed discontinuous conduction mode (DCM). Further decrease of load current beyond that point results in the typical discontinuous inductor current waveform shown in Fig. 19 from which the name originated. The inductor current, after reaching zero level in interval D_2T_s, stays at this level for the remaining part of the $D'T_s$ interval (D_3T_s), thus resulting in a third linear network for which both transistor and diode are OFF.

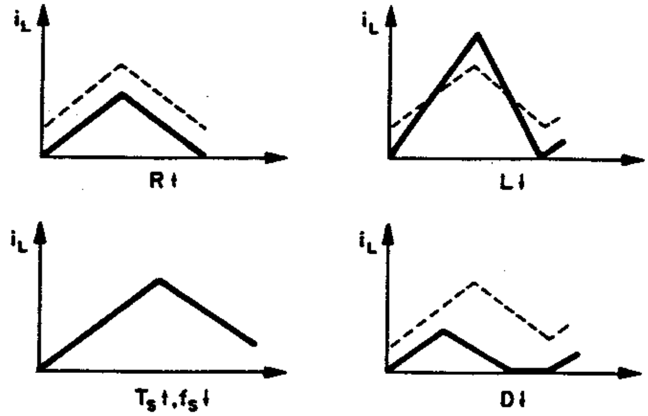

Fig. 20. Four parameters are affecting discontinuous conduction mode: decrease of load current, inductance L, switching frequency f_s and duty cycle D.

As seen from Fig. 20, in addition to increase of load resistance, other parameters are those which affect the inductor current ripple: decrease of inductance value, increase of switching period and decrease of duty ratio. The first three can conveniently be lumped into a single dimensionless parameter K

$$K = \frac{2L}{RT_s} \tag{26}$$

whose reduction in value leads to the discontinuous conduction mode. Note that the decay interval D_2T_s and the voltage gain M are as yet undetermined:

$$\frac{V}{V_g} = f_1(D,K) \tag{27}$$

$$D_2 = f_2(D,K) \tag{28}$$

However, from the volt-sec balance on the inductor (Fig. 21)

$$\frac{V}{V_g} = \frac{D}{D_2} \tag{29}$$

in which the "decay" duty ratio D_2 is still unknown. However, from the instantaneous diode current in Fig. 21 and 100% efficiency assumption,

$$D_2\left(\frac{1}{2}\frac{V}{L}D_2T_s\right) = \frac{V}{R} \tag{30}$$

$$D_2 = \sqrt{K} \quad ; \quad K = \frac{2L}{RT_s} \tag{31}$$

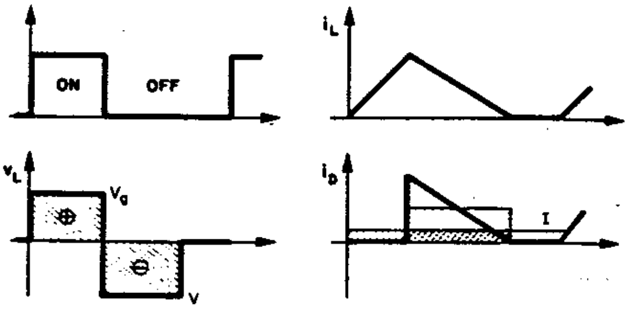

Fig. 21. Evaluation of dc conditions in discontinuous conduction mode (DCM) through waveform observation.

Thus, the solution for (27) and (28) becomes

$$\frac{V}{V_g} = \frac{D}{\sqrt{K}} \tag{32}$$

$$D_2 = \sqrt{K} \tag{33}$$

The converter will then operate in this discontinuous conduction mode whenever:

$$\text{DCM:} \quad D_2 < 1 - D \qquad K < (1 - D)^2 \tag{34}$$

The normal mode of converter operation ($K > (1-D)^2$) is often designated continuous conduction mode (CCM).

Two-Quadrant Converter Concept

The onset of discontinuous conduction mode is triggered by the inability of a diode to conduct current in the reverse direction, that is, because of the *current unidirectional* implementation of the ideal switch. However, if an alternative path is provided for the current to flow in the reverse direction, this mode of operation will be circumvented and continuous conduction mode obtained even in the no-load case. This is shown by addition of another transistor across the diode and another diode across the original transistor, which provide for alternate current flow and realize in hardware a *current bidirectional* switch or, as termed here, a *two-quadrant switch*. The two transistors in Fig. 22 are switched out of phase (when one transistor is ON the other is OFF and vice versa), and the diodes act as synchronous switches. Special precautions usually have to be made (dead time) to guard against their overlapping conduction.

The immediate result of such two-quadrant switch implementation is that the discontinuous conduction mode is completely eliminated, even at no load, as seen in Fig. 22. Note, however, that even though the instantaneous inductor current may become negative, its average current (and also the average diode current) has to be positive, because the power flow is in *average* still from the source to the load (from left to right in Fig. 22). Nevertheless, the direction of power flow can be changed provided an active load such as a battery or motor turning into a generator is used, as illustrated in Fig. 23.

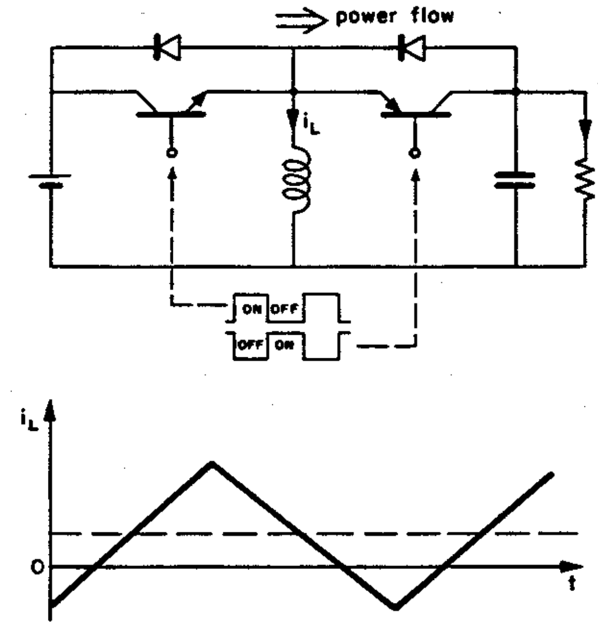

Fig. 22. Bidirectional current implementation of the ideal switch eliminates discontinuous conduction mode even at low load currents.

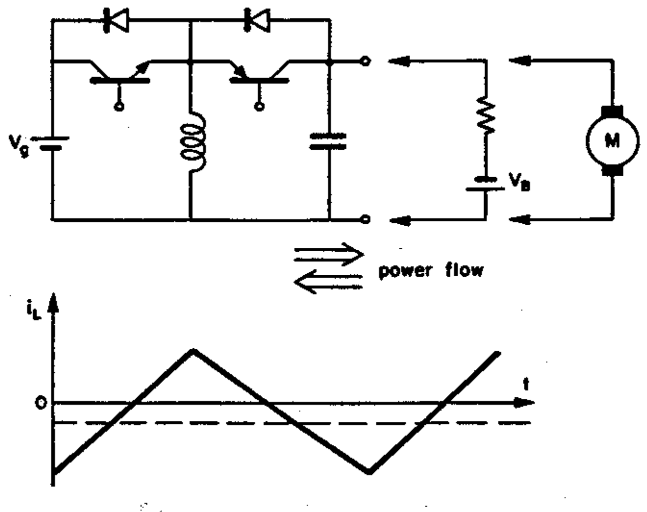

Fig. 23. Bidirectional power flow allows the motor load to become generator, and battery to change from a current sink (charge) to a current source (discharge).

Therefore, the average inductor current can be either positive (battery charging) or negative (battery discharging). Note, however, that the output voltage polarity is the same, negative, for either current direction. Hence, the converter is classified as a *two-quadrant converter:* a single polarity of voltage and two polarities of current, which on voltage vs. current plot would occupy two quadrants. Finally it is apparent that any one-quadrant converter can easily be turned into a two-quadrant converter, provided its switch implementation is current-bidirectional, that is, a two-quadrant switch.

Dc Isolation and Multiple Outputs

For many practical applications dc isolation is required between the input (source) and (load). Besides the main protection reasons and requirement for different output grounds, a number of additional side benefits are achieved, as illustrated on Fig. 24. The dc isolated version of the buck-boost converter (sometimes also referred to as the flyback converter) is obtained in two simple steps: first, the two winding (bifilar or otherwise) inductor is built (Fig. 24a), and then electrical connection between the two windings is broken, thus resulting in the dc isolated version of Fig. 24b. Note, however, that this process itself suggests that the transformer obtained in such a way must have the same inductive storage capability as the original single inductor. This has a rather serious drawback, as will be discussed later in Section 4 on magnetics design, since such a transformer has to be designed to withstand a dc bias greater than the average input current. Although this may limit its usefulness for higher power designs, the simplicity of the dc isolation generation makes this configuration a viable choice for lower power designs.

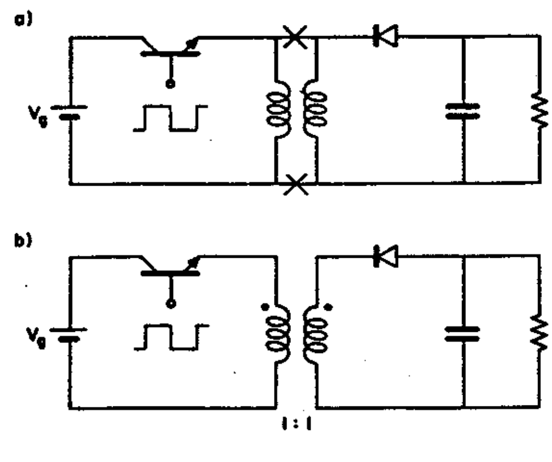

Fig. 24. Simple bifilar windings step (a) leads to a dc isolation in the buck-boost converter (b) through breaking electrical connections.

The isolation feature, brings as a by product some additional benefits (as it does in general for any isolated configuration). A simple change of the isolation transformer turns ratio contributes an additional step-up (or step-down) factor (Fig. 25), which helps alleviate efficiency degradation problems occurring at high duty cycles (as described in Paper 18). Namely, an additional step-up is obtained by the turns ratio without running the converter at an excessively high duty cycle. Finally, the original converter limitation (negative output voltage polarity for positive input voltage polarity) is easily removed by simple interchange of transformer secondary connections (dot polarity marks inverted) and appropriate change of diode direction, as seen in Fig. 25.

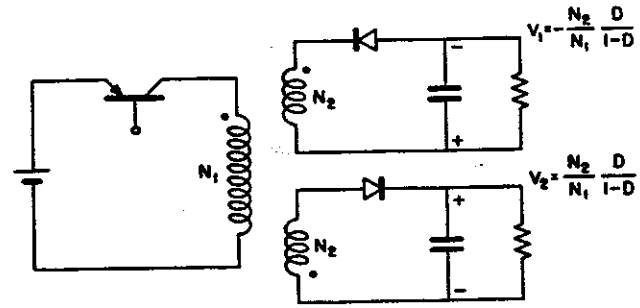

Fig. 25. *Multiple outputs and polarity inversion are immediate additional benefits of the dc isolation transformer.*

Both nonisolated and isolated versions of the buck-boost converter are clear examples of the converter based on *inductive energy transfer* — the input energy is stored in the inductor (or transformer magnetizing inductance) while the transistor is ON, and released to the load when transistor is OFF. As a consequence both input (transistor) and output (diode) currents come in lumps (pulsating currents), which can cause substantial input and output conducted noise — recognized as a potentially serious problem in switching power supplies.

Until recently it was believed that the buck, the boost, and the buck-boost converters were the simplest and the only conceivable single-switch configurations. However, this was readily disproved by the conception of a new single-switch configuration, which in an elegant and optimum manner resolved deficiencies such as pulsating currents and the far from ideal isolation transformer, such as that in the buck-boost converter.

3.4 One Step Closer to the Ideal Dc-to-Dc Converter (Ćuk converter)

With a clearly defined goal of achieving nonpulsating currents, the desired converter configuration gradually emerges: an inductor is needed in series with both input source and output load for either switch position. Then, energy transfer and level conversion is achieved by use of a single capacitance and a single switch as shown in Fig. 26a, or its bipolar transistor, diode implementation in Fig. 26b. Unlike previous single switch configurations, the Ćuk converter is based on *capacitive energy transfer*. Thus its dc current gain may be easily deduced from the capacitor current waveform using a charge-balance method in steady-state (see waveform in Fig. 26)

$$I_1 D'T_s = I_2 DT_s \tag{35}$$

or, from the 100% efficiency argument, the voltage dc gain is

$$\frac{V}{V_g} = \frac{D}{1 - D} \tag{36}$$

that is, the same as for conventional buck-boost (Fig. 24). Note that for simplicity of argument the inductors were assumed to be large enough such that the slope is negligible and results in rectangular current waveforms. The transistor and diode in Fig. 26b operate in the usual synchronous manner: when the transistor is OFF, the diode is ON and the capacitance is charged with polarity direction shown; when the transistor subsequently turns ON, the capacitance voltage reverse biases the diode and turns it OFF. More details about the Ćuk converter, including the original approach to its discovery, are given in Paper 18.

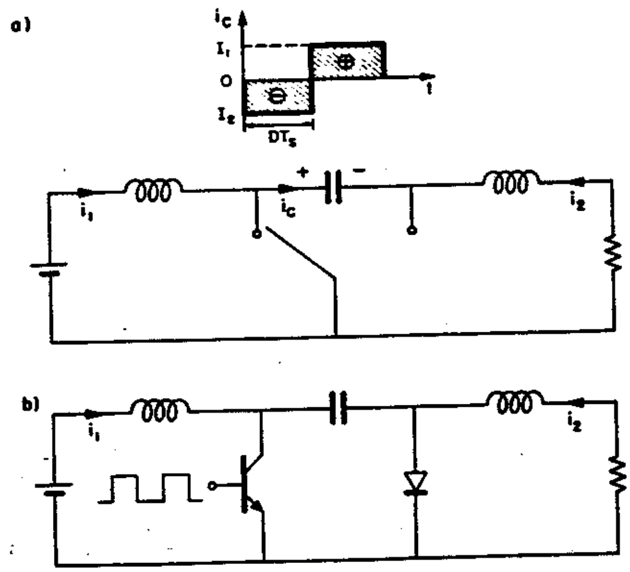

Fig. 26. *Basic Ćuk converter is comprised of two inductors, capacitor, and single switch (a) implemented by a transistor and a diode (b).*